4000 Series Logic and Analog Circuitry

By James M Bryant

This article discusses the benefits of the long-established (for more than forty years) 4000 Series CMOS logic circuits as an almost perfect solution to the problem of providing simple logic in high-performance analog circuitry without compromising analog performance.

All electronic circuits have inputs and outputs (occasionally the only input is the power supply). Circuits that have inputs and outputs with two distinct possible states (binary inputs and outputs) are digital or logic circuits. Ranging in complexity from a single logic inverter to massively complex microprocessors and FPGAs, they process their logic inputs to deliver determinate logic outputs. The majority of modern electronic systems are based on complex logic circuits of one sort or another.

There are many books on logic design and much software to simplify and verify logic. It is not the purpose of this article to discuss the design of logic systems, much less the design of digital computation systems; rather it is to discuss circuit level issues that arise when it is necessary to have simple logical operations in a mainly analog system. Such logic will almost certainly be saturating logic (TTL or CMOS) rather than very-high-speed current-steering types (ECL).

If we need such logic in a mainly analog system there are several things to consider:

- Logic circuitry usually requires a well-defined power supply with a narrow (±20%, ±10%, or sometimes even less) range of values; in the past this supply was generally 5 V, but in recent years several lower supply voltages have become common. Analog circuitry may operate from a much wider range of supply voltages.
- Saturating logic inputs and outputs are defined by the supply rails of the logic circuitry and may not be compatible with signal voltages in analog circuitry.
- Most saturating logic is noisy, generating supply-line noise which can degrade the performance of precision analog circuits.

The 4000 Series

Fortunately, a simple forty-year-old solution provides a family of over 150 logic circuits ideally suited for use in analog circuitry and largely overcomes these issues. This is the 4000 Series CMOS logic family, originally introduced by RCA in 1968 and still widely available from a large number of manufacturers. A list of its most common members is found in Table 1 in the Appendix.

Basic DC Characteristics of the 4000 Series

4000 Series devices will work over a supply voltage range from 3 V to 15 V (and in some cases 18 V—RTFDS[1] to find out which ones). Many precision analog circuits will do the same, making supply regulation unnecessary and simplifying battery-operated circuits. Of course the input and output logic levels will vary with the supply voltage in use (RTFDS again for the threshold values as they vary slightly from manufacturer to manufacturer).

Operating speed and short-circuit output currents also vary with supply voltage, so when 4000 Series devices are used in applications where these may matter it is again important to verify that the required performance is available over the proposed supply voltage range.

The original 4000 Series devices (the A range, with part numbers 4xxxA) had unbuffered outputs. Simplified diagrams of the basic NOR and NAND gates are shown in Figure 1.

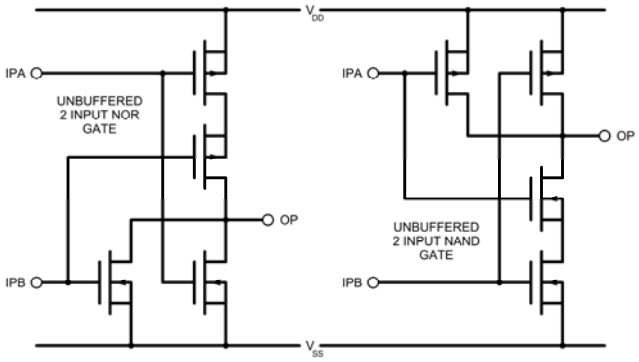

Figure 1. 4000 Series unbuffered 2-input NAND & NOR gates.

Their operation is obvious: if both inputs of the NOR gate are low, the two series PMOS devices are both on; neither of the parallel NMOS devices is on, so the output is connected to V_{DD}. If either input is high, one of the series PMOS devices is off, disconnecting V_{DD} from the output; one of the parallel NMOS devices is on, connecting the output to V_{SS}. The NAND gate is identical except that the NMOS devices are in series and the PMOS ones in parallel; it works in exactly the same way, but inverted. The principle works with additional inputs; the 4068 and 4078 are respectively 8-input NAND and NOR gates.

Some 4000 Series devices are still available in the unbuffered A variety, but today most are found as buffered B types, which have part numbers 4xxxB. In the buffered versions, as shown in Figure 2, inverting buffers are between the actual gates and the input and output terminals.

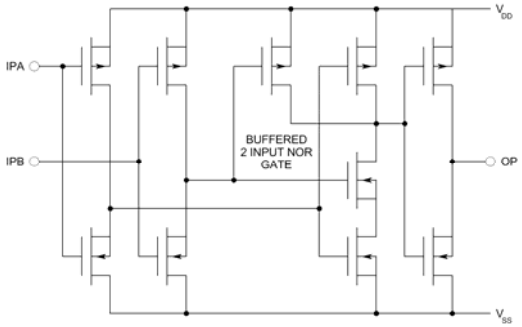

Figure 2. 4000 Series buffered 2-input NOR gate.

These buffers are used only on input and output terminals, not internally between stages in more complex devices. In the simplest buffered gates, there are three stages between input and output instead of one, so buffered devices have faster output slew rate, but slightly slower propagation delay. They are also slightly less vulnerable to damage from electrostatic discharge (ESD).

When a CMOS logic gate of this type is driven with valid logic levels at its input(s) there is no current path between V_{DD} and V_{SS}, so the only current flowing in the power supplies is device leakage, which at room temperature is usually well under 1 μA, plus any current flowing in the output. In general, 4000 Series logic has extremely low current consumption.

If the inputs are outside the correct ranges for logic 0 or logic 1, however, both the PMOS and the NMOS may conduct slightly and the input buffer may draw a current of a few tens or hundreds of microamps. 4000 Series devices are better in this respect than more modern fast CMOS devices, which may have output stage switching transient currents of hundreds of microamps or more. These fast devices therefore inject high-frequency transient noise into their supply rails, which may degrade the performance of precision analog circuitry unless

carefully filtered. They also have higher current consumption when actively handling high-frequency logic.

Even the 4000 Series, though, draws some current when it is handling high-frequency logic signals—in addition to the small switching leakage we have already mentioned. When a logic terminal (input or output) changes state, its internal capacitance or external (load) capacitance must also charge or discharge—which requires a short pulse of current. So, although 4000 Series logic has very small steady-state power consumption, a small current, approximately proportional to the frequency of the signal on the logic inputs, will be drawn from the supply.

To summarize, 4000 Series logic works with supply voltages in the 3-V to 15-V range, draws very little power (a few microwatts) when its inputs are static and its outputs are not loaded, and quite low power (a few milliwatts—for the values for particular devices see the formulae on the individual device data sheets that relate power consumption to supply voltage, input frequency, output frequency and capacitive loading) when it is switching at speeds up to 1 MHz or even more.

Note that these power formulae assume that the inputs are driven with logic levels and that the transition between logic levels takes less than 20 ns. If an input is at a steady potential somewhere between the logic thresholds, both the PMOS and NMOS devices may be partially turned on, and the device will draw additional current of several tens of microamps. Slow transitions between valid logic levels will also increase the mean current slightly.

Of course the power consumption will also increase if any of the outputs are required to drive resistive loads; in such cases it is necessary to invoke Ohm's Law (and the duty cycle) to determine the mean current in the load. The output resistance of buffered 4000 Series output stages is quite high and varies with both supply voltage and temperature (TC = –0.4%/°C). Typical characteristics are shown in Figure 3.

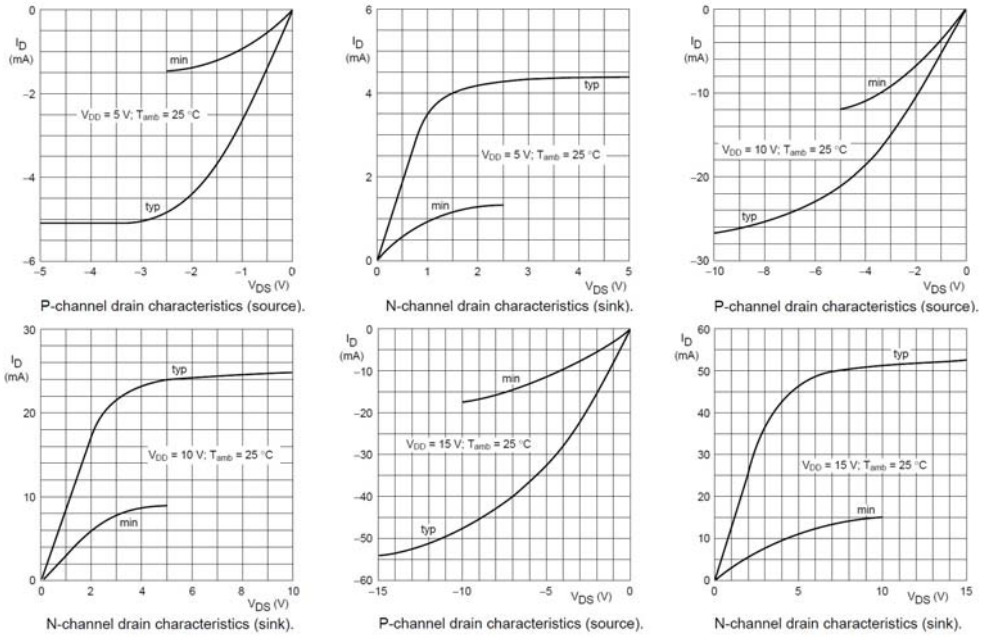

Figure 3. 4000 Series output characteristics.

At lower supply voltages, certainly below V_{DD} = 10V, the output resistance will be high enough that a single output may be short-circuited to either supply without exceeding the absolute maximum output current of 50 mA or the package dissipation of 500 mW. Short-

circuits should be avoided when V_{DD} > 10 V as either or both ratings may be exceeded. At V_{DD} = 5 V, several outputs may be short-circuited without risk.

The circuits in Figure 1 and Figure 2 show the basic functionality of 4000 Series gates, but do not show their input structure in detail. Figure 4 shows the gate input circuitry in more detail. Between the external terminal and the gates of the CMOS devices an arrangement of two diode clamps and a resistor is designed to protect the CMOS gates from damaging circuit voltages and ESD. If the input voltages go above V_{DD} or below V_{SS} one of the diodes conducts and clamps the input voltage.

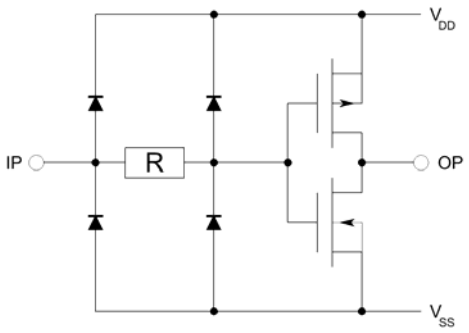

Figure 4. 4000 Series gate input protection circuitry.

These diodes provide efficient protection, provided the voltages and currents do not exceed their absolute maximum values, but if a logic 1 (positive) input is applied to any input of an unpowered array of 4000 Series logic, current will flow through the diode to the V_{DD} rail and, provided the logic source can provide the necessary current, the array will power up and start working. This is rarely a good thing as the logic source may be overloaded and damaged if the current drain of the array is too large. Also, if the array starts working when it is supposed to be unpowered, it may cause unwanted operation of other circuitry or damage it by applying inputs that cannot be tolerated by the unpowered circuitry. It is therefore wise to design systems which ensure that logic signals cannot be applied to unpowered 4000 Series devices.

Unused input pins must never be left unconnected, but should be tied to V_{DD}, V_{SS}, or to an unused input in a multi-input gate (this will, of course, increase the input capacitance).

The capacitance of a typical 4000 Series input is approximately 7.5 pF, and the input resistance is very high indeed (many tens of MΩ). The worst case bias current specified in the data sheet is 300 nA at room temperature (25°C) and only 1 μA at 85°C, but in practice it is usually much lower than this and rarely exceeds a few tens of nanoamps. Thus, the fan-out of a 4000 Series device driving other such devices is almost unlimited as far as current sourcing/sinking is concerned, and is limited only by speed considerations.

AC and Speed Issues of 4000 Series Devices

The purpose of this article is to describe how 4000 Series logic may be used in analog systems where a small amount of control logic is required. It is far from an ideal choice for high-speed applications as its speed is relatively low (MHz to tens of MHz) and varies with its supply voltage (and to a certain extent with temperature). We shall not, therefore, engage in a discussion of how best to use high-speed logic, but simply summarize what speed issues must be considered when using 4000 Series devices.

The speed, in terms of propagation delays of gates or maximum input frequencies for flip-flops and dividers, is defined, for V_{DD} of 5 V, 10 V, and 15 V—and often by a formula for other supply voltages as well—on the individual device data sheets. Typical gate propagation delays are of the order of 50 ns to 120 ns at V_{DD} = 5V and 20 ns to 50 ns at V_{DD} = 15 V. An additional term in the formula accounts for the speed reduction caused by load capacitance. A

more detailed description of 4000 Series switching, together with definitions of all the terms used, may be found in the device family specification document on the NXP website.[2]

If the input transition time is too long, there is a risk that the logic gate at the input may appear to oscillate due to noise amplification. As a general rule, the input transition times should not exceed 15 µs at V_{DD} = 5V, 4 µs at 10 V, and 1 µs at 15 V. In analog systems, this transition time limit may well cause problems, but Schmitt trigger inputs provide a simple way of overcoming the problem.

Schmitt Trigger Inputs

The input buffer shown in Figure 4 behaves as an inverting amplifier over a range of inputs somewhere approximately midway between logic 0 and logic 1. If the input is in this range, any noise is amplified and may cause additional unwanted logic transitions at the output. With a more complex buffer that has positive feedback, known as a Schmitt[3] trigger, the output remains in one logic state until the input passes a threshold when it immediately (subject to normal switching speed limitations) switches to the other state and will not go back to its previous state until the input has moved back some distance towards its original state. The gap between the two thresholds is known as the hysteresis. A simplified diagram of a (non-inverting) Schmitt input buffer is shown in Figure 5. Note that the MOS devices PMOS(a) and NMOS(a) are several times larger than the devices PMOS(b) and NMOS(b).

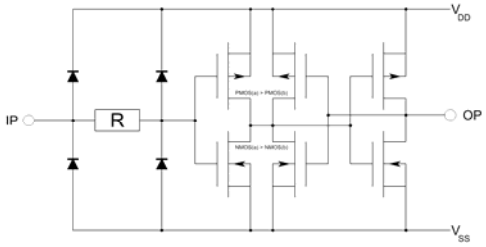

Figure 5. Schmitt input non-inverting buffer (simplified diagram).

The transfer characteristics of a simple buffer and a Schmitt input buffer are shown in Figure 6A and Figure 6B, respectively. The basic buffer characteristics are those of an amplifier, but the Schmitt device is different. As the input is increased, the output does not change until the input reaches VT1, when it abruptly switches from V_{SS} to V_{DD}. Positive or negative changes at the input then have no effect on the output unless the input is reduced to VT2, when the output changes equally abruptly to V_{SS}.

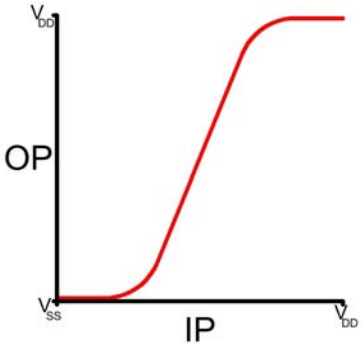

Figure 6A.

Transfer characteristics of a basic CMOS buffer.

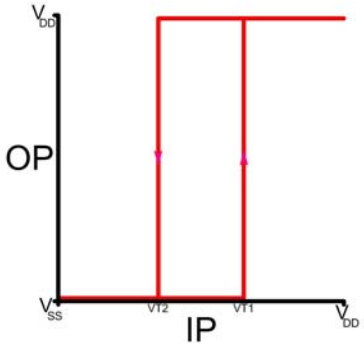

Figure 6B.

Transfer characteristics of a Schmitt input buffer.

This behavior is very useful, as it allows logic to be driven by slowly changing analog signals without noise problems. The only drawback of Schmitt input circuits is that they draw

hundreds of microamps of supply current when their input is between the upper and lower logic threshold voltages.

A number of 4000 Series counters and MSI devices have Schmitt inputs to their clock and oscillator circuitry. There are also three basic Schmitt input devices: the 4093 quad 2-input NAND gate with Schmitt inputs on all the gates, and the 4584 and the 40106 hex (six in one package) inverting buffers. The typical hysteresis differs from device to device, over supply voltage, and over temperature. It also varies somewhat between manufacturers, so it is sensible to consult the data sheet of the actual device to be used before designing timers or oscillators using Schmitt input gates.

Using Schmitt Input Gates as Oscillators and Timers

In addition to their obvious application in preventing noise problems with slowly changing signals, Schmitt input gates may be used as oscillators and pulse generators. A single Schmitt input inverter and two other components make a convenient, if not particularly precise, oscillator. The circuit and waveforms of such an oscillator are shown in Figure 7.

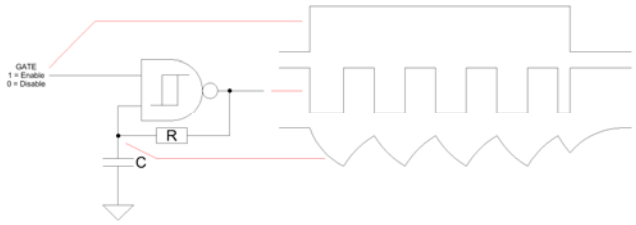

Figure 7. Basic oscillator using a Schmitt input CMOS inverting gate.

This oscillator has an operating frequency somewhere between 0.5 and 2 times 1/RC (I said it was not particularly precise!) and an output mark:space ratio of approximately 1:1, but this, again, is not precise as VT1 and VT2 are not very symmetrically placed about the midpoint of the power supply. If an exact 1:1 mark:space is required, it is better to use the oscillator at twice the required frequency to drive a flip-flop as a 2:1 divider.

If a gate from a 4093 is used as such an oscillator, it may be turned on and off by a control signal on the other gate input: logic 1 enables the oscillator, logic 0 disables it. Note that the first half-cycle is longer than subsequent ones.

This oscillator may be modified to give a pulse train with programmed (but not very accurate) mark:space ratio by using an additional resistor and a diode. This modification is shown in Figure 8. For short pulses R1<<R; for negative-going pulses the diode should be reversed.

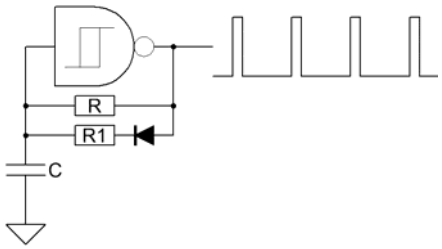

Figure 8. Pulse generator using a Schmitt input gate.

Another useful circuit using a Schmitt input gate is a simple edge-triggered monostable. The basic circuit, shown in Figure 9, consists, again, of simply a resistor and a capacitor. With capacitors larger than 10 nF, it is advisable to have a diode to minimize the current in the gate's input protection diode during the second transition (the end of the input pulse), but with smaller capacitors the gate protection diode should handle this current quite safely.

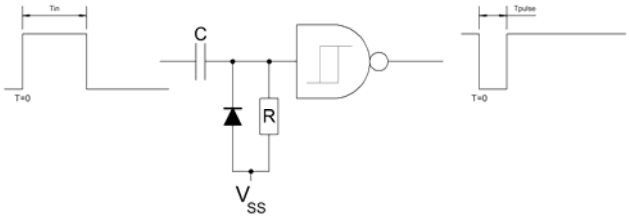

Figure 9. Edge triggered monostable pulse generator using a Schmitt input gate

The monostable shown delivers a negative output pulse, of duration 0.5 to 2 times RC (I *said* these things were not very accurate), on a positive-going input (0 to 1 transition). It is important that the input pulse duration T_{in} should be greater than the output pulse duration T_{pulse}, as if T_{in} goes negative before the output pulse is complete it will be prematurely truncated. If the diode is reversed and the diode and resistor are connected to V_{DD}, the monostable will trigger on a negative-going edge (1 to 0 transition) and deliver a positive output pulse.

By reversing the positions of the resistor and the capacitor in the circuit above, a Schmitt input may be used as a delay circuit. With the addition of a diode (and perhaps a second resistor), different delays may be obtained on rising and falling edges. This circuit is shown in Figure 10.

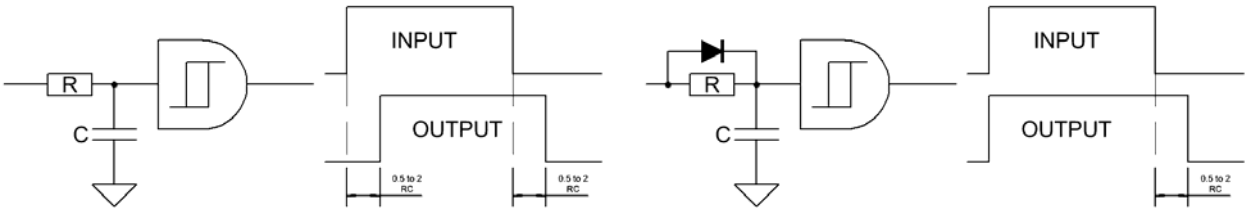

Figure 10. Schmitt input gates in delay circuits.

As before, the delay is in the range 0.5 to 2 RC. The input capacitance of a 4000 Series gate is approximately 7.5 pF, and with the addition of circuit board capacitances may well be 10 pF. If a 1 MΩ resistor is chosen, this will give a 10 µs delay without the necessity of an additional capacitor.

The second circuit in Figure 10 shows a diode in parallel with the resistor. This eliminates the delay on the rising edge (0 to 1 transition). If the diode were to be reversed, the falling edge transition would be the one to be undelayed. An extra resistor in series with the diode would allow different delays to be chosen for the rising and falling edges.

Expanding 4000 Series Inputs

4000 Series logic gates are available with up to eight inputs (the 4068 and 4078 are, as we have already noted, respectively 8-input NAND and 8-input NOR gates). The 4048 is an 8-input gate that can be reconfigured by logic control to accomplish AND, NAND, OR, or NOR functions, and can be expanded, with additional 4048s, to 16, 24, or more inputs. For many applications this is overly complex, however, as any 4000 Series input may be expanded by the use of a resistor and two or more diodes as shown in Figure 11.

The circuit in Figure 11A is an OR gate—if any one of the N inputs is at logic 1, the gate output will also be at logic 1. With the NAND gate in Figure 11B, the output will be at logic 1 only if ALL the inputs are at logic 1. Note that the resistor in the NOR gate is connected to V_{SS} while the resistor in the NAND gate goes to V_{DD}. It is not possible to combine NAND and NOR functions in one gate without additional diodes and resistors. While this may be possible with higher supply voltages, it should not be attempted with supplies under about 8 V because of the loss of noise immunity due to diode voltage drops.

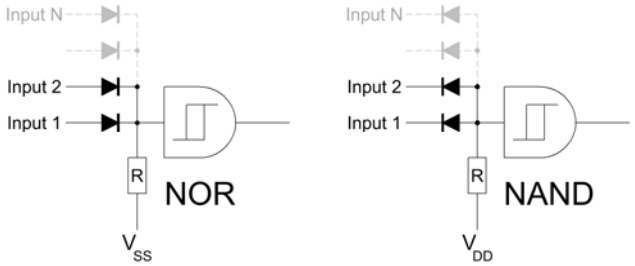

Figure 11. Diode/resistor gate expansion.

The resistor R may be quite large, but when no diode is conducting, the input capacitance of the gate (and any stray capacitance) can only discharge through the resistor, creating a delay circuit similar to the one in Figure 10. If R = 1 MΩ, for example, we can expect a delay of around 10 μs on this transition (but not on the one where a diode conducts). R must be chosen to give an acceptable delay, but if it is too low it may sink an unacceptable current while any diode is conducting. Engineering always involves trade-offs.

Useful functions in 4000 Series

The 4000 Series contains a wide range of logic: gates, flip-flops and latches, counters, shift registers, decoders, display drivers, ALUs and much else. Consult table 1 for a complete list of what is available.

While I do not wish to discuss the range of available functions in any detail, since this is an article on logic associated with analog circuitry, I do wish to discuss three functions: multiplexers, crystal oscillators and phase-locked loops (PLLs).

Multiplexers

The 4000 Series contains a number of CMOS multiplexers that are more than adequate for many applications, but they use quite old technology and do not have the performance of more modern types. In particular, their on-resistance and capacitance are both quite high, making them less suitable for high-speed and high-precision applications, and they are more vulnerable to destructive latch-up than more modern designs. If you do use these multiplexers (they are cheap and interface easily with other 4000 Series devices), it is very important to ensure that none of their terminals is ever at a potential more than 300 mV above the V_{DD} pin or 300 mV below the V_{SS} pin—even when they are powered off, and especially during power-up. Failure to observe this precaution may result in a hardware latch-up which can short-circuit the power supply through the multiplexer chip and destroy it in a few ms.

Latch-up may also result from local electrostatic fields. No terminal of a CMOS multiplexer or switch should ever be left open-circuit and unconnected—even the inputs and outputs of unused channels. Quite small electrostatic fields on such terminals may trigger latch-up, but even if this does not happen they may inject minority carriers into the CMOS substrate. Having a relatively long lifetime, these carriers may migrate through the substrate and corrupt analog signals in an active channel. All unused terminals must be connected to ground, a power supply, or a potential at or between V_{DD} and V_{SS}.

Crystal Oscillators

It is quite common to use logic gates as crystal oscillators. Several 4000 Series devices contain circuitry designed for use as crystal oscillators—in particular the 4060 14-stage binary ripple counter. Such oscillators are convenient, inexpensive, and quite stable for timing applications. But their phase noise, and the phase noise of *any* logic gate used as an oscillator of any sort, is considerably worse than the phase noise of an oscillator built with ICs optimized for low phase noise, or simply with low noise discrete semiconductors. 4000

Series devices should not be used in sampling or reconstruction systems where system resolution is affected by clock jitter.[4]

Phase-Locked Loops

The 4046 contains a voltage-controlled oscillator (VCO) and two phase comparators—a type-1 phase comparator and a type-2 phase/frequency comparator. It may be used for frequency synthesis, clock regeneration, and FM demodulation. As an example, we shall consider its use in a frequency-to-voltage converter (FVC).

A phase-locked loop (PLL) is a servo system that acts to minimize the phase error between a voltage-controlled oscillator (VCO) and an input signal as shown in Figure 12. A VCO is an oscillator whose output frequency is a monotonic function of a control voltage; a voltage-to-frequency converter (VFC) is a special case of a VCO with a linear voltage/frequency characteristic.

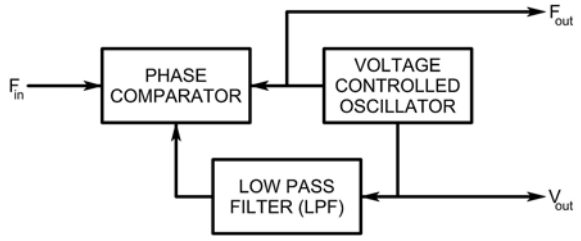

Figure 12. PLL Frequency-to-Voltage Converter

Phase-locked loops are the subject of large books and much argument and are far too complex to deal with exhaustively in a few pages. For the purposes of FVC demodulation, however, we can consider a type-2 PLL using the 4046.

If pin 13 of the 4046 (the output of the type-2 phase detector) is fed through a resistor, R, to a capacitor, C (which may have a damping resistor, Rd, in series with it), and the voltage on the capacitor is buffered to drive a VFC with an output frequency, F, for a control voltage, V, then the following equations apply:

Phase Detector Gain

$$K_d = V_{dd}/(4\pi R) \text{ amperes/radian}$$

VFC Gain

$$K_o = 2\pi F/V \text{ radians/volt-sec}$$

Natural Frequency

$$\omega_n = \sqrt{\mathbf{K_o K_d / C}}$$

Damping Factor

$$\xi = \mathbf{R_d}\sqrt{\mathbf{C K_o K_d / 2}}$$

From these equations and the VFC equation, we may derive values for R, R_d, and C for a PLL that has independent control of gain, ripple, and settling time. We can build our FVC using the VCO of the 4046, but it is not very linear.

A more linear device would be a better choice. The Analog Devices AD654 is much more linear and will work over most of the 4000 Series supply range (from 5 V to 18 V). An FVC using the 4046 and the AD654 is shown in Figure 13. The AD654 stops oscillating with analog inputs above V_{DD} – 3.5 V, allowing noise transients to cause (nondestructive) system

latch-up. The clamp in the circuit prevents the control voltage from exceeding this level and thus stops this from happening.

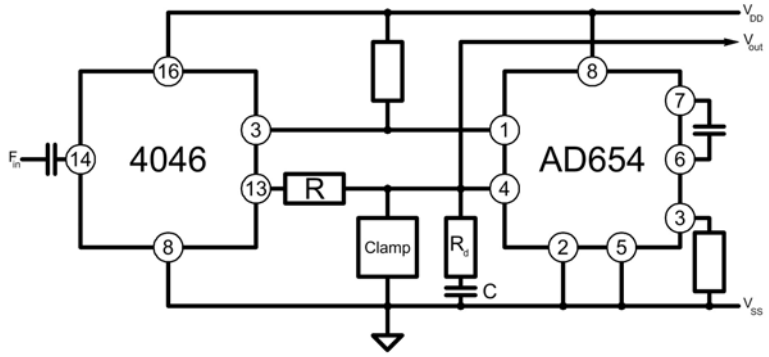

Figure 13. FVC using the 4046 and the AD654.

4000 Series Interfaces to Other Logic Families

4000 Series devices operating at 3.3 V or 5 V can readily interface with other CMOS families operating from the same supplies, but will not interface with 5-V TTL because the input voltage threshold of the 4000 Series operating with a 5-V supply is higher than the output high voltage of TTL. When operated at higher voltages they can neither receive signals from, nor send signals to, 3.3-V or 5-V logic families.[5]

Sending signals from low-voltage logic to 4000 Series operating at higher voltages is quite simple. Three 4000 Series devices are designed to interface low-voltage logic outputs with high-voltage logic inputs: the 40109, the 4104, and the 4504. They are simply connected as buffers with one of their supplies tied to the 5-V logic supply and the other to the 4000 Series supply. But only one of them will allow the high-voltage 4000 Series output to drive a low voltage CMOS input, and that one will drive only 5-V CMOS, not 3-V.

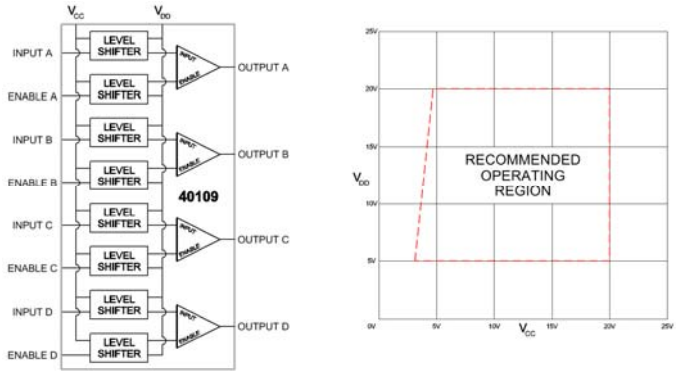

Figure 14. The 40109 quad up/down logic level shifter with individual tri-state enable.

The 40109 is versatile, operating with an input logic supply between 3 V and 20 V and an output supply between 5 V and 20 V. Not only can the output be lower than the input, but there are no supply sequence problems as any input and any supply may be applied in the absence of any of the others. There are only four buffers per package, however, but they have individual enable pins that allow the outputs to go high impedance [tri-state].

Fortunately, a simple interface technique allows up and down shift over a very large range of supply voltages: a discrete NMOS resistor/transistor logic (RTL) inverter connected as in Figure 15. If it is possible to obtain a discrete NMOS transistor with a well-defined threshold voltage of 40% of the CMOS supply voltage, with a tolerance of no more than ±20% (i.e., its threshold is between 32% and 48% of the CMOS supply voltage), then R_1 and R_2 are unnecessary and the logic signal may be connected directly to the NMOS gate. Otherwise R_1

and R_2 must be chosen so that if V_1 is 40% of the CMOS supply and V_t is the NMOS threshold voltage, then $V_t = V_1R_2/R_1+R_2$.

Obviously the time constant introduced by the resistors and the gate capacitance, C_g, is

$$C_g \Big/ \left(1/R_1 + 1/R_2 \right)$$

so R1 and R2 must be chosen to be as large as possible to avoid loading the CMOS driving them but not so large as to introduce too much propagation delay.

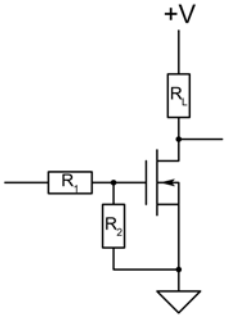

Figure 15. Basic NMOS RTL Inverter.

The load resistor, R_L, is likewise chosen to be large enough to draw as little current as possible while the time constant R_LC_L, where C_L is load capacitance, is acceptably short. In a slow system the resistors may be very large and delays quite long, but in such a case it is best to drive a Schmitt input with the slow logic edge.

Conclusion

High-performance analog systems often need small amounts of logic for control or other purposes. It is helpful if such logic can share the analog power supplies, which may not be compatible with 5-V or 3-V logic systems, without imposing a large additional power drain or corrupting the system with logic noise.

The old, slow 4000 Series CMOS logic is ideally suited to such tasks. This note has discussed some of the issues that may be encountered when it is so used.

Appendix
Table 1. Series 4000 Logic

4000	Dual 3-input NOR gate + 1 Inverter	4060	14-stage binary ripple counter and oscillator	4539	Dual 4-input multiplexer
4001	Quad 2-input NOR gate	4062	Logic dual 3 majority gate	4541	Programmable Timer
4002	Dual 4-input NOR gate	4063	4-bit Digital comparator	4543	BCD to 7-Segment Latch/Decoder/Driver with Phase Input
4006	18 stage Shift register	4066	Quad Analog switch (Low "ON" Resistance)	4553	3-digit BCD counter
4007	Dual Complementary Pair Plus Inverter	4067	16-channel analogue multiplexer/demultiplexer (1-of-16 switch)	4555	Dual 1-of-4 decoder/demultiplexer HIGH output
4008	4 bit adder	4068	8-input NAND gate	4556	Dual 1-of-4 decoder/demultiplexer LOW output
4009	Hex inverting buffer	4069	Hex inverter	4557	1-to-64 Bit Variable Length Shift Register
4010	Hex non-inverting buffer	4070	Quad XOR gate	4560	NBCD adder
4011	Buffered Quad 2-Input NAND gate	4071	Quad 2-input OR gate	4566	Industrial time-base generator

4012	Dual 4-input NAND gate	4072	Dual 4-input OR gate	4572	Hex gate : quad NOT, single NAND, single NOR
4013	Dual D-type flip-flop	4073	Triple 3-input AND gate	4584	Hex schmitt trigger
4014	8-stage shift register	4075	Triple 3-input OR gate	4585	4-bit Digital comparator
4015	Dual 4-stage shift register	4076	Quad D-type register with tristate outputs	4724	8-bit addressable latch
4016	Quad bilateral switch	4077	Quad 2-input XNOR gate	4750	Frequency synthesizer
4017	Divide-by-10 counter (5-stage Johnson counter)	4078	8-input NOR gate	4751	Universal divider
4018	Presettable divide-by-n counter	4081	Quad 2-input AND gate	4794	8-Stage Shift-and-Store Register LED Driver
4019	Quad AND-OR Select Gate	4082	Dual 4-input AND gate	4894	12-Stage Shift-and-Store Register LED Driver
4020	14-stage binary counter	4085	Dual 2-wide, 2-input AND/OR invert (AOI)	4938	Dual Retriggerable Precision Monostable Multivibrator with Reset
4021	8-bit static shift register	4086	Expandable 4-wide, 2-input AND/OR invert (AOI)	4952	8-channel analog multiplexer/demultiplexer
4022	Divide-by-8 counter (4-stage Johnson counter)	4089	Binary rate multiplier	40098	3-state hex inverting buffer
4023	Triple 3-input NAND gate	4093	Quad 2-input Schmitt trigger NAND gate	40100	32-bit left/right Shift Register
4024	7-Stage Binary Ripple Counter	4094	8-stage shift-and-store bus	40101	9-bit Parity Generator/Checker
4025	Triple 3-input NOR gate	4095	Gated "J-K" (non-inverting)	40102	Presettable 2-decade BCD down counter
4026	BCD counter with decoded 7-segment output	4096	Gated "J-K" (inverting and non-inverting)	40103	Presettable 8-bit binary down counter
4027	Dual JK flip-flop	4097	Differential 8-channel analog multiplexer/demultiplexer	40104	4 bit bidirectional Parallel-in/Parallel-out PIPO Shift Register (tristate)
4028	BCD to decimal (1-of-10) decoder	4098	Dual one-shot monostable	40105	4-bit x 16 word Register
4029	Presettable up/down counter, binary or BCD-decade	4099	8-bit addressable latch	40106	Hex Inverting Schmitt-Trigger-(NOT gates)
4030	Quad XOR gate (replaced by 4070)	4104	Quad Low-to-High Voltage Translator with tristate outputs	40107	dual 2-input NAND buffer/driver
4031	64-Bit Static Shift Register	4502	Hex inverting buffer (tristate)	40108	4x4-bit (tristate) synchronous triple-port register file
4032	Triple serial adder	4503	Hex non-inverting buffer with tristate outputs	40109	level shifter
4033	BCD counter + 7-segment decoder w/ripple blank	4504	Hex voltage level shifter for TTL-to-CMOS or CMOS-to-CMOS operation	40110	Up/Down Counter-Latch-Decoder-Driver
4034	8-stage bidirectional parallel or serial input/parallel output	4508	Dual 4-bit latch with tristate outputs	40116	8-bit bidirectional CMOS-to-TTL level converter
4035	4-stage parallel-in/parallel-out (PIPO) with J-K input and true/complement output	4510	Presettable 4-bit BCD up/down counter	40117	Programmable dual 4-bit terminator
4038	Triple serial adder	4511	BCD to 7-segment latch/decoder/driver	40147	10-line to 4-line [BCD] priority encoder
4040	12-stage binary ripple counter	4512	8-input multiplexer (data selector) with tristate output	40160	Decade counter/asynchronous clear
4041	Quad true/complement buffer	4513	BCD to 7-segment latch/decoder/driver (4511 plus ripple blanking)	40161	Binary counter/asynchronous clear
4042	Quad D-type latch	4514	1-of-16 decoder/demultiplexer HIGH output	40162	4-bit synchronous decade counter with load, reset, and ripple carry output
4043	Quad NOR R/S latch	4515	1-of-16 decoder/demultiplexer LOW output	40163	4-bit synchronous binary counter with load, reset, and ripple carry output
4044	Quad NAND R/S (tristate output)	4516	Presettable 4-bit binary up/down counter	40174	Hex D-type flip-flop with reset; positive-edge trigger
4045	21-Stage Counter	4517	Dual 64-Bit Static Shift Register	40175	Quad D-type flip-flop with reset; positive-edge trigger
4046	PLL with VCO	4518	Dual BCD up counter	40181	4-bit 16-function arithmetic logic unit (ALU)
4047	Monostable/Astable Multivibrator	4519	Quad 2-input multiplexer (data selector)	40192	Presettable 4-bit BCD up/down counter
4048	Multifunctional expandable 8-input (tristate output)	4520	Dual 4-bit binary up counter	40193	Presettable 4-bit binary up/down counter

4049	Hex inverter/buffer (NOT gate)	4521	24-stage frequency divider	40194	4-bit universal bidirectional with asynchronous master reset
4050	Hex buffer/converter (non-inverting)	4522	Programmable BCD divide-by-N counter	40195	4-bit universal shift register
4051	Analogue multiplexer/demultiplexer (1-of-8 switch)	4526	Programmable 4-bit binary down counter	40208	4 × 4-bit (tristate) synchronous triple-port register file
4052	Analogue multiplexer/demultiplexer (Dual 1-of-4 switch)	4527	BCD rate multiplier	40240	Buffer/Line driver; Inverting (tristate)
4053	Analogue multiplexer/demultiplexer (Triple 1-of-2 switch)	4528	Dual Retriggerable Monostable Multivibrator with Reset	40244	Buffer/Line Driver; Non-Inverting (tristate)
4054	7-segment decoder/LCD driver	4529	Dual 4-channel analog	40245	Octuple bus transceiver; (tristate) outputs ,
4055	BCD-to-7-segment decoder/driver with "display-frequency" output	4532	8-bit priority encoder	40257	Quad 2-Line-to-1-Line Data Selector/Multiplexer (tristate)
4056	BCD-to-7-segment decoder/driver with strobed latch function	4536	Programmable Timer	40373	Octal D-Type Transparent latch (tristate)
4059	Programmable divide-by-N counter	4538	Dual Retriggerable Precision Monostable Multivibrator	40374	Octal D-type flip-flop; positive-edge trigger (tristate)

[1] "Read the Friendly Data Sheet" – See RAQ # 4 and its links – http://www.analog.com/en/analog-to-digital-converters/products/rarely-asked-questions/RAQ_caveat/fca.html

[2] http://ics.nxp.com/support/documents/logic/pdf/family.hef4000.specification.pdf (Note that at the time this document was written NXP was Philips Semiconductors).

[3] Named for Otto H Schmitt (1913-1998) who invented the original Schmitt Trigger circuit in 1934 as a postgraduate student at Washington University, St. Louis, MO as a direct result of his study of neural impulse propagation in squid nerves.

[4] For more details on the effects of phase noise in sampling and reconstruction systems see RAQ # 6 and its links - http://www.analog.com/en/analog-to-digital-converters/products/rarely-asked-questions/RAQ_tickTock/fca.html

[5] For more details on fast low voltage logic interfaces see Analog Devices Application Note MT-098 http://www.analog.com/static/imported-files/tutorials/MT-098.pdf