ANALOG DEVICES
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LTspice User Guide – AD8460 Model

Tim Green
Principal Engineer, Product Applications
PAG (Precision Amplifiers Group)
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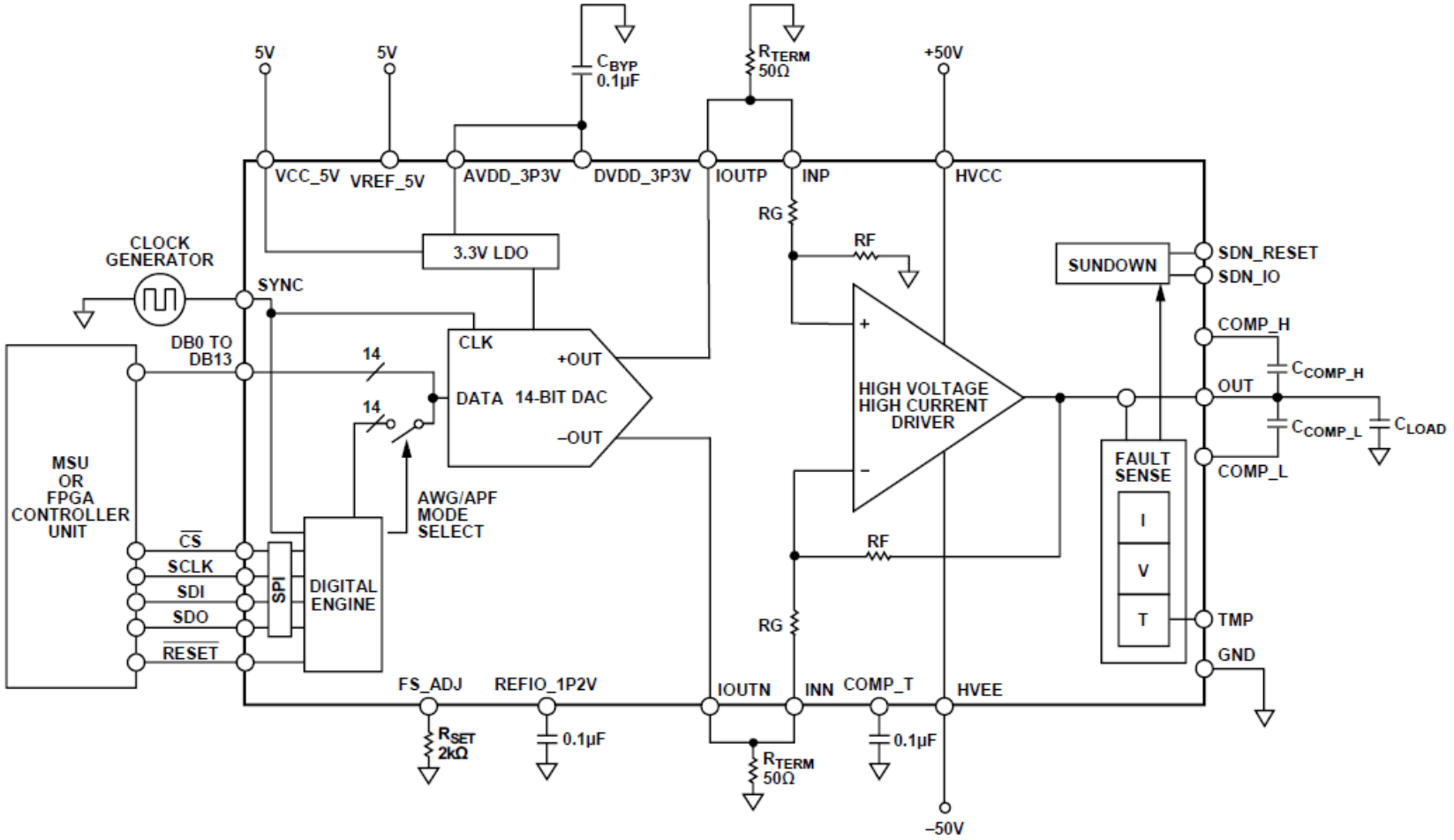

Figure 1. Simplified Functional Block Diagram

Overview

- All LTspice schematics referenced in this presentation are available in the zip folder *AD8460 LTspice.zip*
- Keep all files in the same folder and run the LTspice ".asc" files out of that respective folder, if you want post-simulation plots to be prepopulated with key curves.
- Where LTspice schematics are used in this presentation, the corresponding LTspice ".asc" file is noted on the schematic figure, in a red box.
- Many of the Fault Detect Circuit Tests are run with Maximum Timestep=10ns, so when zooming in to measure 400ns type delays, some accuracy can be achieved. For most simulations, by leaving Maximum Timestep blank, will result in faster simulation times.
- The real IC uses 5000+ transistors, which yield the resultant detailed behaviors and plots, documented in the datasheet.
- The AD8460 Macromodel was designed to best model the cases listed here, while providing other case results as close to the datasheet performances as design compromises would allow for convergence, complexity, and simulation time trade-offs.
  - Cload=1nF, Ccomp=0pF
  - Cload=22nF, Ccomp=10pF
  - Cload=47nF, Ccomp = 20pF

Model Features

AD8460 LTspice Macromodel versus Real IC		
Function	**Real IC**	**LTspice Model**
Digital Interface	SPI/Parallel Interface	Not Modeled
Clock Generator Input	SYNC pin	Not Modeled
Arbitrary Waveform Generator Mode	AWG Mode	Not Modeled
Arbitrary Pattern Generation Mode	APG Mode	Not Modeled
Thermal Monitor	TMP pin	Not Modeled. No OverTemperature Shutdown.
Thermal Monitor Comp	COMP_T pin	Not Modeled
DAC	14Bit DAC with INL, DNL	Not Modeled. Ideal DAC as Vdac Voltage scaled for 0 to Full-scale Current Out.
Temperature Effects	Drifts, Gain Errors, etc.	Not Modeled. 25C Typical Specs only.
Fault Detect Thresholds	Register Programmable	External Analog Voltage Programmable
Fault Detect Alarms	Register Read, Latched/Real Time	External Output Pins: 1=Fault, 0=No Fault, Not Latched, Real Time only
SDN_IO Function	Fault Detect Delay/Override	Fault Detect Delay/Override
SDN_RESET	Hardware Reset pin	Hardware Reset pin
Adjustable Iq	Register Programmable	Fixed at Iq=22.5mA
DAC FS Adjust	Typical Datasheet Specs	Typical Datasheet Specs
DAC Reference	Typical Datasheet Specs	Typical Datasheet Specs
Output Offset Voltage	Typical Datasheet Specs	Typical Datasheet Specs
Power Op Amp Zout Enabled/Disabled	Typical Datasheet Curves	Typical Datasheet Curves
Power Op Amp Iout versus Vout	Typical Datasheet Curves	Typical Datasheet Curves
Power Op Amp PSRR over Frequency	Typical Datasheet Curves	Typical Datasheet Curves
Power Op Amp CMRR over Frequency	Typical Datasheet Curves	Typical Datasheet Curves
Power Op Amp Vnoise	Typical Datasheet Curves	Typical Datasheet Curves
Power Op Amp Inoise	Typical Datasheet Curves	Typical Datasheet Curves
Harmonic Distortion	Typical Datasheet Curves	Not Modeled
Large Signal/Small Signal Behavior:	Typical Datasheet Curves:	Typical Datasheet Curves:
Slew Rate	CL=1nF, Ccomp=0pF	CL=1nF, Ccomp=0pF
Small Signal Bandwidth	CL=22nF, Ccomp=10pF	CL=22nF, Ccomp=10pF
Power Op Amp Overload Recovery Time	CL=47nF, Ccomp=20pF	CL=47nF, Ccomp=20pF
Power Op Amp Settling Time		
Internal Power Dissipation	Datasheet Information	Not Modeled- R&D for Future Model
Thermal Performance	Datasheet Information	Not Modeled- R&D for Future Model

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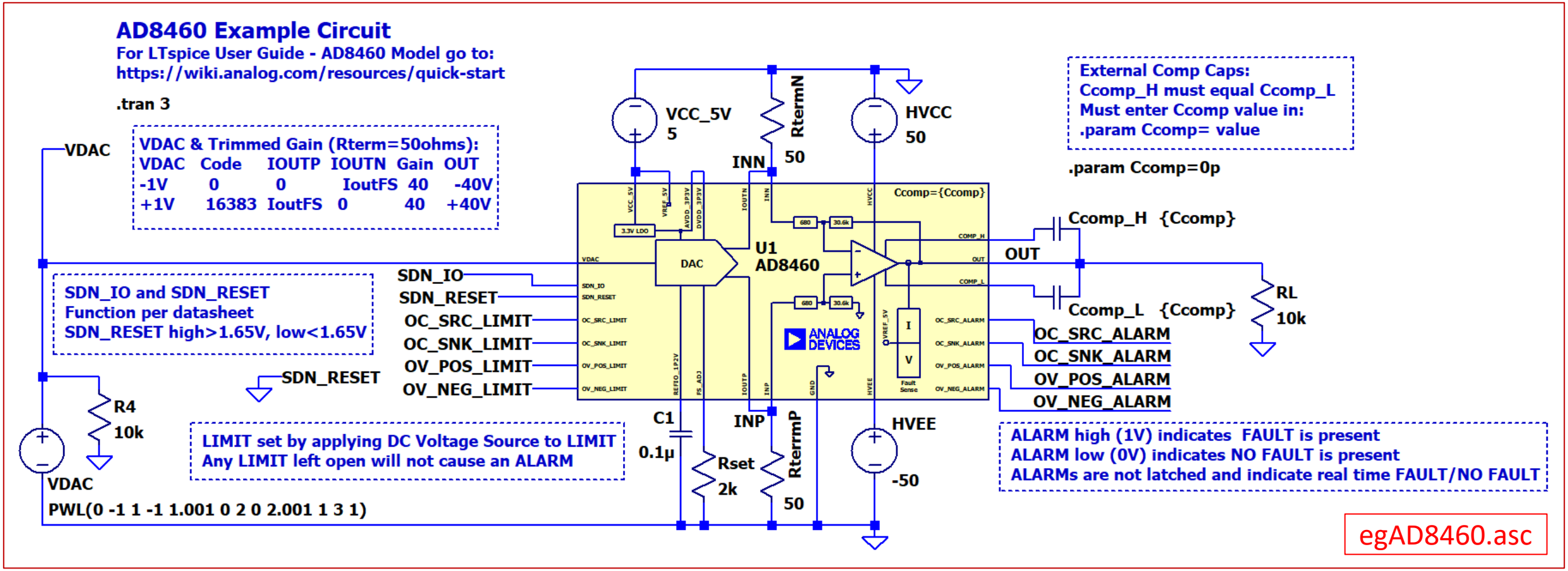
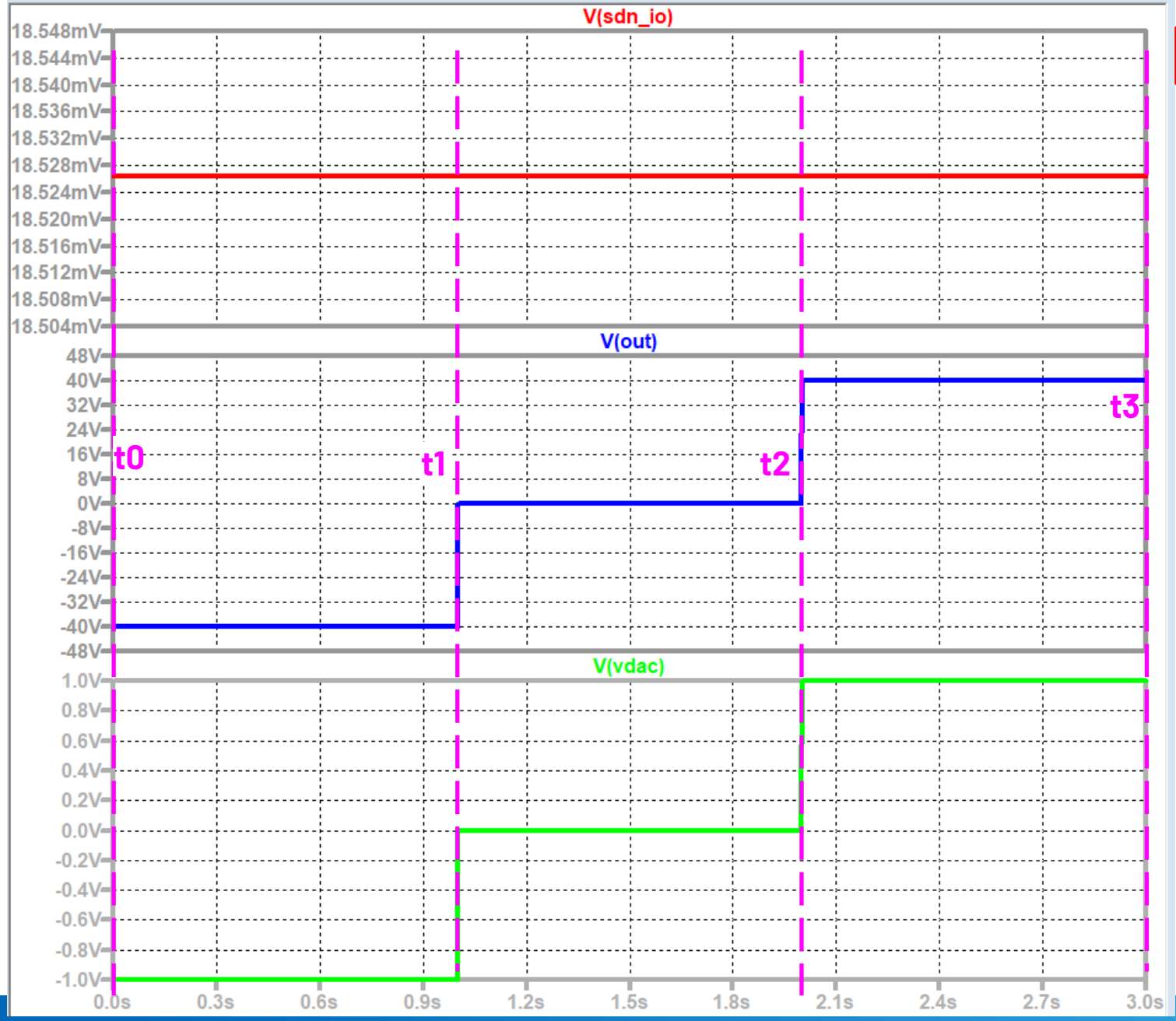
Example Circuit Checkout

Example Circuit Checkout



Example Circuit Checkout



t0-t3: No Faults created. V(SDN_IO) = 0V.

t0-t1: V(OUT) = VDAC *40 = -1V*40 = -40V
t1-t2: V(OUT) = VDAC *0 = 0V*40 = 0V
t2-t3: V(OUT) = VDAC *40 = +1V*40 = +40V

t0-t1: V(VDAC) = -1V = 0 LSB
t1-t2: V(VDAC) = 0V = 8191.5LSB
t2-t3: V(VDAC) = +1V = 16383 LSB

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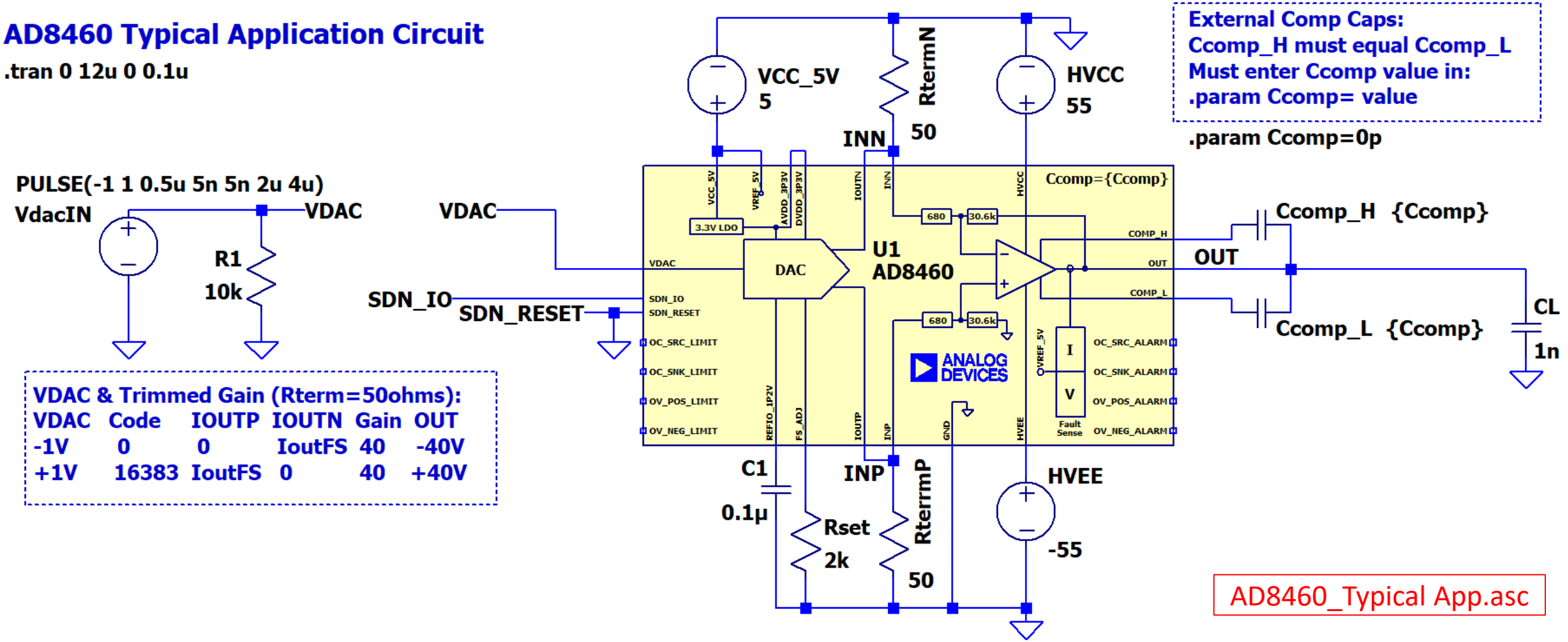
Typical Application Operation

Typical Application

AD8460 Typical Application Circuit

.tran 0 12u 0 0.1u

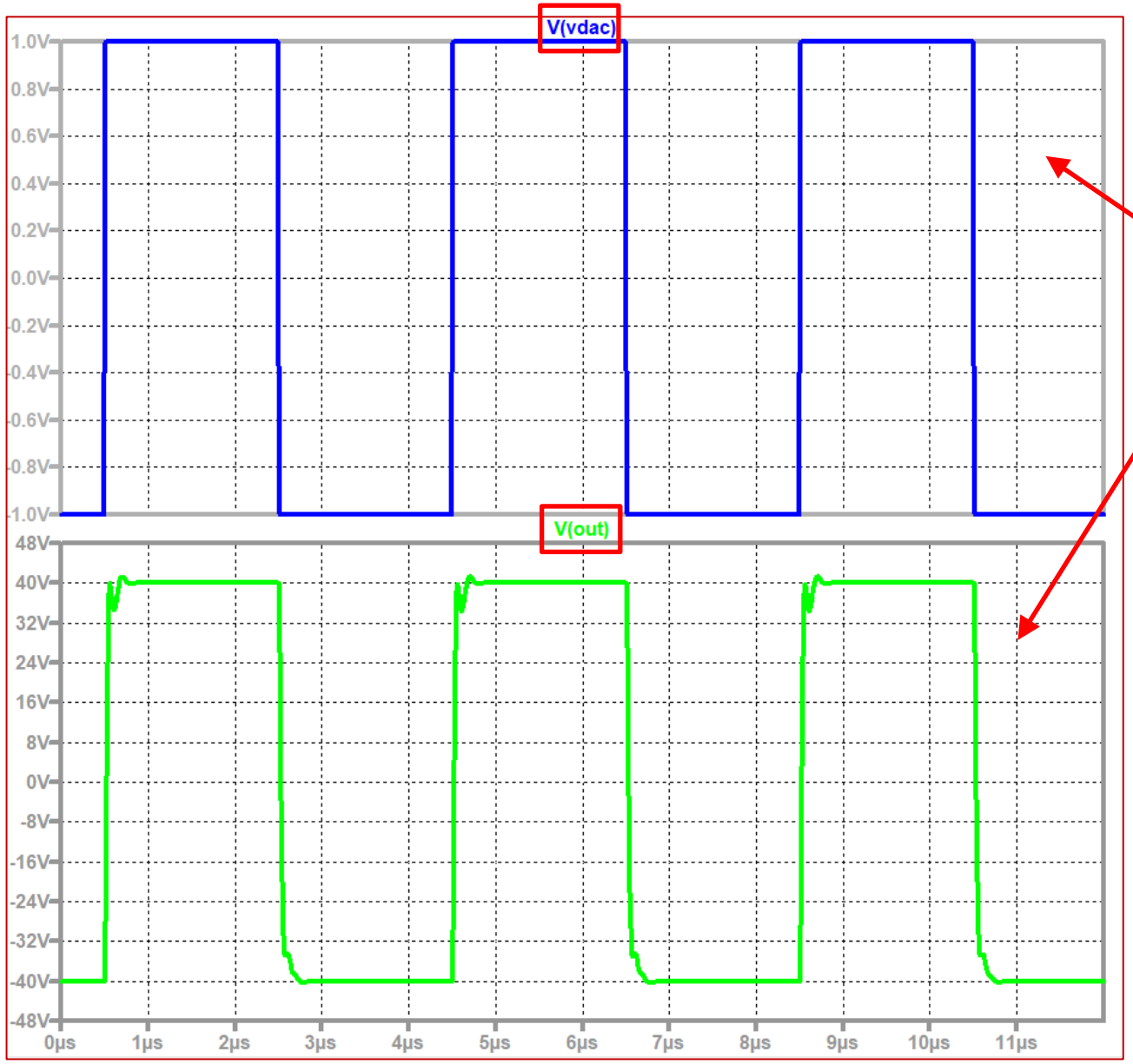


VDAC & Trimmed Gain (Rterm=50ohms):

VDAC	Code	IOUTP	IOUTN	Gain	OUT
-1V	0	0	IoutFS	40	-40V
+1V	16383	IoutFS	0	40	+40V

AD8460_Typical App.asc

Typical Application



For V(vdac) input = +/-1V, expect V(out) to be +/-40V.

Typical Application

SPECIFICATIONS

Table 1. Electrical Characteristics

(HVCC = + 50 V, HVEE = - 50 V, IHVCC = + 22.5 mA, IHVEE = - 22.5 mA, VCC_5V = + 5 V, VREF_5V = + 5 V, VREF_1P2V = + 1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_C = 30°C , Unless Otherwise Noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Small Signal Bandwidth	f_{3db}	V_{OUT} = 0.1 V p-p, T_J = 85°C. See *Figure 44*.		4.3		MHz
Large Signal Bandwidth[1]		V_{OUT} = 80 V p-p. See *Figure 41*.		1		MHz
Slew Rate, 20% to 80%	SR_{RISE}	V_{OUT} = 80 V p-p. See *Figure 8*.		2100		V/µs
	SR_{FALL}	V_{OUT} = 80 V p-p. See *Figure 9*.		1800		V/µs

Typical Application

Slew Rate Measure Points (20% to 80%)

VoutP=+40V

VoutM=-40V

Vout_step=VoutP-VoutM

Vout_step=+40V-(-40V)=80V

Vout_mid=(VoutP+VoutM)/2

Vout_mid=(+40V+(-40V))/2=0V

20% to 80% Slew Rate Measure = 60%(Vout_step)

SR_meas=0.6*80V=48V

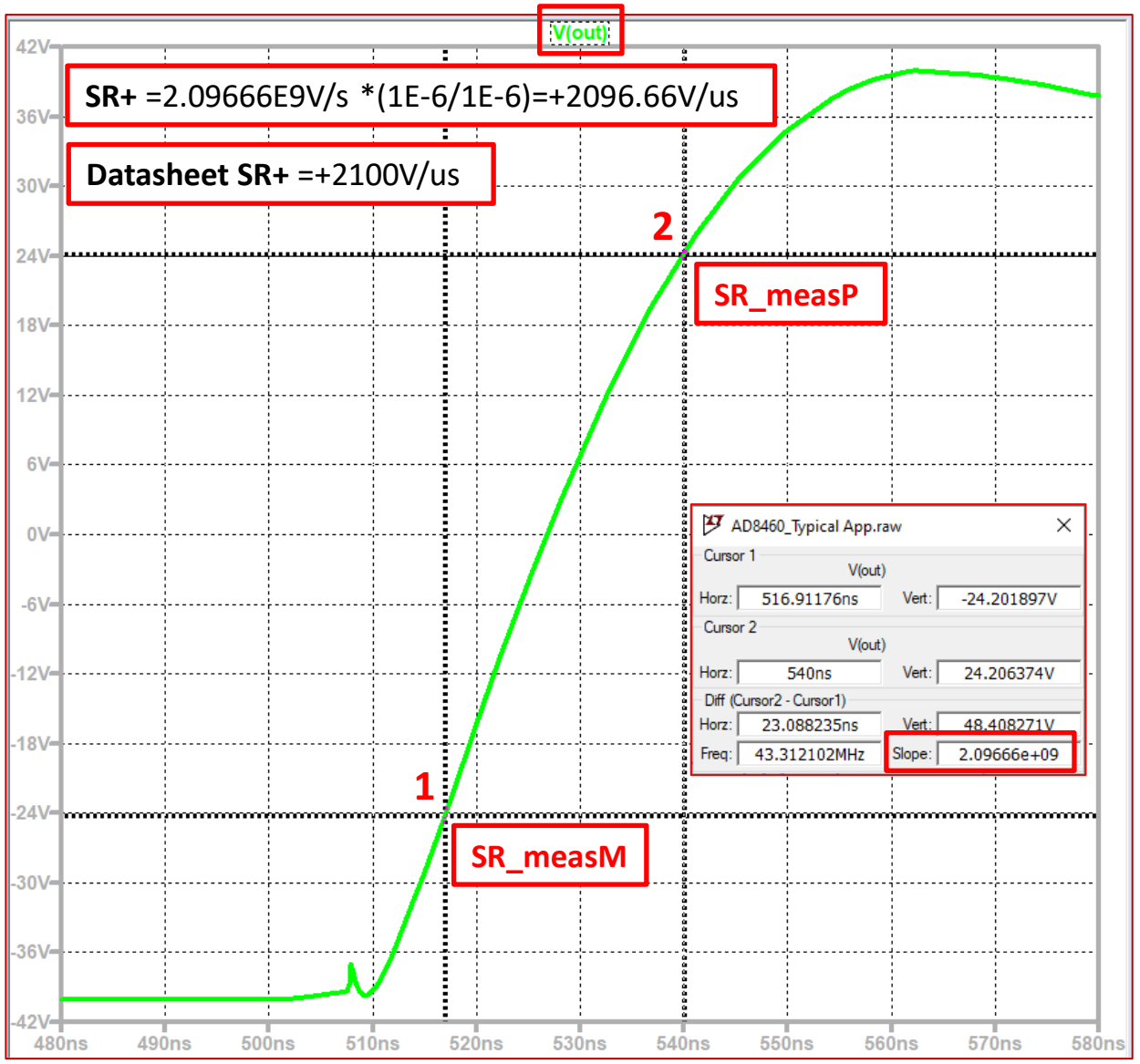
SR_measP=Vout_mid + 1/2(SR_meas)

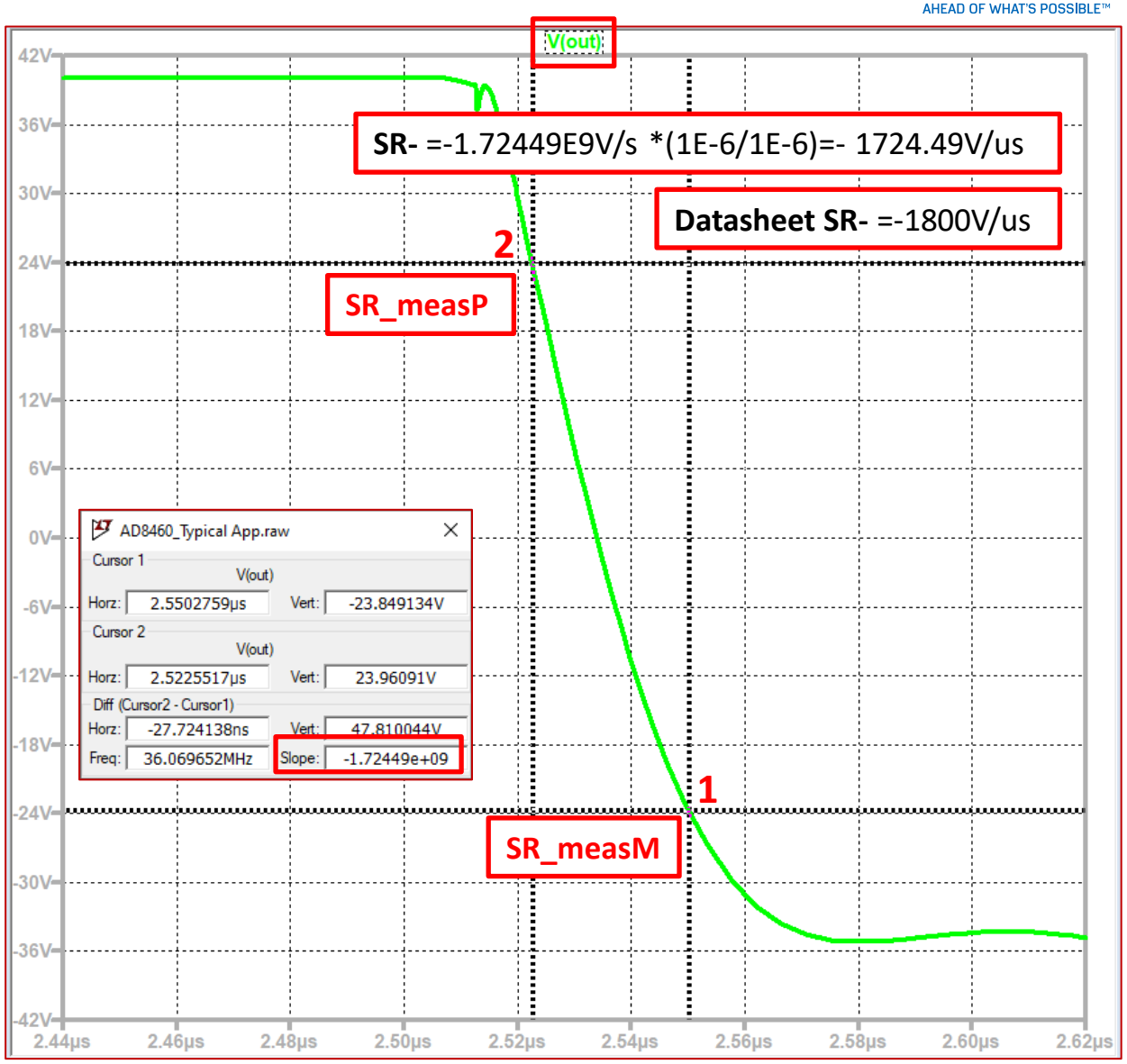
SR_measP=0+ 1/2(48V)=+24V

SR_measM=Vout_mid - 1/2(SR_meas)

SR_measM=0- 1/2(48V)=-24V

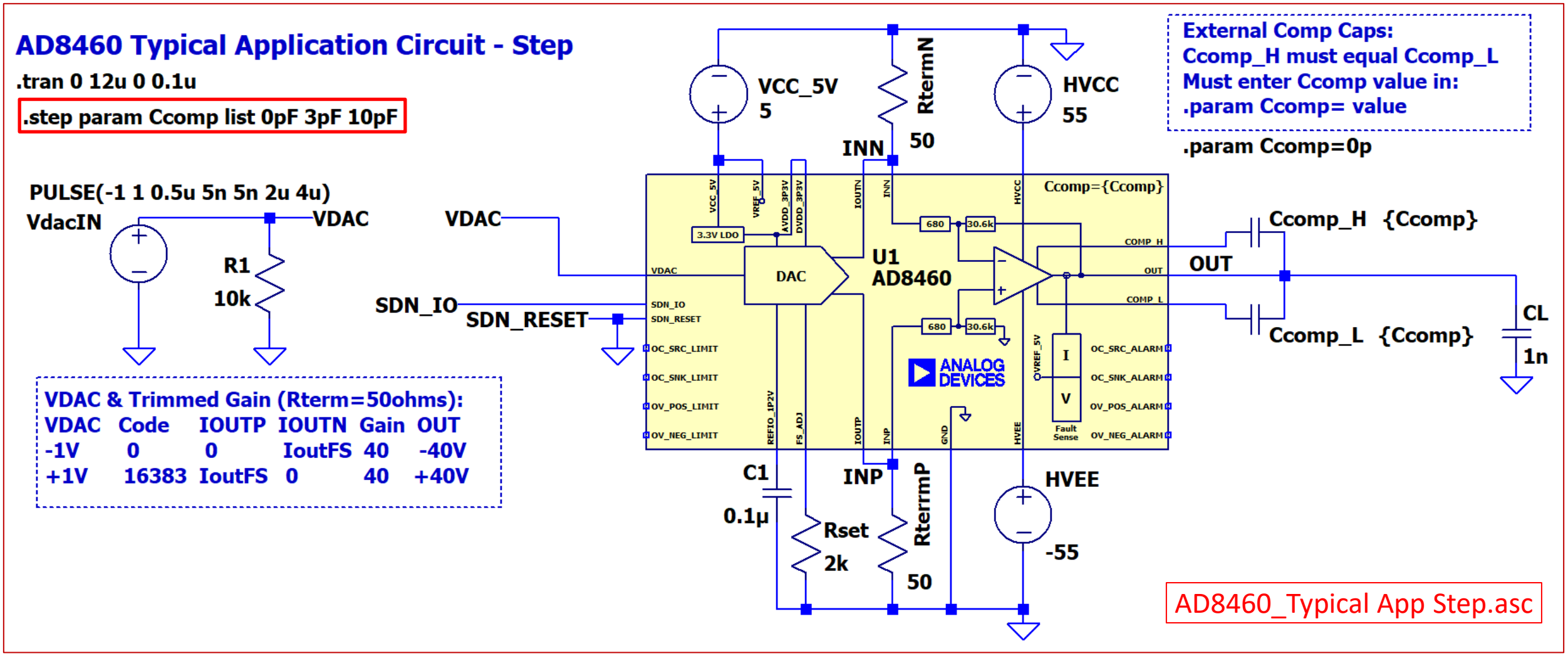
Typical Application





Typical Application

Use LTspice ".step" directive to change Ccomp to compare different values to datasheet curves for Large Signal Transient Responses.



Easy Compare Datasheet Curves to LTspice Plots

Step1: Use Windows “Snipping Tool” to copy and past Datasheet Curve into PowerPoint.

Step2: Run LTspice and in top “Toolbar” select “Window>Tile Vertically” on one monitor screen. This will give the best image resolution for copy and paste.

Step3: Scale X and Y axis in LTspice Plot Window to match Datasheet Curve axes.

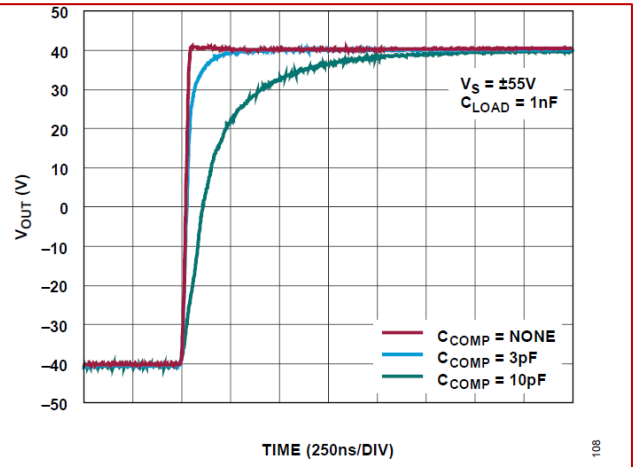
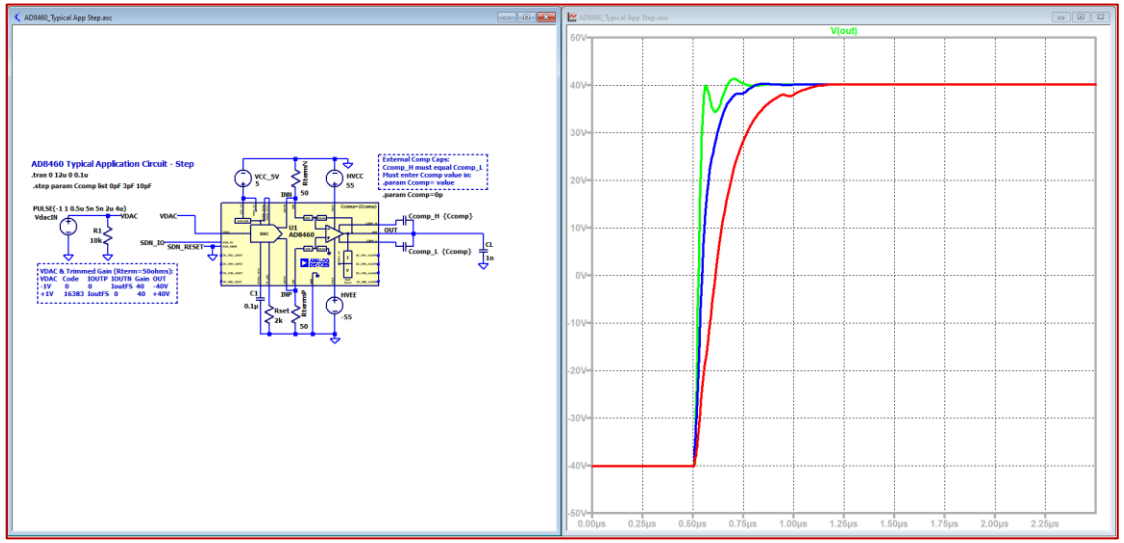
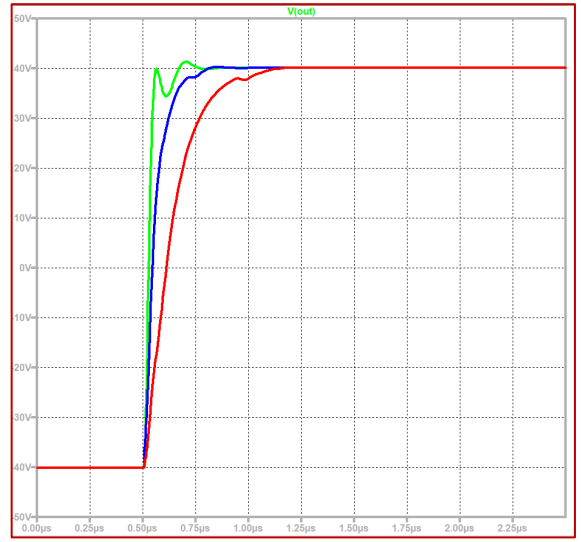


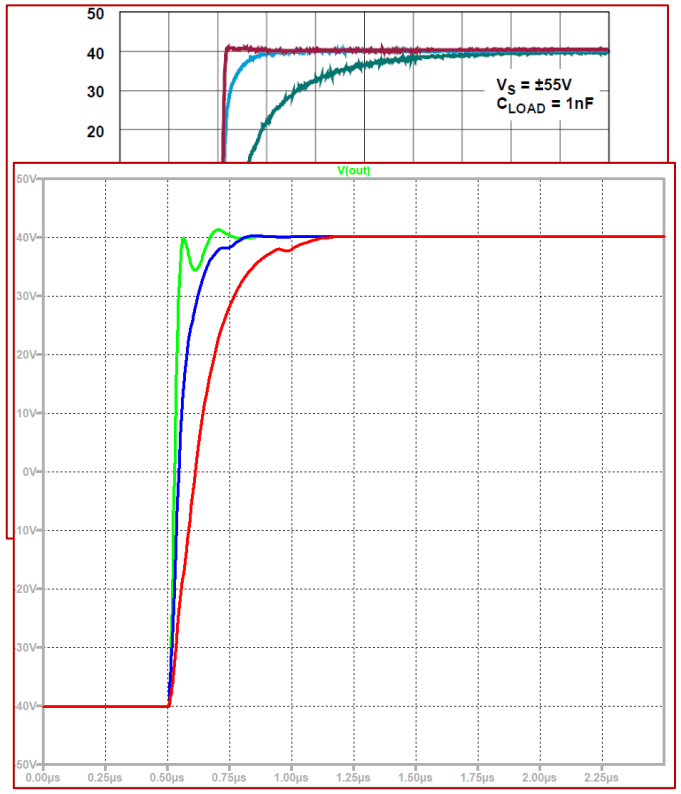
Figure 8. Large Signal Pulse Response vs. C_{LOAD} and C_{COMP}, Rising Edge, C_{LOAD} = 1 nF



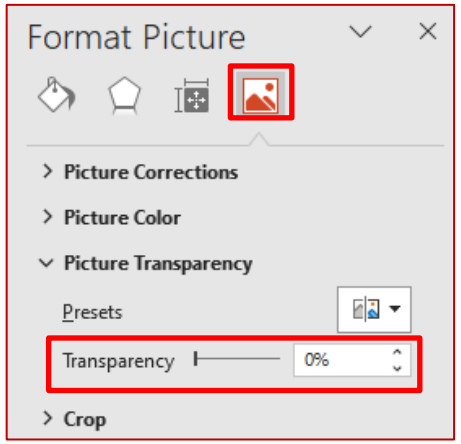


Easy Compare Datasheet Curves to LTspice Plots

Step4: Use Windows “Snipping Tool” to copy and paste LTspice PLot into PowerPoint. Bring the LTspice Plot to the front.



Step5: Now need to make the LTspice Plot ”transparent” so can see and compare the Datasheet Curve behind it. Select the LTspice Plot image, right click on it and select “Format Picture”. On the “Picture Transparency” slider adjust the slider to see both the Datasheet Curve and LTspice Plot. Here 35% was used. Place the LTspice Plot image, by selecting it and holding down left mouse button and moving to align with Datasheet Curve graticules as shown here. Can use up/down and left/right arrows on keyboard for fine movements. Use the dots on left/right side and top/bottom to resize the image.



Direct compare of Datasheet Curve to LTspice Plot

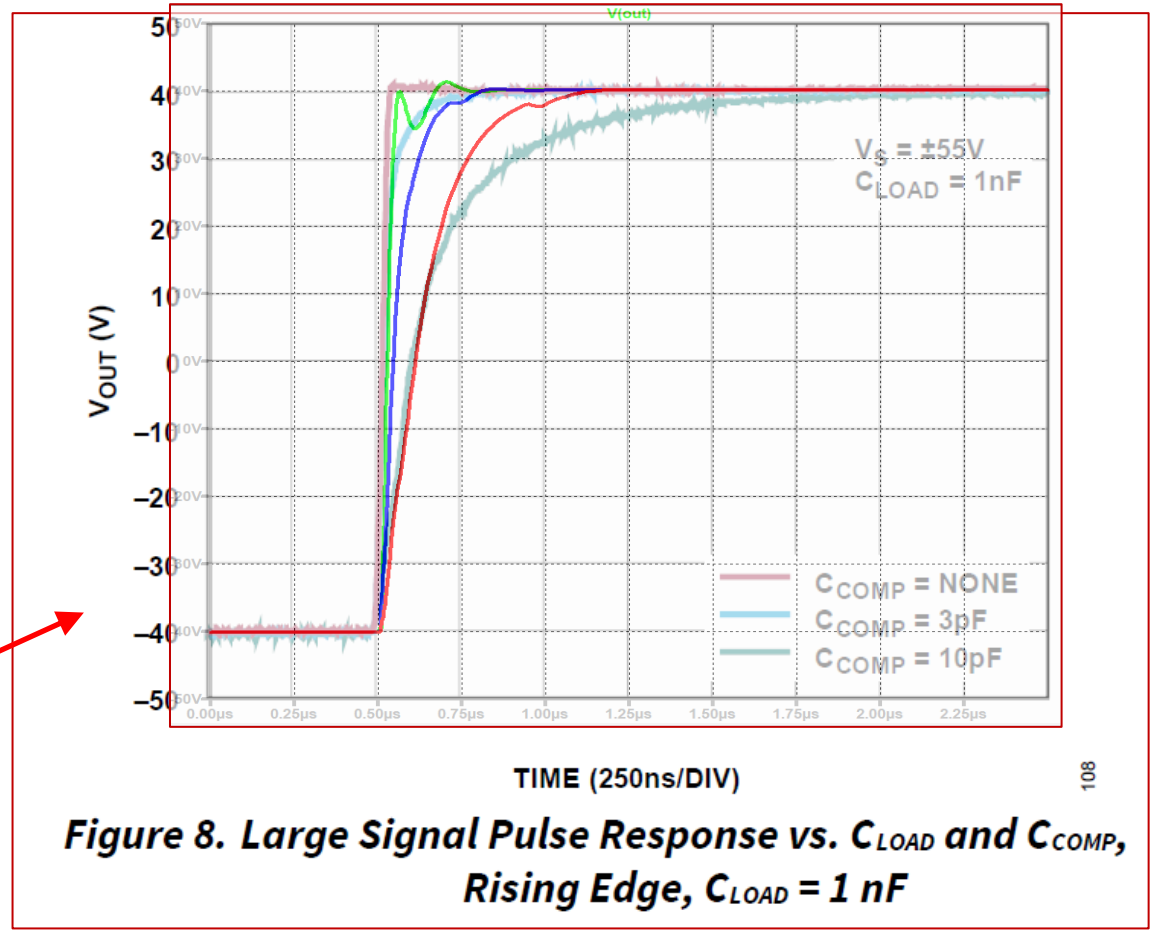


Figure 8. Large Signal Pulse Response vs. C_{LOAD} and C_{COMP}, Rising Edge, C_{LOAD} = 1 nF

Typical Application

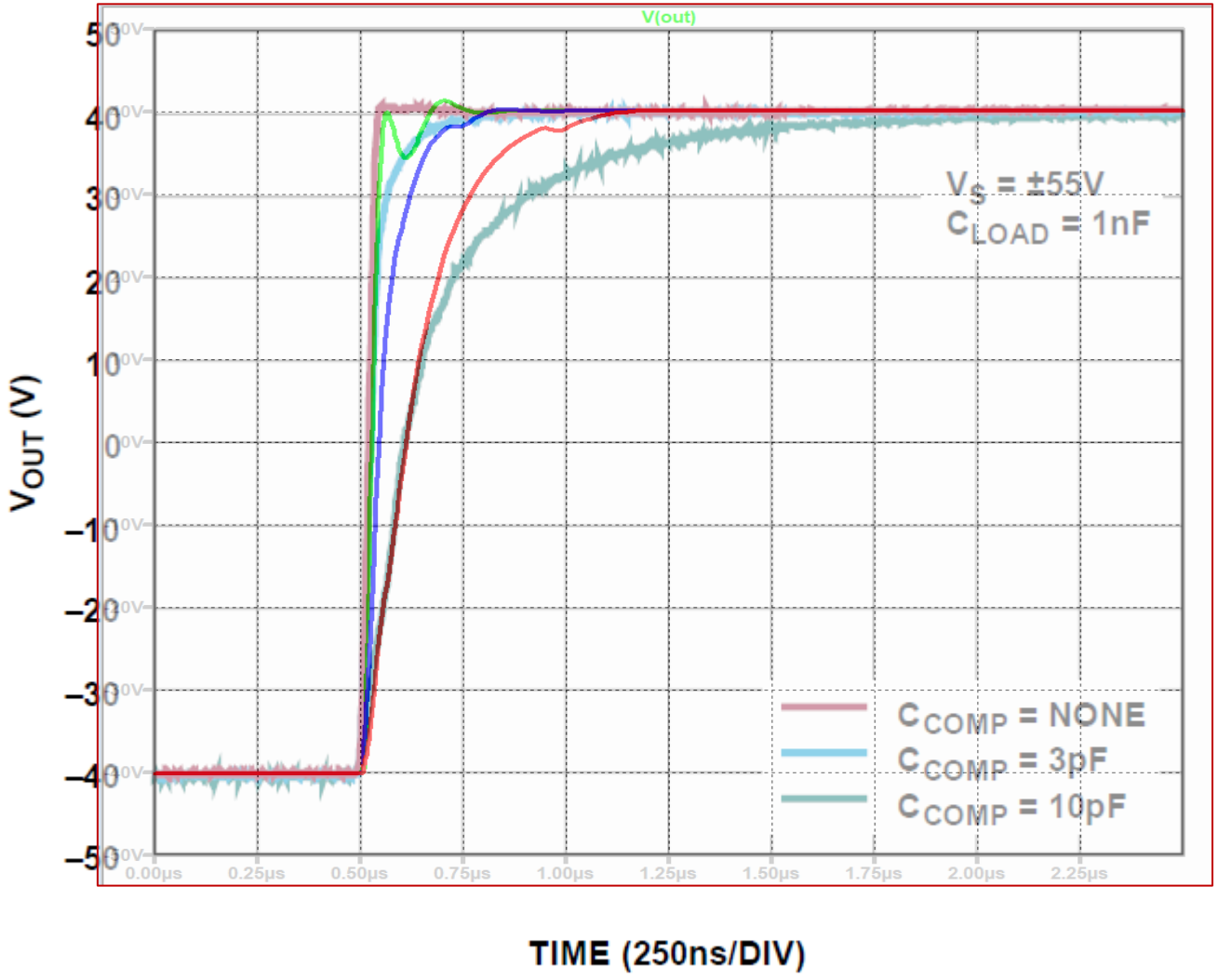


Figure 8. Large Signal Pulse Response vs. C_{LOAD} and C_{COMP}, Rising Edge, C_{LOAD} = 1 nF

- AD8460 LTspice Plot comparison with Datasheet Curves for Large Signal Pulse Response.
- Model was designed for Ccomp = NONE, Cload = 1nF.
- Step response changes with different Ccomp. Not an exact match, but a close trend to Real IC, given model trade-offs.

Typical Application

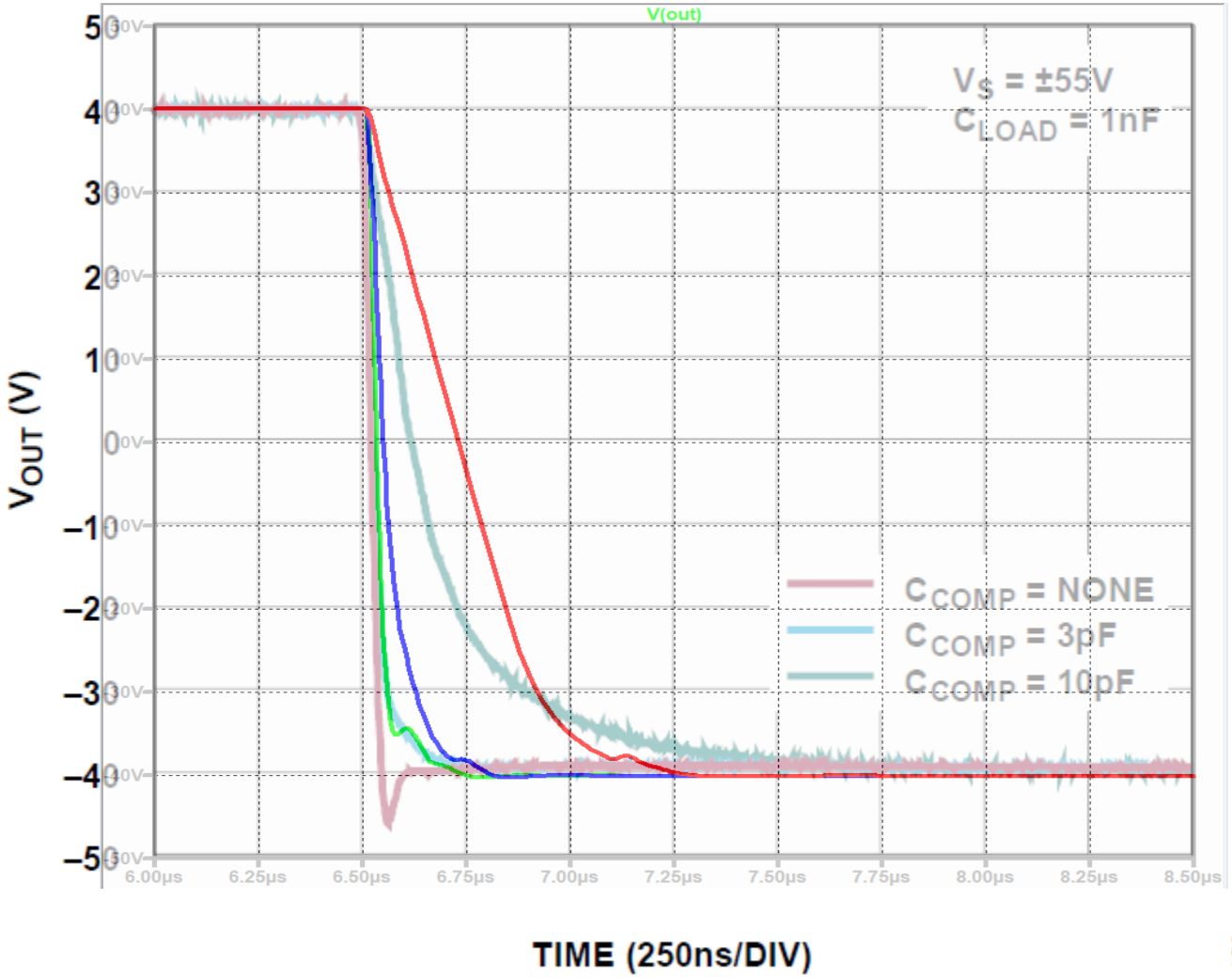


Figure 9. Falling Edge - Large Signal Pulse Response vs. C_{LOAD} and C_{COMP}, Falling Edge, C_{LOAD} = 1 nF

- AD8460 LTspice Plot comparison with Datasheet Curves for Large Signal Pulse Response.
- Model was designed for Ccomp = NONE, Cload = 1nF.
- Step response changes with different Ccomp. Not an exact match, but a close trend to Real IC, given model trade-offs.

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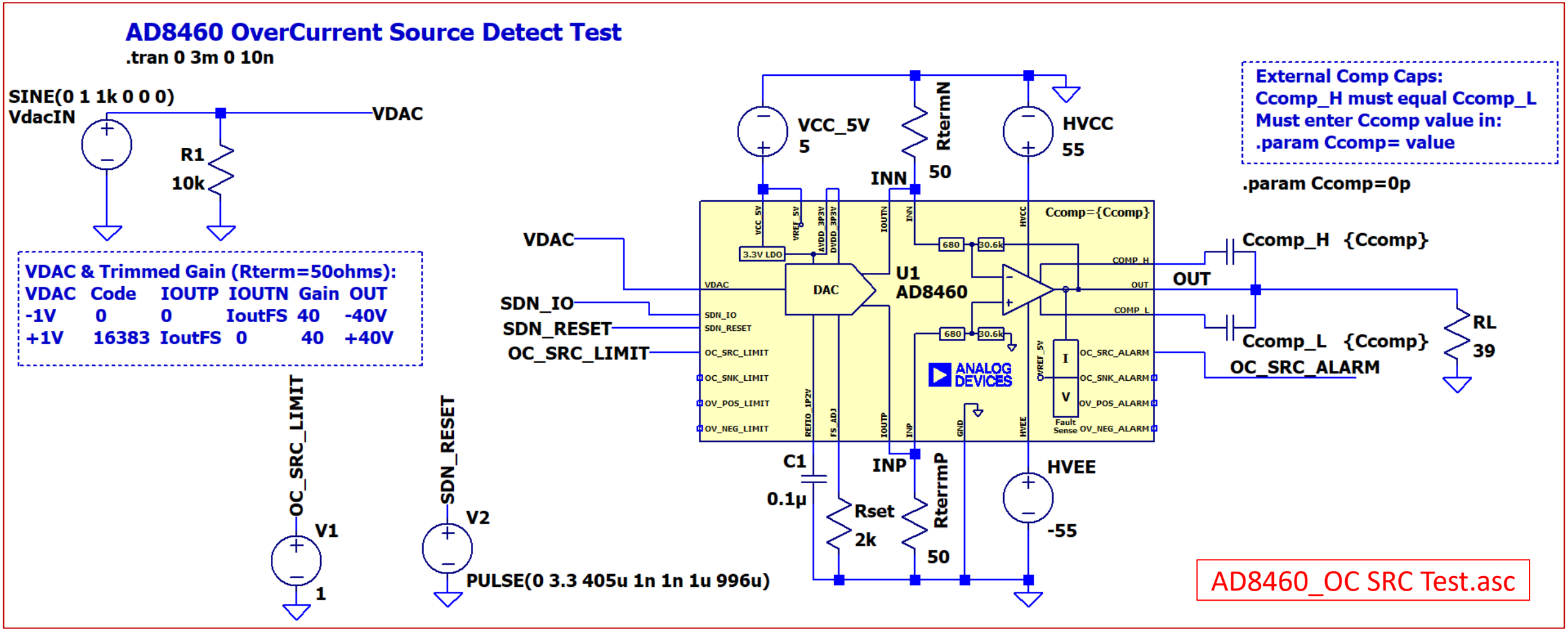
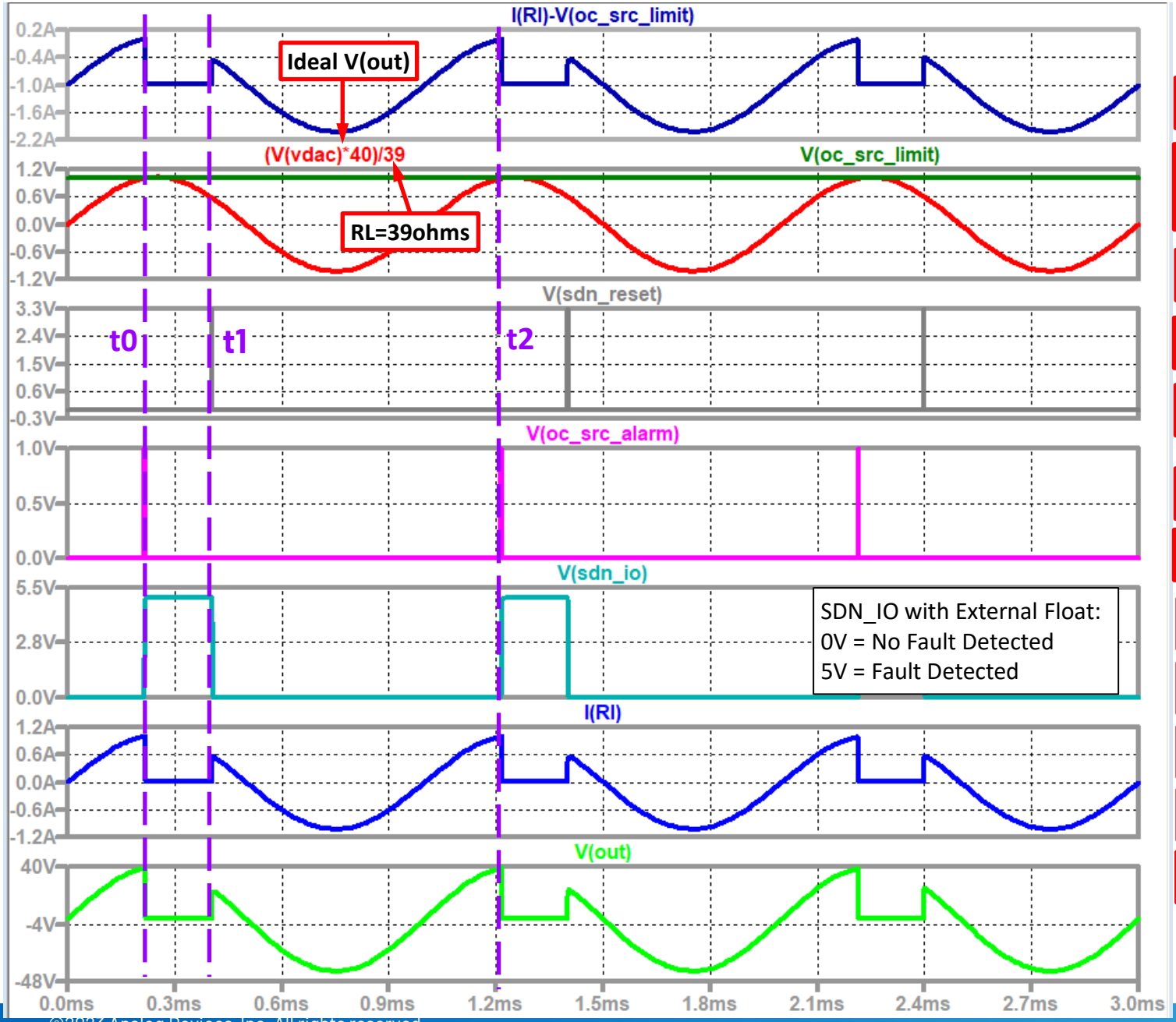
Fault Detect Operation

OverCurrent Source Fault Test



OverCurrent Source Fault Test



t0: I(RL) – V(OC_SRC_LIMIT) = 0 → OC_SRC trip

t0: (V(VDAC)*40)/39 > V(OC_SRC_LIMIT) → OC_SRC trip

t0: V(SDN_RESET) is set at 0V (Logic Low)

t0: V(OC_SRC_ALARM) goes high due to OC_SRC trip and then drops back to zero when amp is disabled, OC_SRC fault is gone

t0: V(SDN_IO) goes high due to OC_SRC trip

t0: I(RL) drops to zero as amp shuts off due to OC_SRC trip

t0: V(OUT) drops to zero as amp shuts off due to OC_SRC trip

t1: I(RL) – V(OC_SRC_LIMIT) ≠ 0 → No OC_SRC Fault

t1: (V(Vdac)*40)/39 < V(OC_SRC_LIMIT) → No OC _SRC Fault

t1: V(SDN_RESET) is pulsed from low to high (Logic high > 1.65V)

t1: V(SDN_IO) is set to low and power amp is enabled

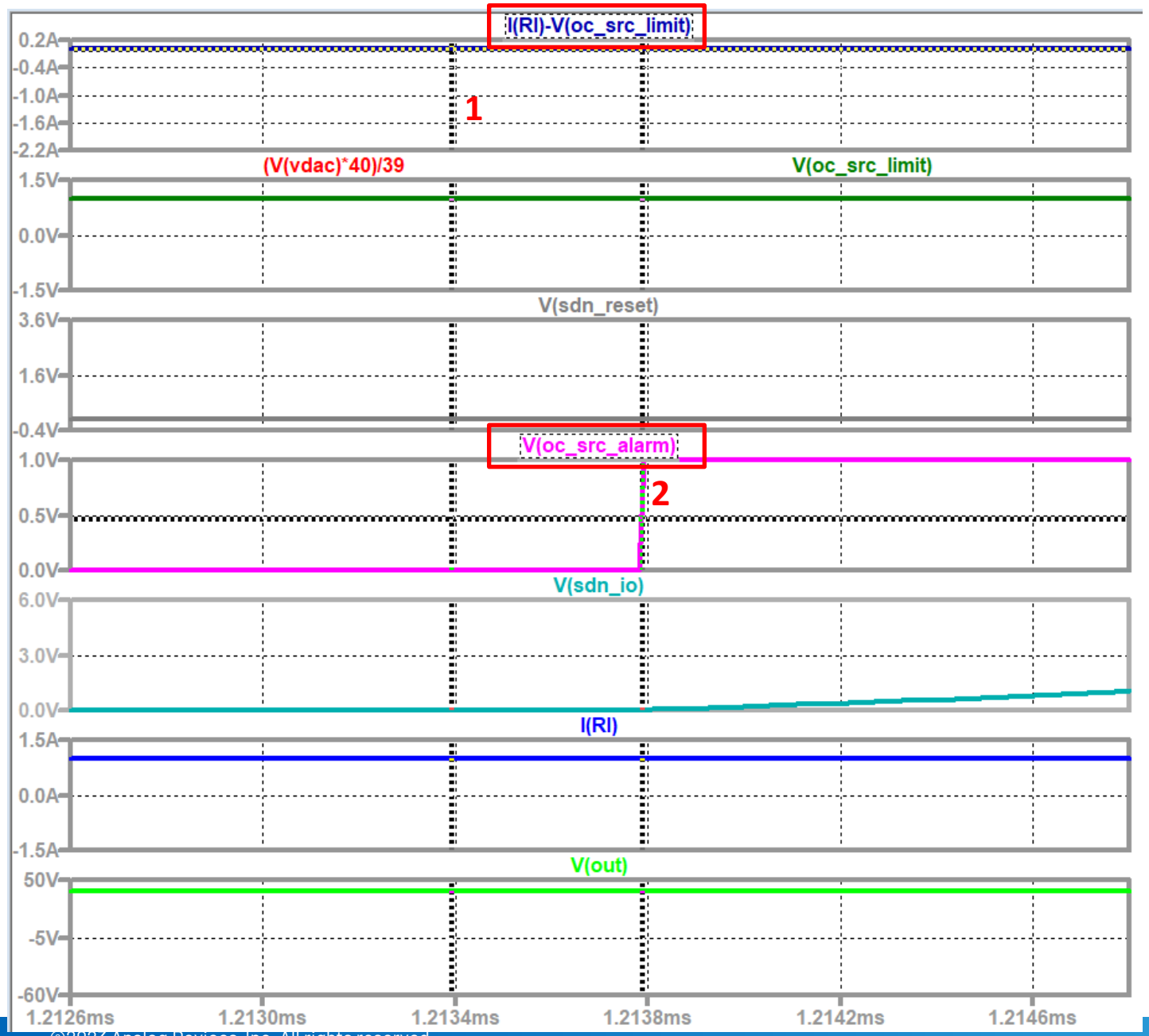
t1: V(OC_SRC_ALARM) stays at zero as no OC_SRC Fault

t1: I(RL) returns to V(OUT)/RL

t1: V(OUT) returns to V(VDAC)*40

t2: Fault condition repeats – check over many cycles

OverCurrent Source Fault Test



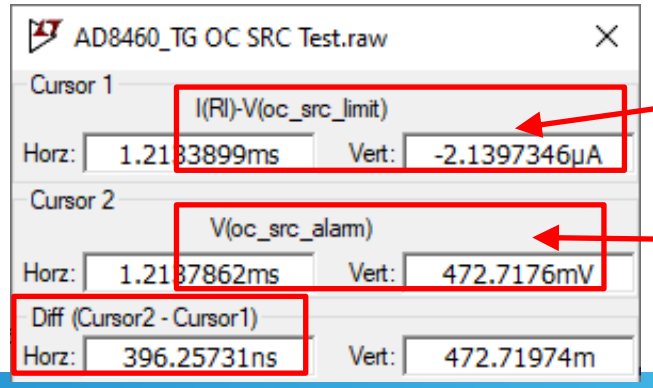
Zoom-in1

SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected

I(RL) – V(OC_SRC_LIMIT) at 0A gives us the trip point time due to OverCurrent Source Fault at Cursor 1.

V(OC_SRC_ALARM) goes high at Cursor 2, when I(RL) goes above V(OC_SRC_LIMIT) threshold, at Cursor 1, after an internal programmed delay.

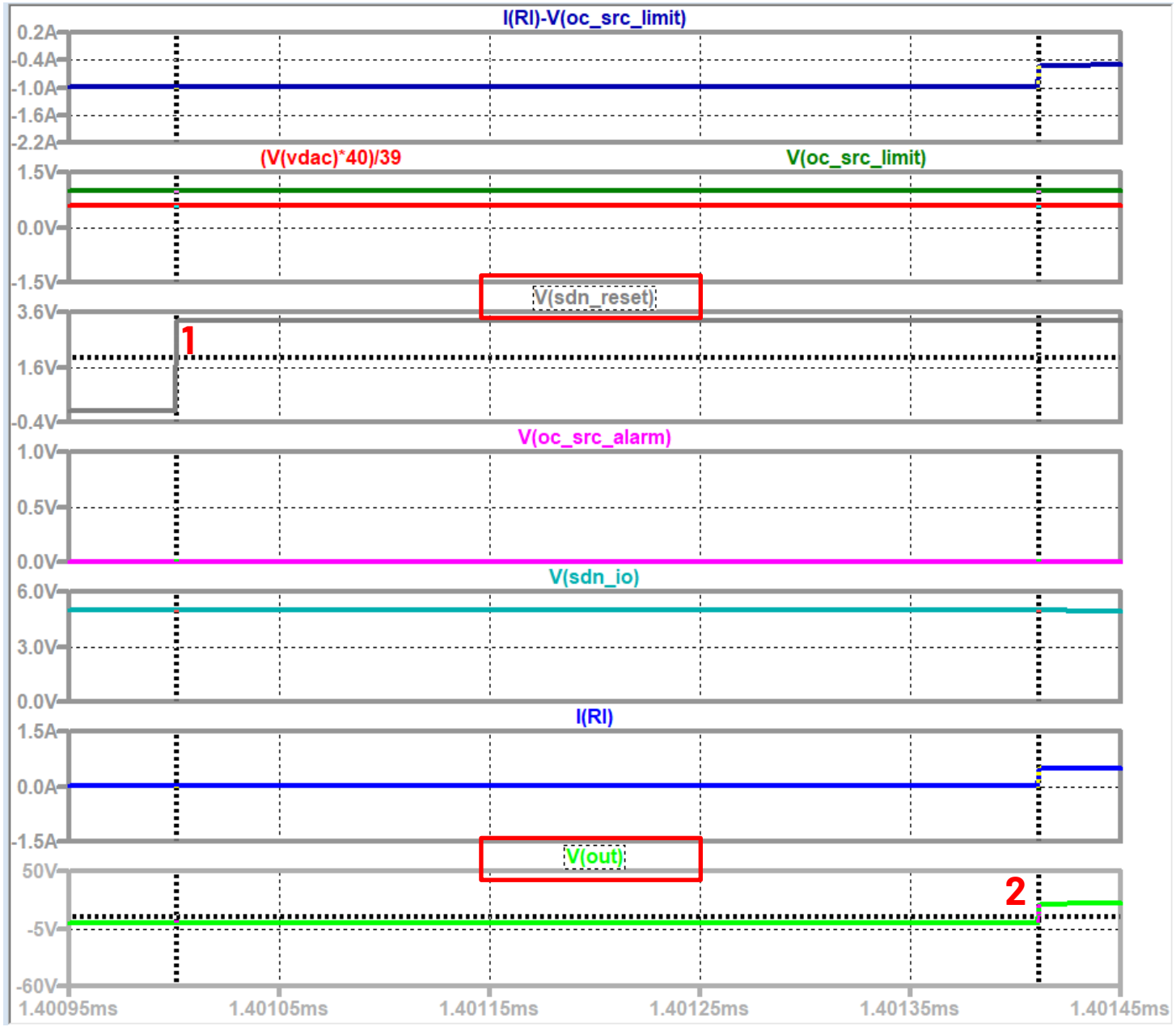
Diff (Cursor2-Cursor1) delta gives us the delay from an OverCurrent Source Fault and V(OC_SRC_ALARM) going high ***Should be 400ns***



As close to 0A as possible.

As close to 500mV as possible.

OverCurrent Source Fault Test



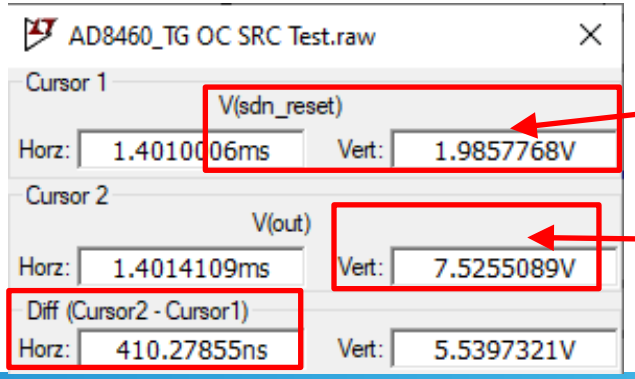
Zoom-in2

SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected

V(SDN_RESET) is pulsed high at Cursor 1

V(OUT) is enabled at Cursor 2

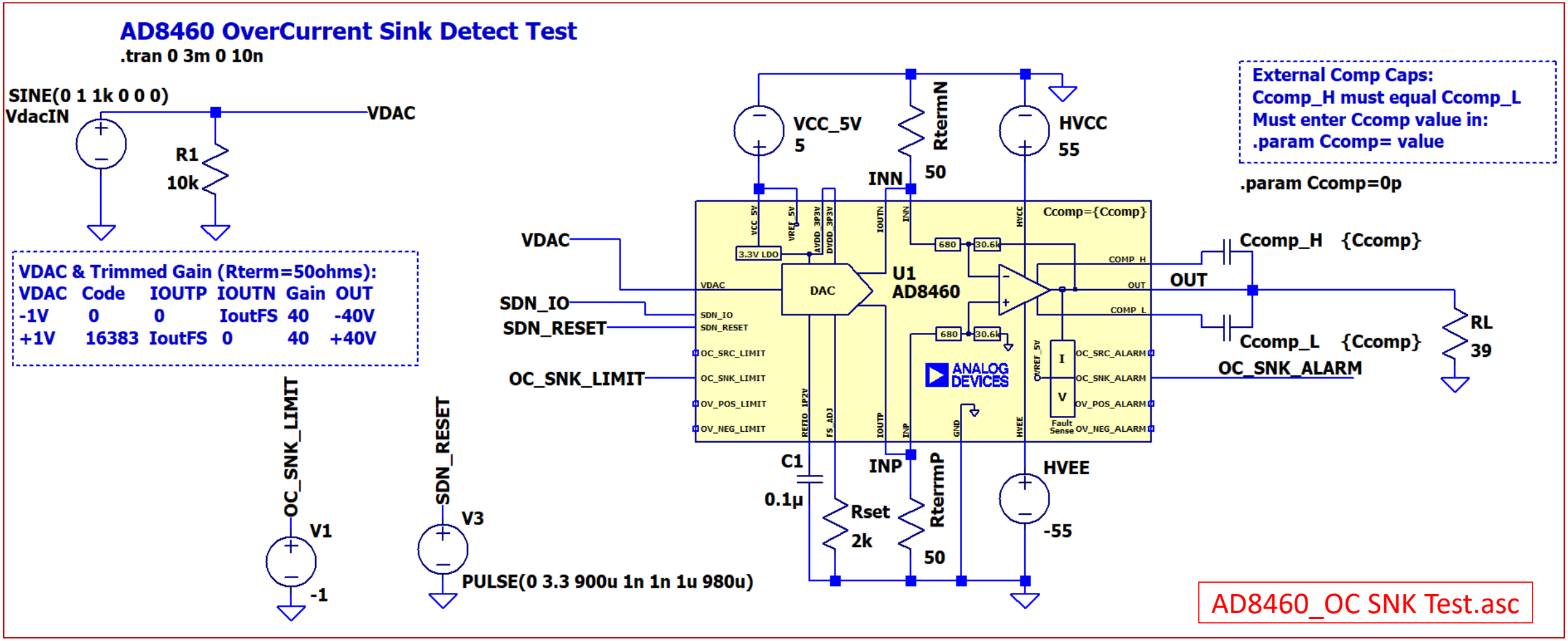
Diff (Cursor2-Cursor1) delta gives us the delay from V(SDN_RESET) going high to V(OUT) enabled.
Should be 410ns



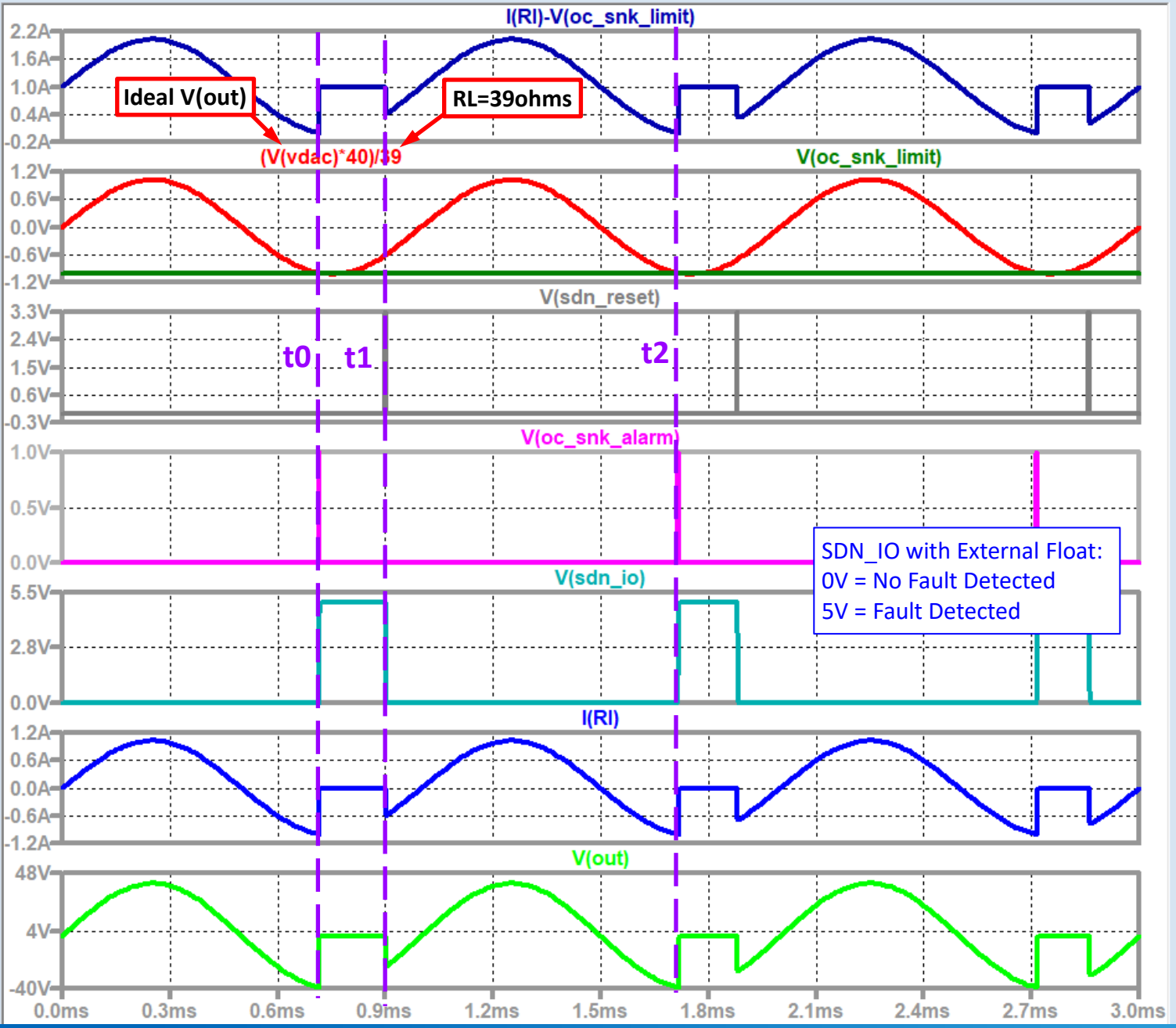
As close to 1.65V as possible.

As close to just > 0V as possible.

OverCurrent Sink Fault Test



OverCurrent Sink Fault Test



t0: I(RL) – V(OC_SNK_LIMIT) = 0 → OC_SNK trip

t0: (V(VDAC)*40)/39 < V(OC_SNK_LIMIT) → OC_SNK trip

t0: V(SDN_RESET) is set at 0V (Logic Low)

t0: V(OC_SNK_ALARM) goes high due to OC_SNK trip and then drops back to zero when amp is disabled, OC_SNK fault is gone

t0: V(SDN_IO) goes high due to OC_SNK trip

t0: I(RL) drops to zero as amp shuts off due to OC_SNK trip

t0: V(OUT) drops to zero as amp shuts off due to OC_SNK trip

t1: I(RL) – V(OC_SNK_LIMIT) ≠ 0 → No OC_SNK Fault

t1: (V(Vdac)*40)/39 > V(OC_SNK_LIMIT) → No OC _SNK Fault

t1: V(SDN_RESET) is pulsed from low to high (Logic high > 1.65V)

t1: V(SDN_IO) is set to low and power amp is enabled

t1: V(OC_SNK_ALARM) stays at zero as no OC_SNK Fault

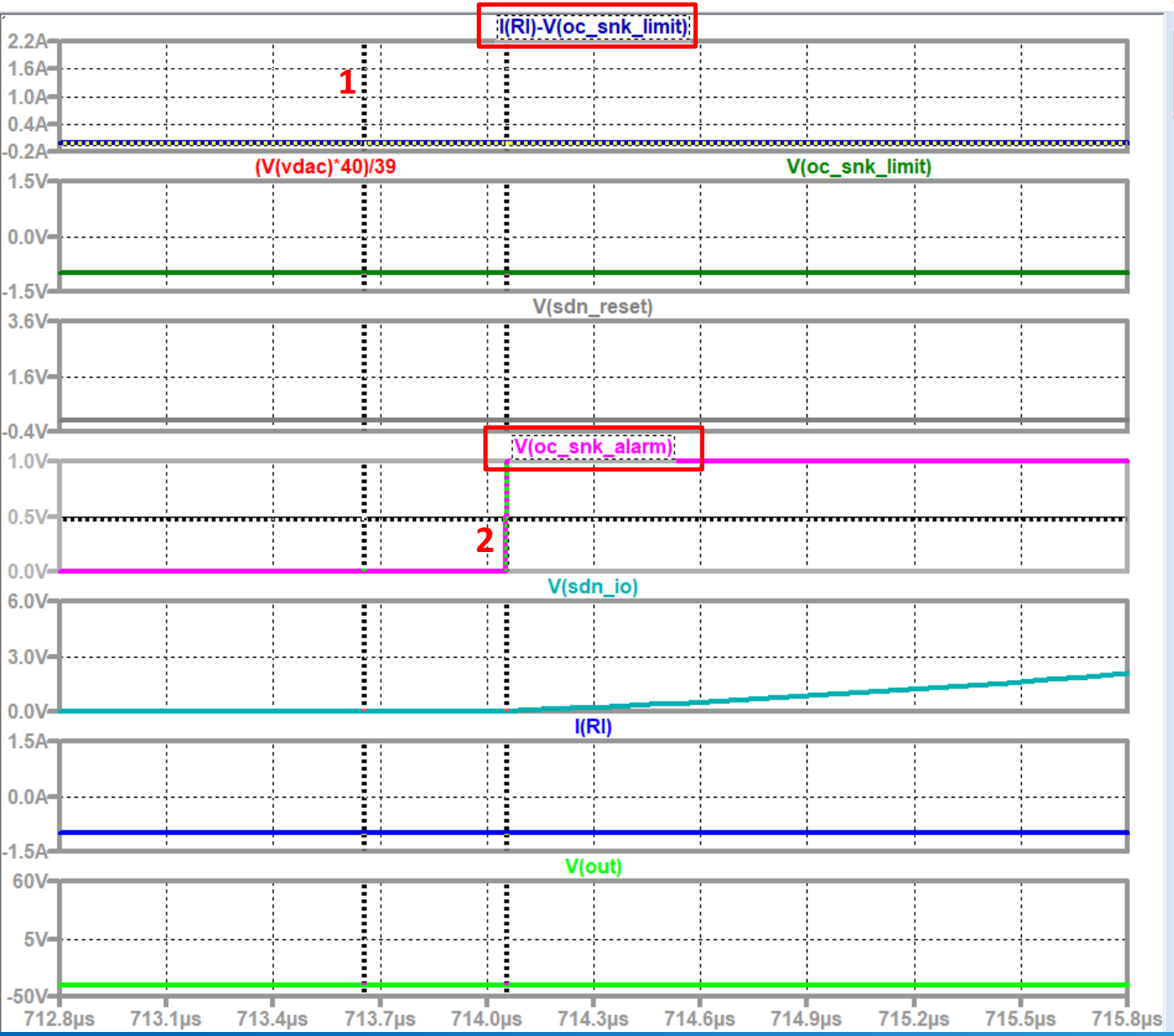
t1: I(RL) returns to V(OUT)/RL

t1: V(OUT) returns to V(VDAC)*40

t2: Fault condition repeats – check over many cycles

OverCurrent Sink Fault Test

Zoom-in1

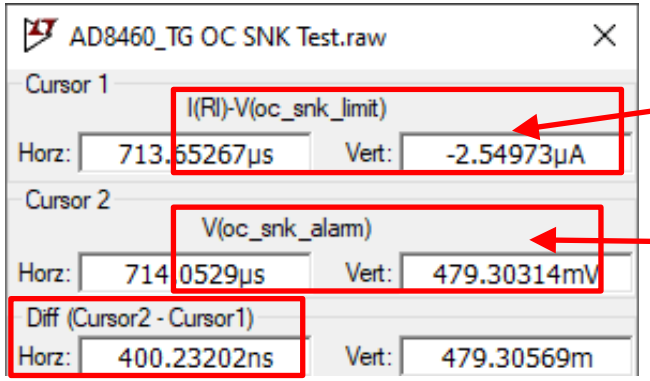


I(RL) – V(OC_SNK_LIMIT) at 0A gives us the trip point time due to OverCurrent Sink Fault at Cursor 1.

SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected

V(OC_SNK_ALARM) goes high at Cursor 2, when I(RL) goes below V(OC_SNK_LIMIT) threshold, at Cursor 1, after an internal programmed delay.

Diff (Cursor2-Cursor1) delta gives us the delay from an OverCurrent Sink Fault and V(OC_SNK_ALARM) going high ***Should be 400ns***



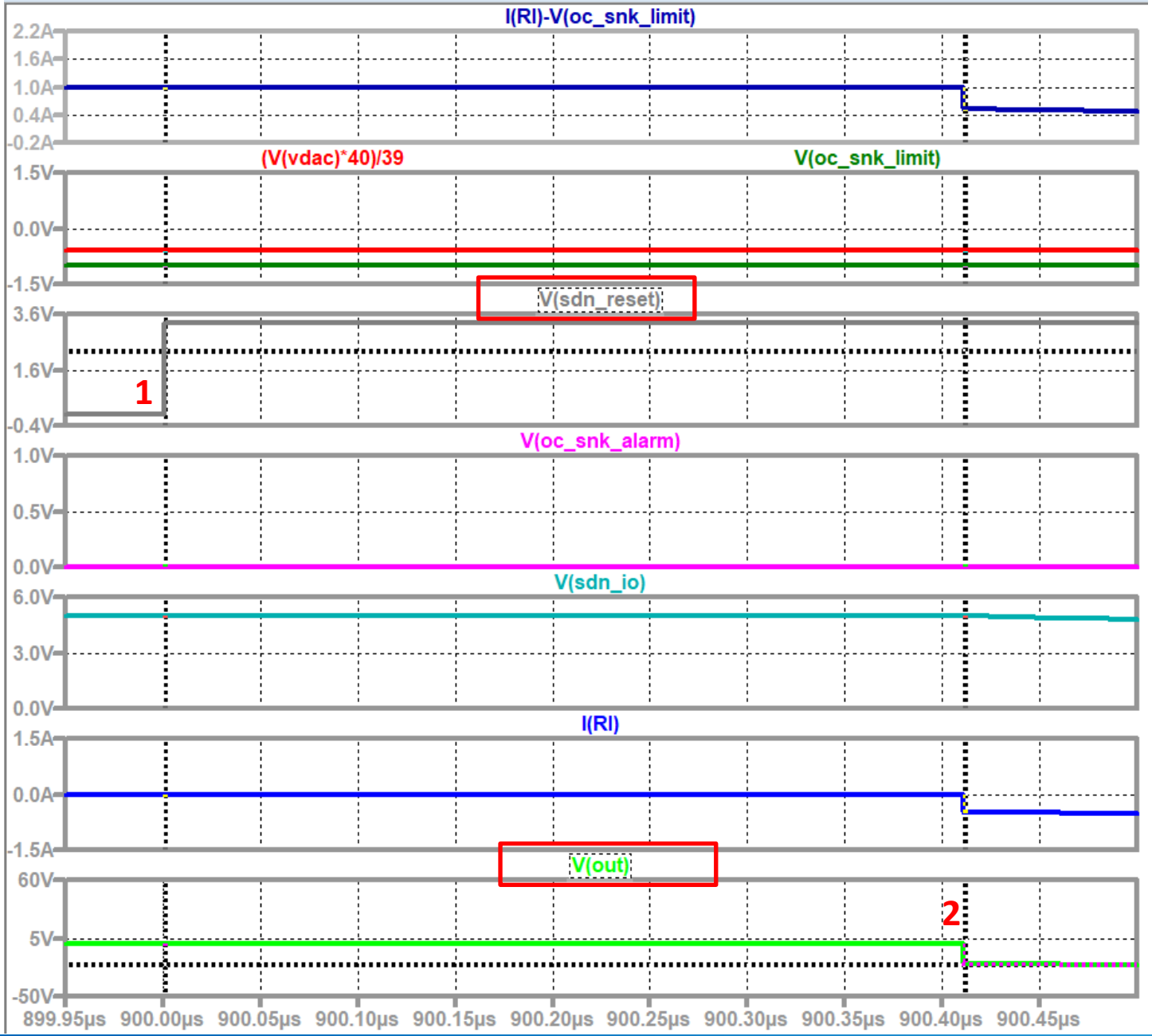
As close to 0A as possible.

As close to 500mV as possible.

OverCurrent Sink Fault Test

Zoom-in2

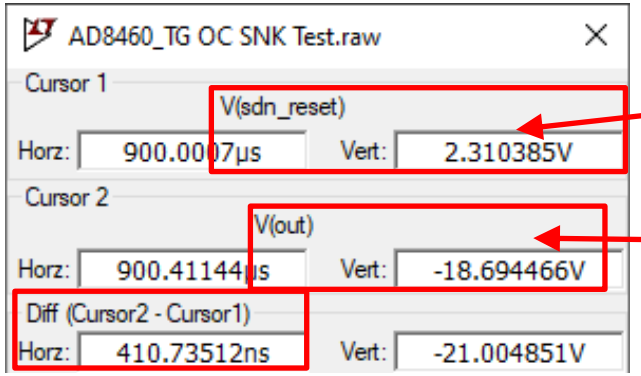
SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected



V(SDN_RESET) is pulsed high at Cursor 1

V(OUT) is enabled at Cursor 2

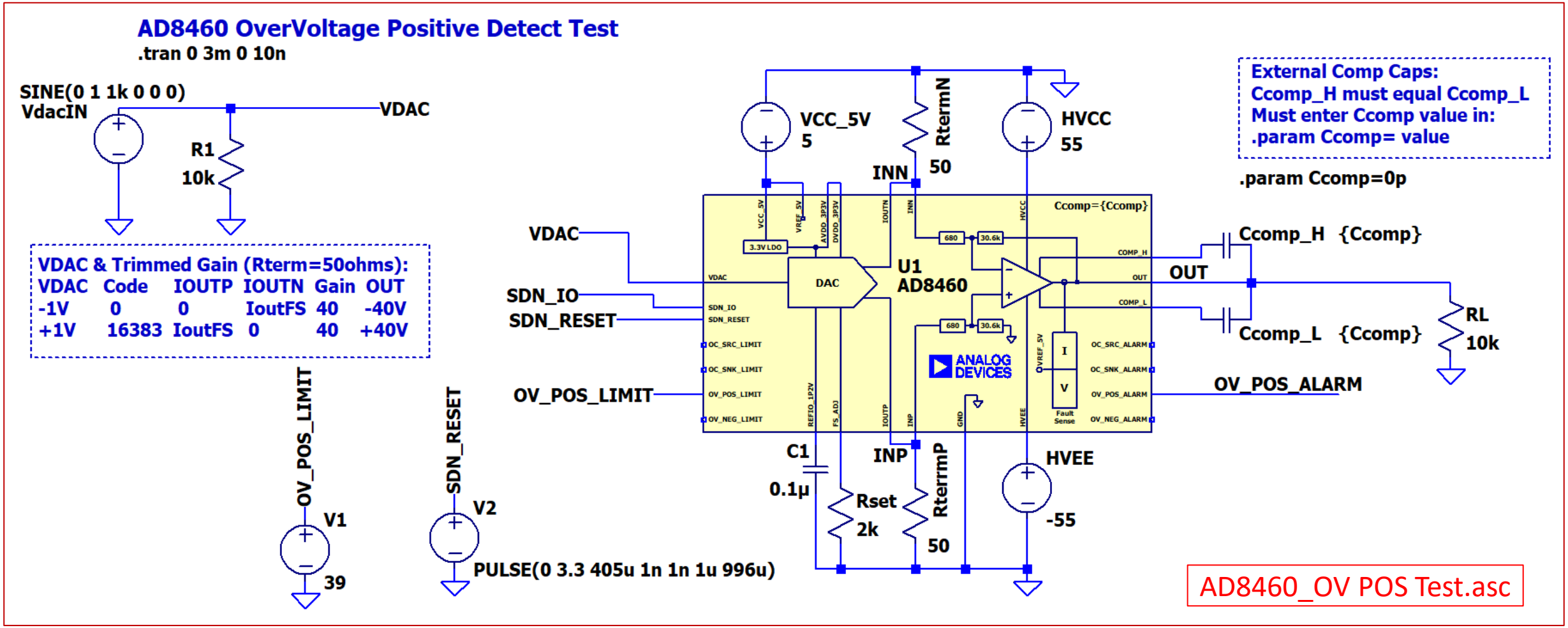
Diff (Cursor2-Cursor1) delta gives us the delay from V(SDN_RESET) going high to V(OUT) enabled.
Should be 410ns



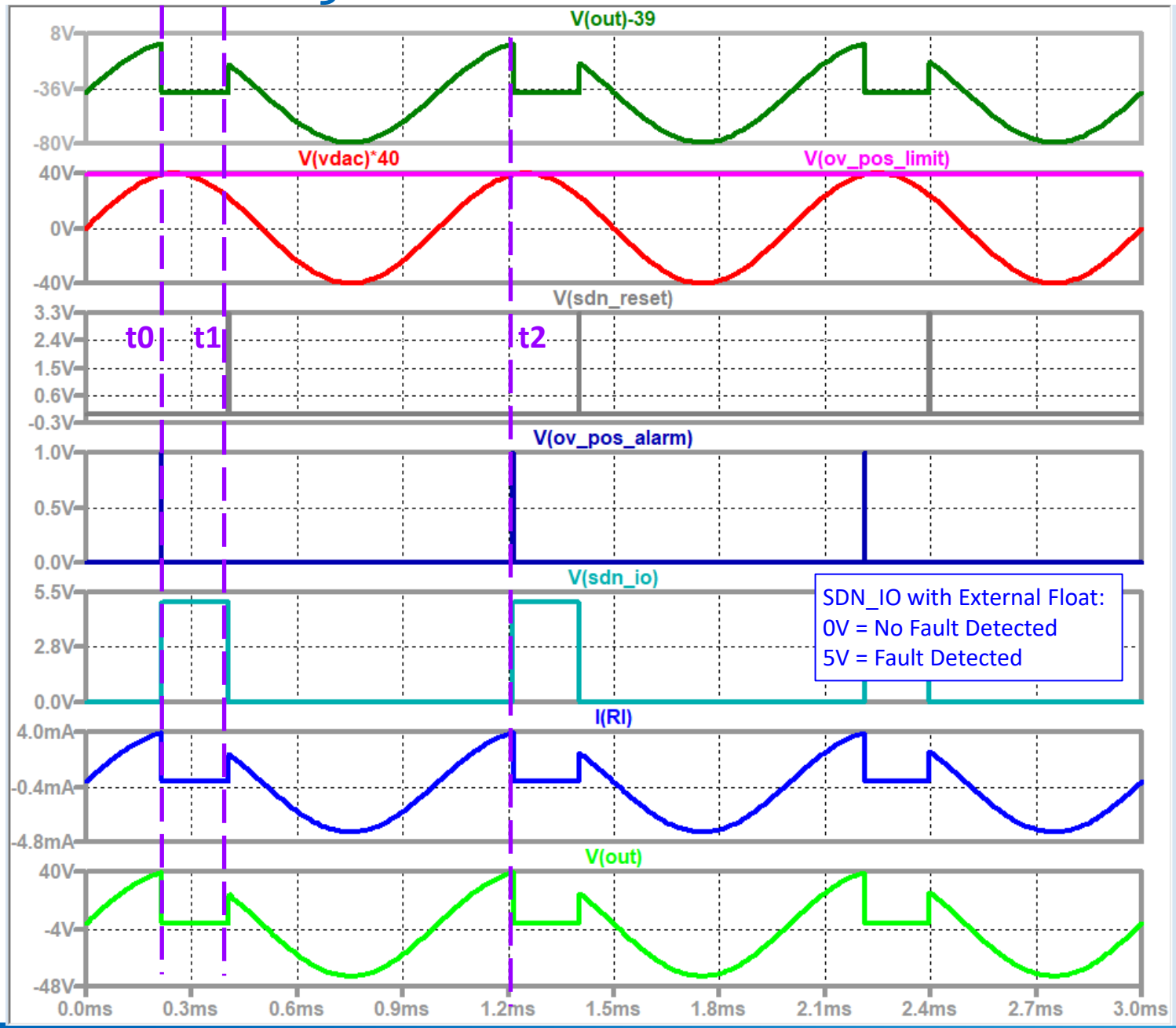
As close to 1.65V as possible.

As close to just < 0V as possible.

OverVoltage Positive Fault Test



OverVoltage Positive Fault Test



t0: V(OUT)-39 = 0 → OV_POS trip

t0: (V(DAC)*40) > V(OV_POS_LIMIT) → OV_POS trip

t0: V(SDN_RESET) is set at 0V (Logic Low)

t0: V(OV_POS_ALARM) goes high due to OV_POS trip and then drops back to zero when amp is disabled, OV_POS fault is gone

t0: V(SDN_IO) goes high due to OV_POS trip

t0: I(RL) drops to zero as amp shuts off due to OV_POS trip

t0: V(OUT) drops to zero as amp shuts off due to OV_POS trip

t1: V(OUT)-39 ≠ 0 → No OV_POS Fault

t1: (V(Vdac)*40) < V(OV_POS_LIMIT) → No OV _POS Fault

t1: V(SDN_RESET) is pulsed from low to high (Logic high > 1.65V)

t1: V(SDN_IO) is set to low and power amp is enabled

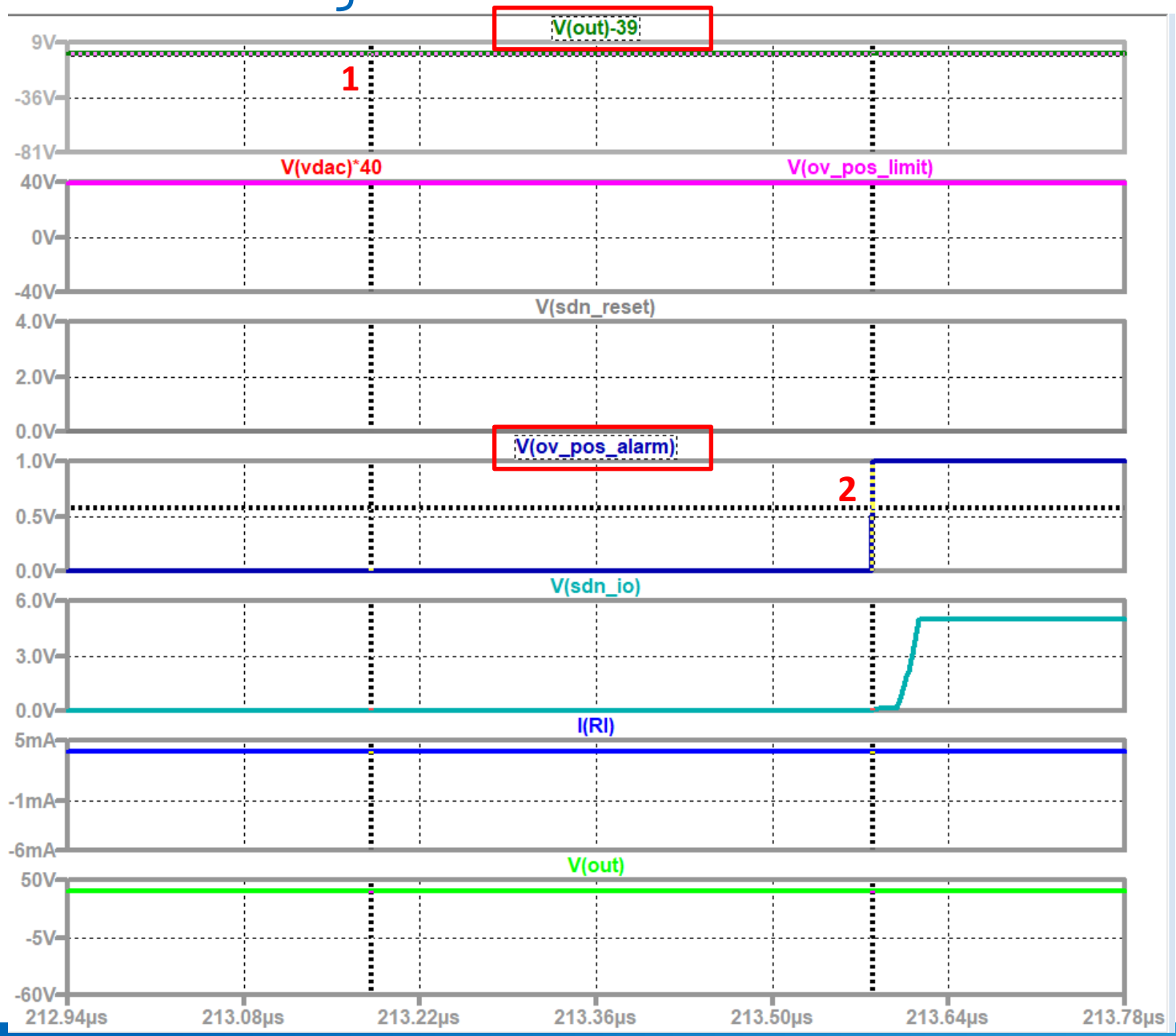
t1: V(OV_POS_ALARM) stays at zero as no OV_POS Fault

t1: I(RL) returns to V(OUT)/RL

t1: V(OUT) returns to V(DAC)*40

t2: Fault condition repeats – check over many cycles

OverVoltage Positive Fault Test



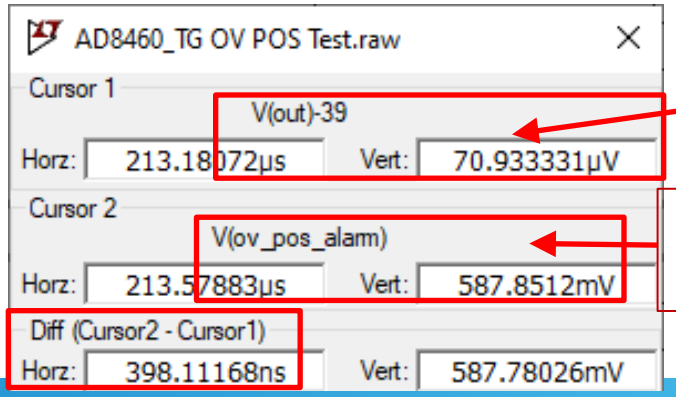
Zoom-in1

V(OUT)-39 = 0 at 0A gives us the trip point time due to OverVoltage Positive Fault at Cursor 1.

SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected

V(OV_POS_ALARM) goes high at Cursor 2, when V(OUT) goes above V(OV_POS_LIMIT) threshold, at Cursor 1, after an internal programmed delay.

Diff (Cursor2-Cursor1) delta gives us the delay from an OverVoltage Positive Fault and V(OV_POS_ALARM) going high ***Should be 400ns***

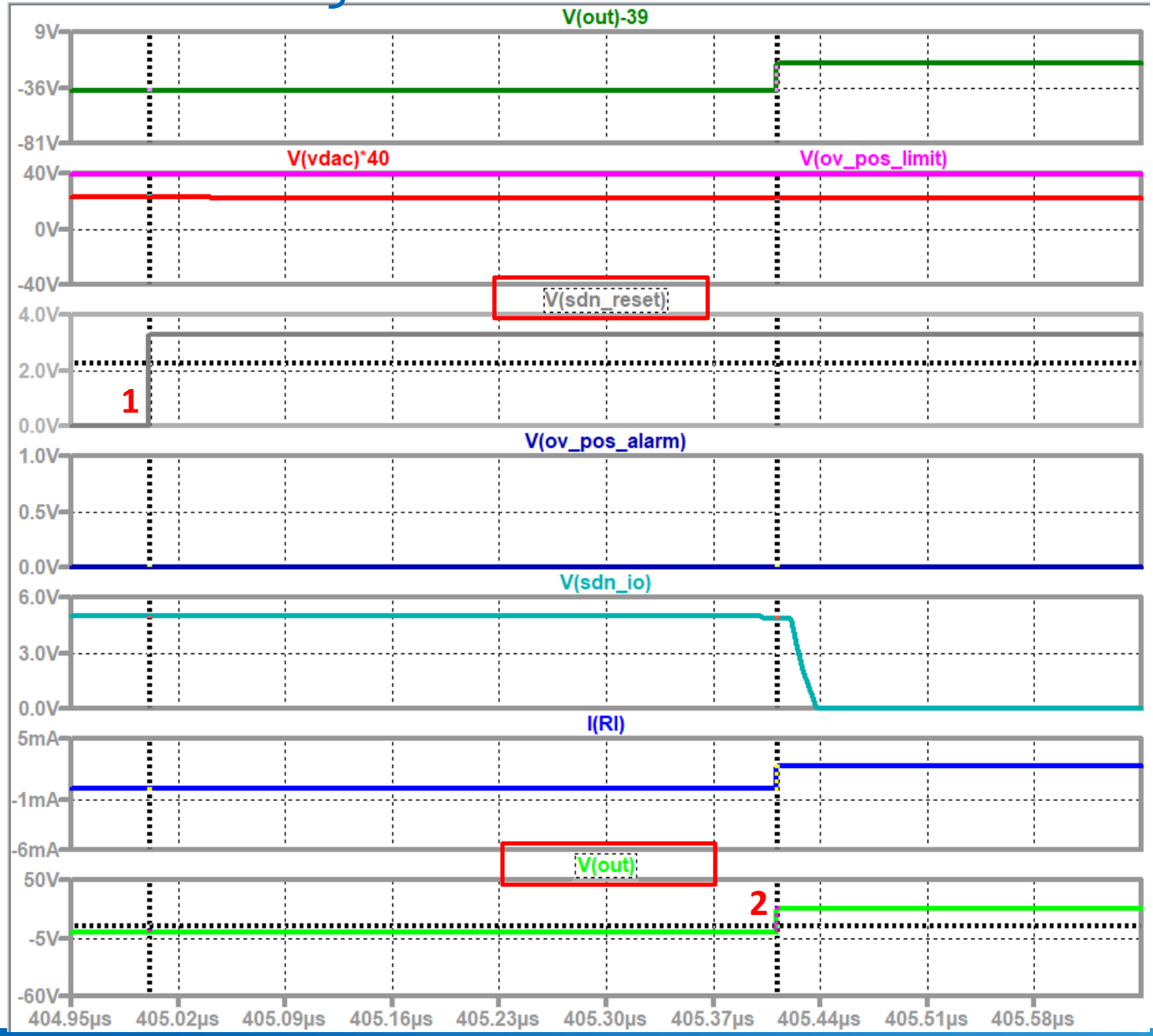


As close to 0V as possible.

As close to 500mV as possible.

OverVoltage Positive Fault Test

Zoom-in2

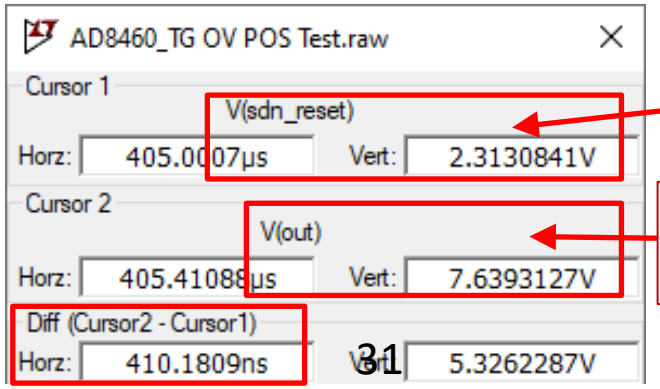


SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected

V(SDN_RESET) is pulsed high at Cursor 1

V(OUT) is enabled at Cursor 2

Diff (Cursor2-Cursor1) delta gives us the delay from V(SDN_RESET) going high to V(OUT) enabled.
Should be 410ns



As close to 1.65V as possible.

As close to just > 0V as possible.

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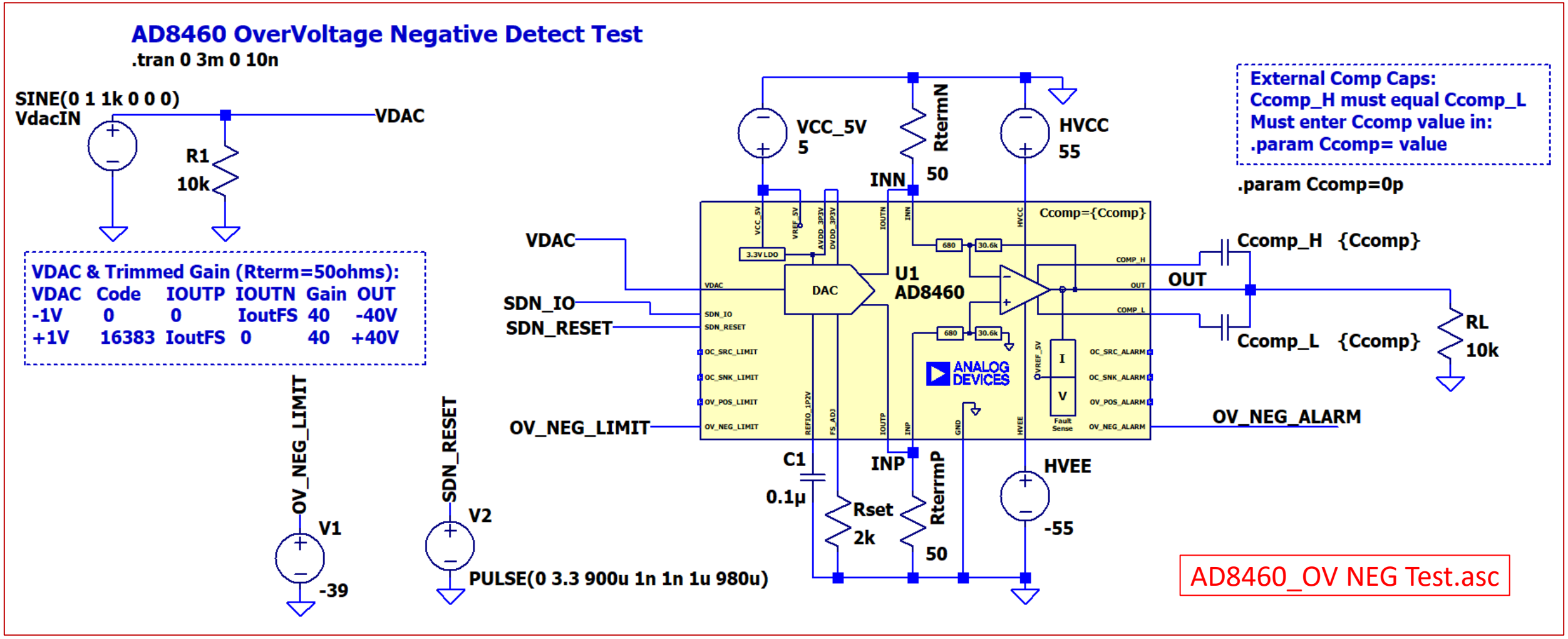
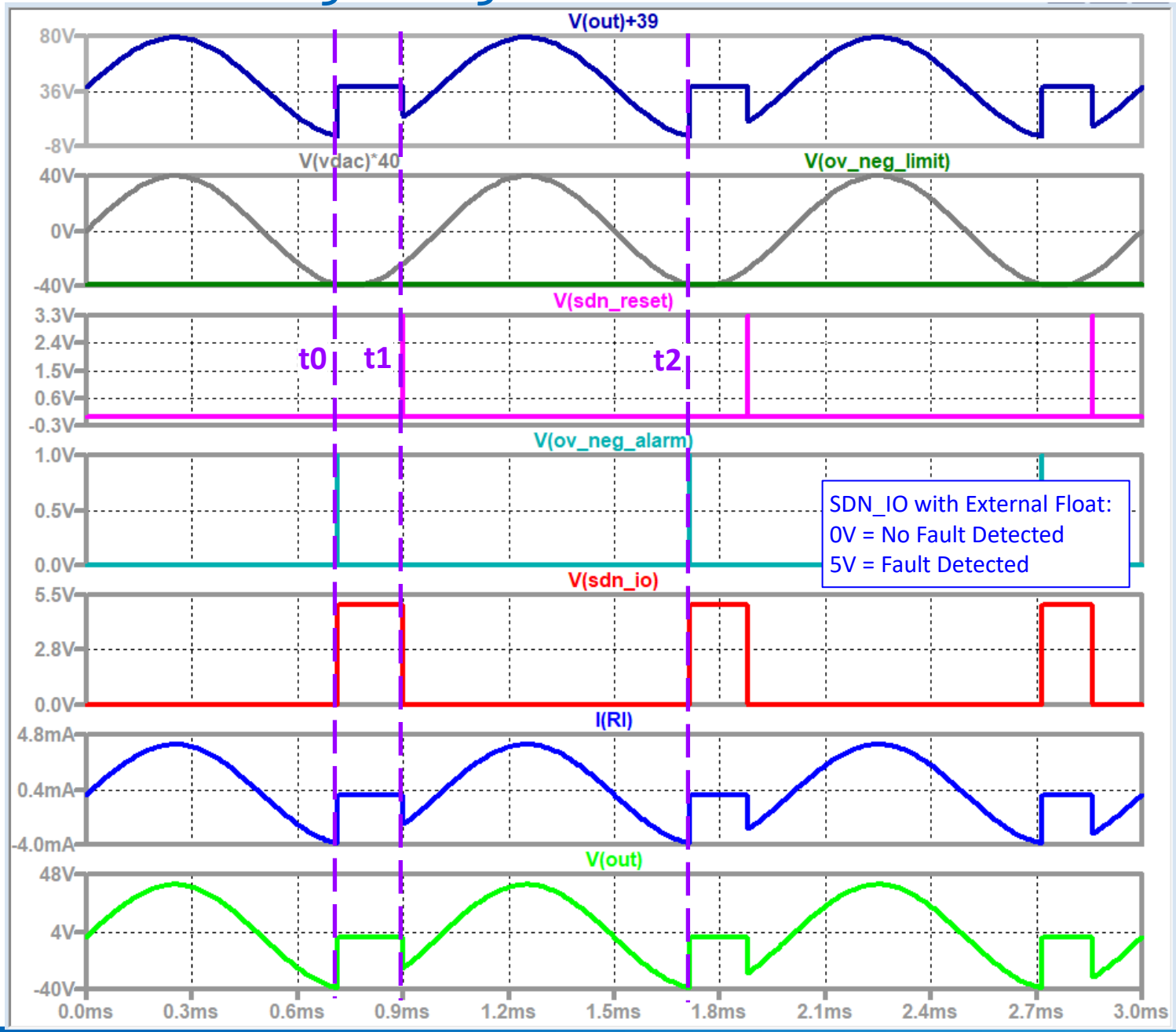
OverVoltage Negative Fault Test



OverVoltage Negative Fault Test



t0: V(OUT)+39 = 0 → OV_NEG trip

t0: (V(VDAC)*40) < V(OV_NEG_LIMIT) → OV_NEG trip

t0: V(SDN_RESET) is set at 0V (Logic Low)

t0: V(OV_NEG_ALARM) goes high due to OV_NEG trip and then drops back to zero when amp is disabled, OV_NEG fault is gone

t0: V(SDN_IO) goes high due to OV_NEG trip

t0: I(RL) drops to zero as amp shuts off due to OV_NEG trip

t0: V(OUT) drops to zero as amp shuts off due to OV_NEG trip

t1: V(OUT)+39 ≠ 0 → No OV_NEG Fault

t1: (V(Vdac)*40) > V(OV_NEG_LIMIT) → No OV _NEG Fault

t1: V(SDN_RESET) is pulsed from low to high (Logic high > 1.65V)

t1: V(SDN_IO) is set to low and power amp is enabled

t1: V(OV_NEG_ALARM) stays at zero as no OV_NEG Fault

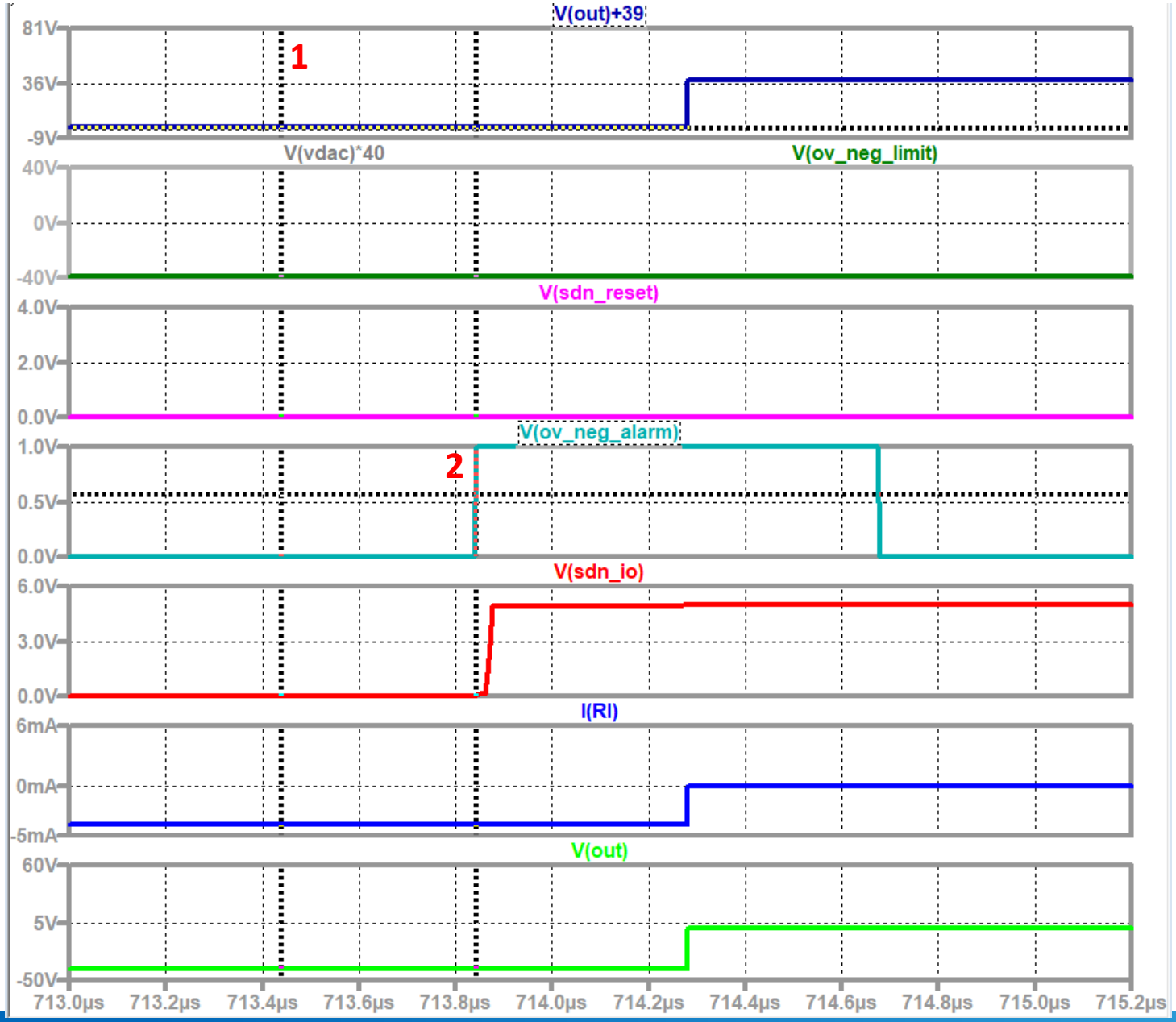
t1: I(RL) returns to V(OUT)/RL

t1: V(OUT) returns to V(VDAC)*40

t2: Fault condition repeats – check over many cycles

OverVoltage Negative Fault Test

Zoom-in1

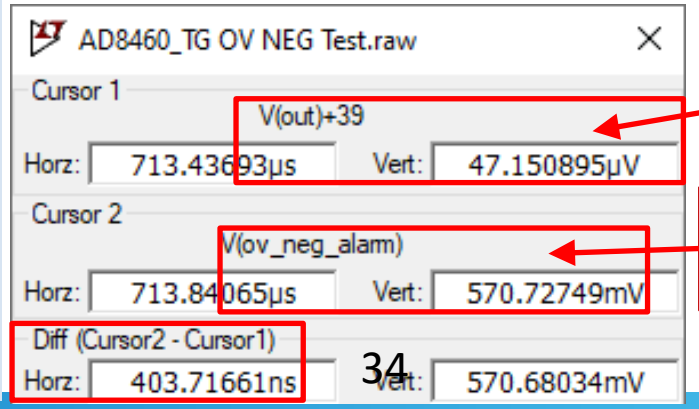


V(OUT)+39 = 0 at 0A gives us the trip point time due to OverVoltage Negative Fault at Cursor 1.

SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected

V(OV_NEG_ALARM) goes high at Cursor 2, when V(OUT) goes below V(OV_NEG_LIMIT) threshold, at Cursor 1, after an internal programmed delay.

Diff (Cursor2-Cursor1) delta gives us the delay from an OverCurrent Negative Fault and V(OV_NEG_ALARM) going high ***Should be 400ns***



As close to 0V as possible.

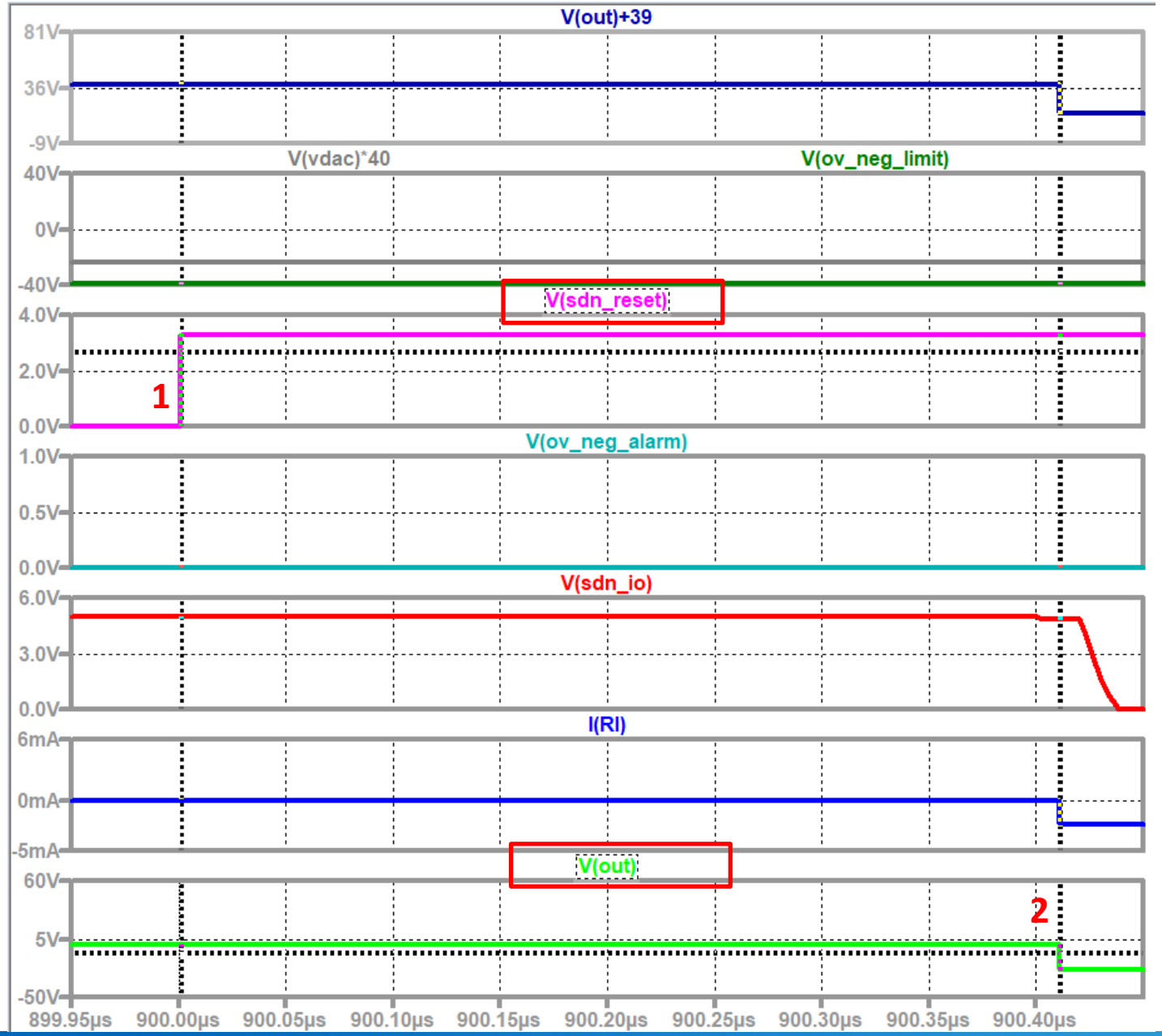
As close to 500mV as possible.

34

OverVoltage Negative Fault Test

Zoom-in2

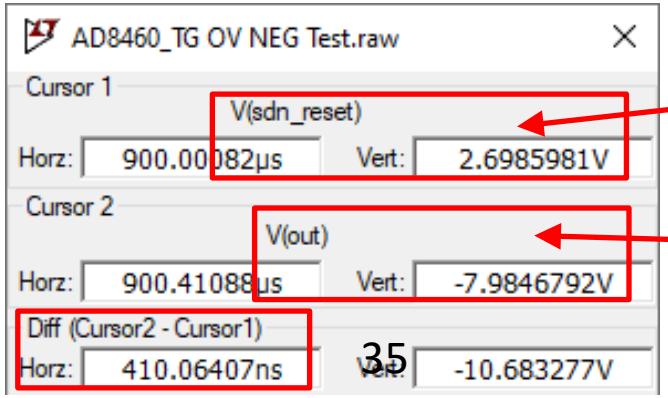
SDN_IO with External Float:
0V = No Fault Detected
5V = Fault Detected



V(SDN_RESET) is pulsed high at Cursor 1

V(OUT) is enabled at Cursor 2

Diff (Cursor2-Cursor1) delta gives us the delay from V(SDN_RESET) going high to V(OUT) enabled.
Should be 410ns



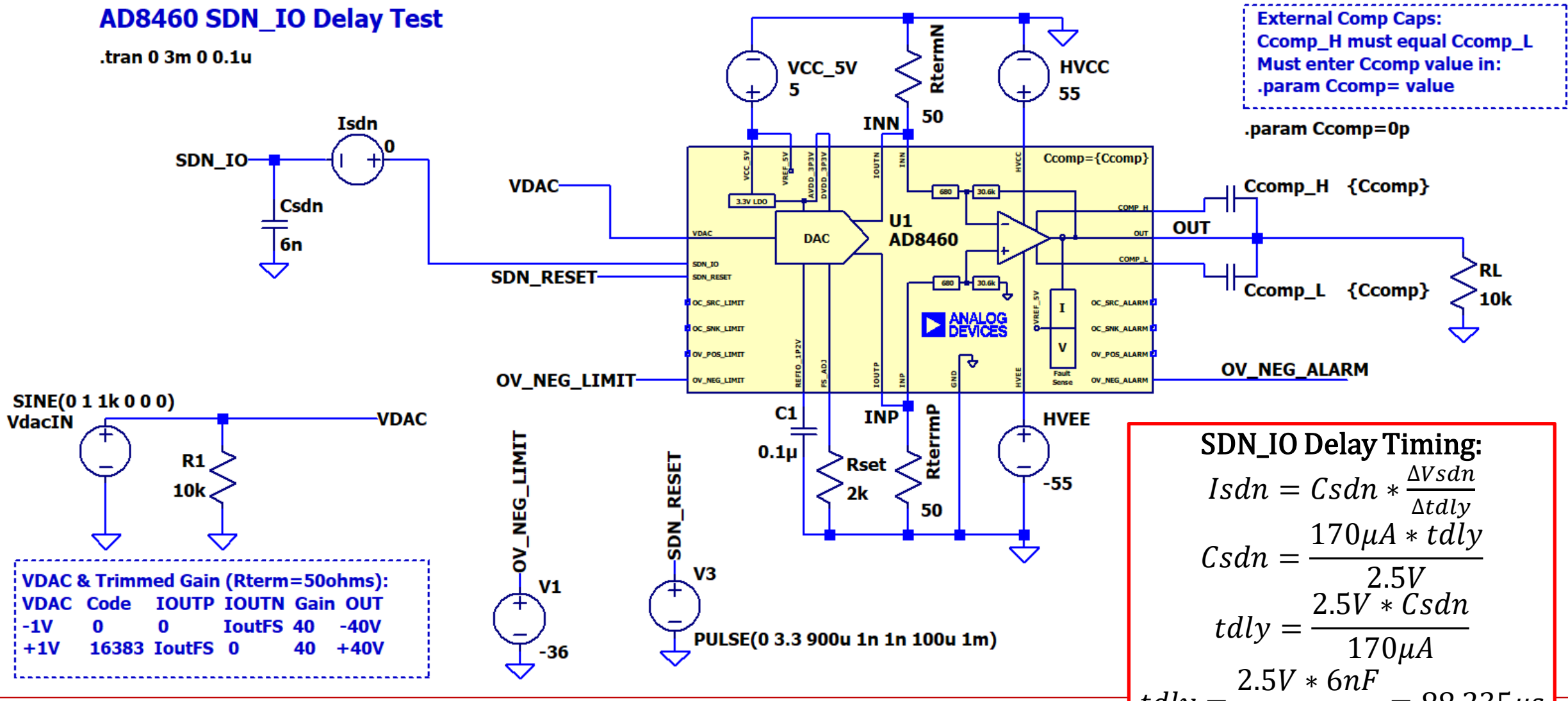
As close to 1.65V as possible.

As close to just < 0V as possible.

SDN_IO Operation
SDN_RESET Operation

SDN_IO Fault Detect Delay

AD8460_SDN_IO Delay Test.asc



SDN_IO Delay Timing:

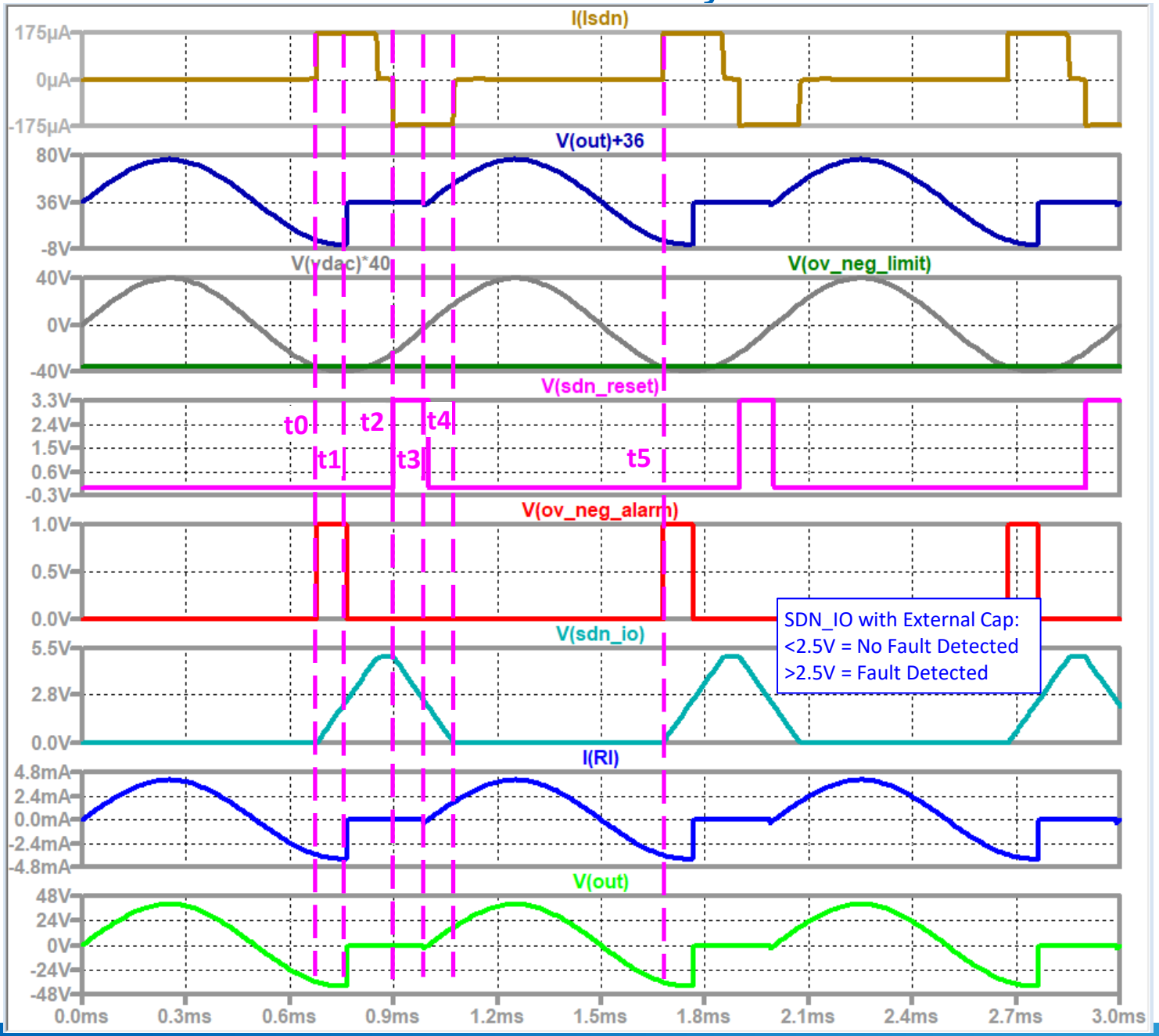
$$Isdn = Csdn * \frac{\Delta Vsdn}{\Delta tdly}$$

$$Csdn = \frac{170\mu A * tdly}{2.5V}$$

$$tdly = \frac{2.5V * Csdn}{170\mu A}$$

$$tdly = \frac{2.5V * 6nF}{170\mu A} = 88.235\mu s$$

SDN_IO Fault Detect Delay



t0: V(OUT)+36 = 0 → OV_NEG trip

t0: (V(VDAC)*40) < V(OV_NEG_LIMIT) → OV_NEG trip

t0: V(SDN_RESET) is set at 0V (Logic Low)

t0: V(OV_NEG_ALARM) goes high due to OV_NEG trip

t0: SDN_IO positive current source (170uA) is turned on

t0: V(SDN_IO) ramps toward 2.5V threshold, due to Csdn capacitor, 6nF. Power Op Amp enabled until SDN_IO > 2.5V.

t1: V(VSDN_IO) > 2.5V, after predicted 88us ramp to 2.5V due to Csdn, 6nF. Power Op Amp is disabled due to OV_NEG Fault.

t1: I(RL) drops zero as amp shuts off due to OV_NEG trip

t1: V(OUT) drops zero as Power Op Amp shuts off due to SDN_IO > 2.5V

t1: V(OV_NEG_ALARM) low since Power Op Amp is disabled

t2: V(SDN_RESET) is pulsed from low to high (Logic high > 1.65V) SDN_IO negative current source (-170uA) is enabled

t2: V(SDN_RESET) must remain high until SDN_IO discharges to <2.5V to clear the OV_NEG Fault

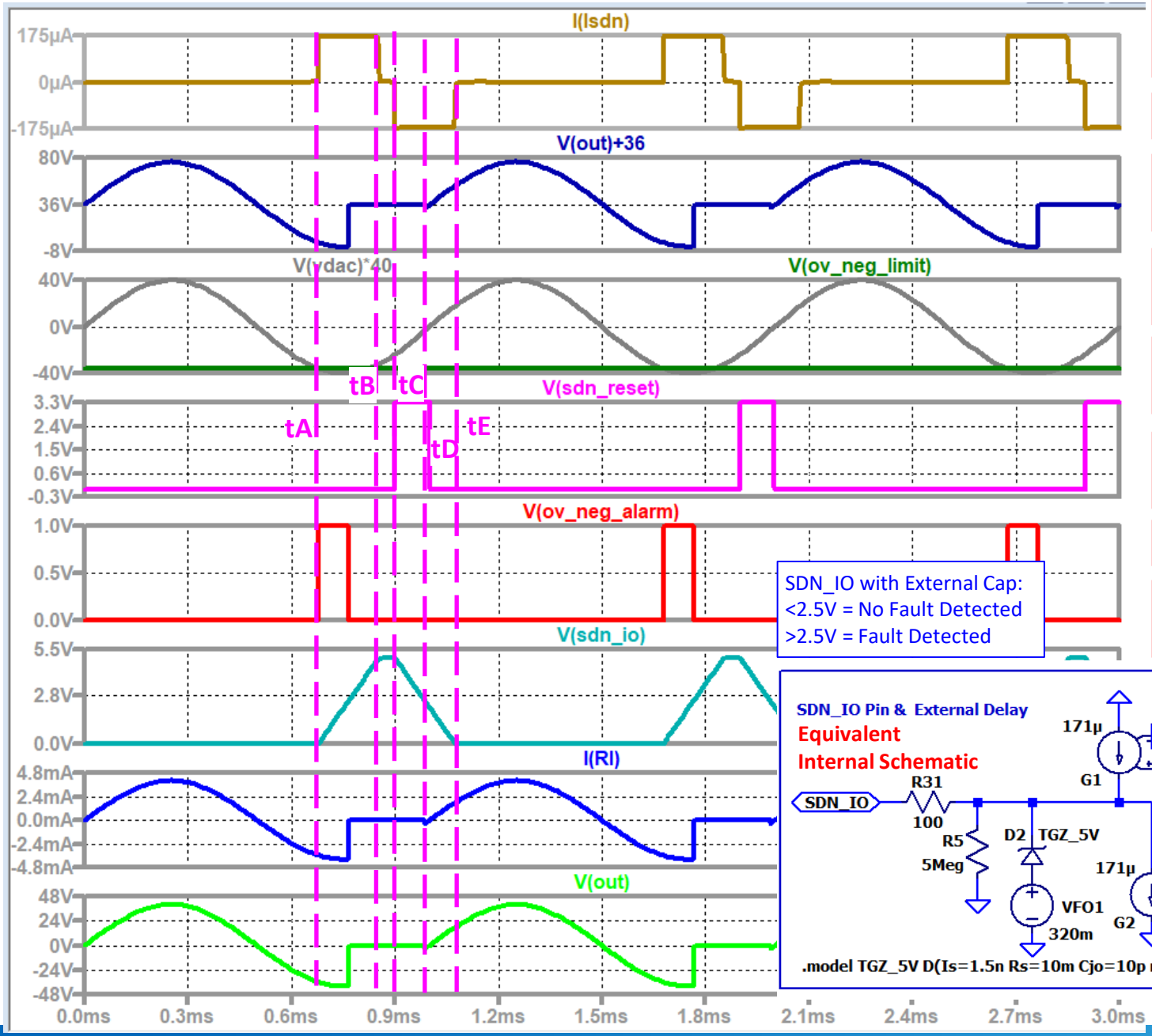
t3: SDN_IO < 2.5V and OV_NEG Fault Cleared

t3: Power Op Amp is enabled, and V(OUT) returns to V(VDAC)*40 and I(RL) returns to V(out)/RL

t4: SDN_IO discharges down to 0V

t5: Fault condition repeats – check over many cycles

SDN_IO Fault Detect Delay-*SDN_IO Current Sources*



SDN_IO with External Cap:
<2.5V = No Fault Detected
>2.5V = Fault Detected

Any time SDN_IO is not driven by a low impedance source externally, it is driven internally high, by a 170uA pull-up current source, or low, by a 170uA pull-down current source. SDN_IO is clamped internally: 0V≤ SDN_IO ≤ 5V.

For this test case SDN_IO has only capacitor, Csdn, connected externally.

tA: SDN_IO starts at 0V and is then driven high internally by OV_NEG Fault detect so 170uA pull-up current source sources out of SDN_IO.

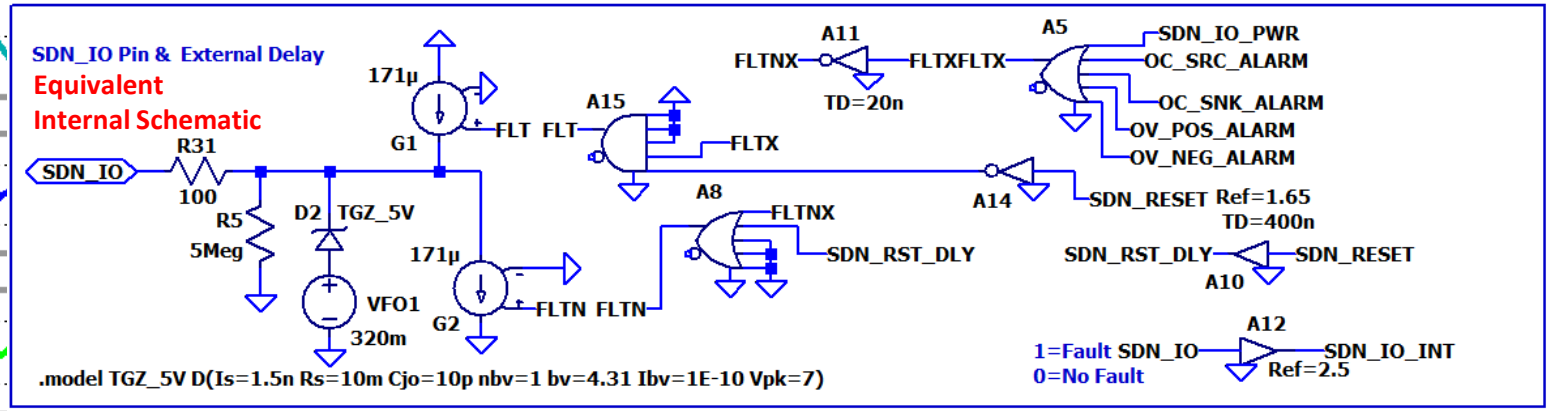
tB-tC: SDN_IO still driven high internally but clamped at 5V so current out of SDN_IO goes to zero.

tC-tD: SDN_IO starts at 5V and is then driven low internally, due to SDN_RESET pulsed high, so 170uA pull-down current source sinks into SDN_IO.

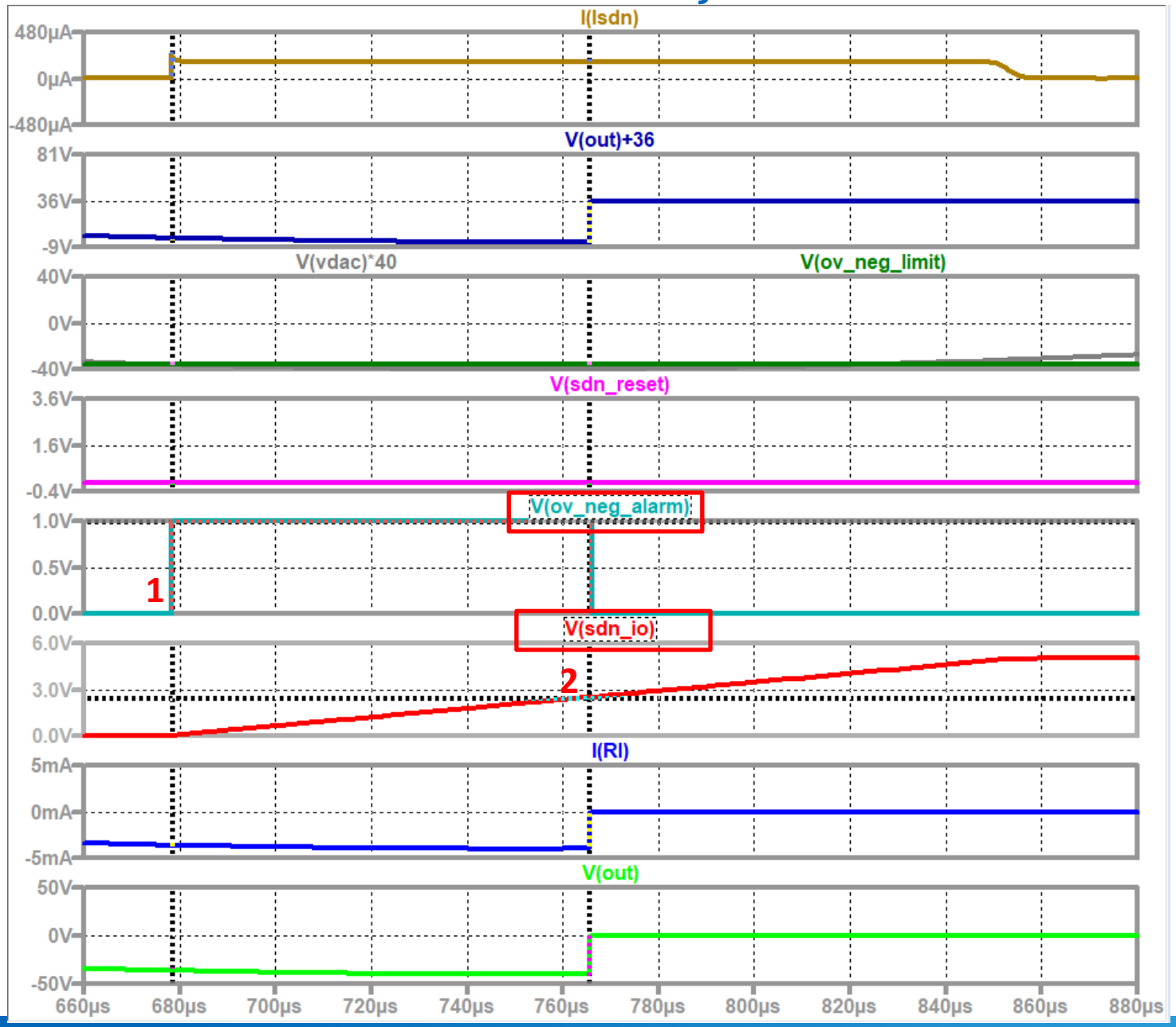
tD: SDN_IO < 2.5V and OV_NEG Fault Cleared and Power Op Amp is enabled, V(OUT) returns to V(VDAC)*40 and I(RL) returns to V(out)/RL

tD-tE: SDN_IO continues to discharge down towards 0V

tE: SDN_IO discharged down to 0V. SDN_IO still driven low internally but clamped at 0V so current out of SDN_IO goes to zero.



SDN_IO Fault Detect Delay



SDN_IO Delay Timing:

$$Isdn = Csdn * \frac{\Delta Vsdn}{\Delta tdly}$$

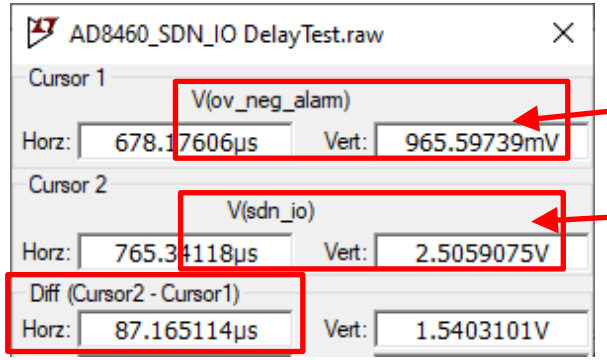
$$Csdn = \frac{170\mu A * tdly}{2.5V}$$

$$tdly = \frac{2.5V * Csdn}{170\mu A}$$

$$tdly = \frac{2.5V * 6nF}{170\mu A} = 88.235\mu s$$

SDN_IO with External Cap:
<2.5V = No Fault Detected
>2.5V = Fault Detected

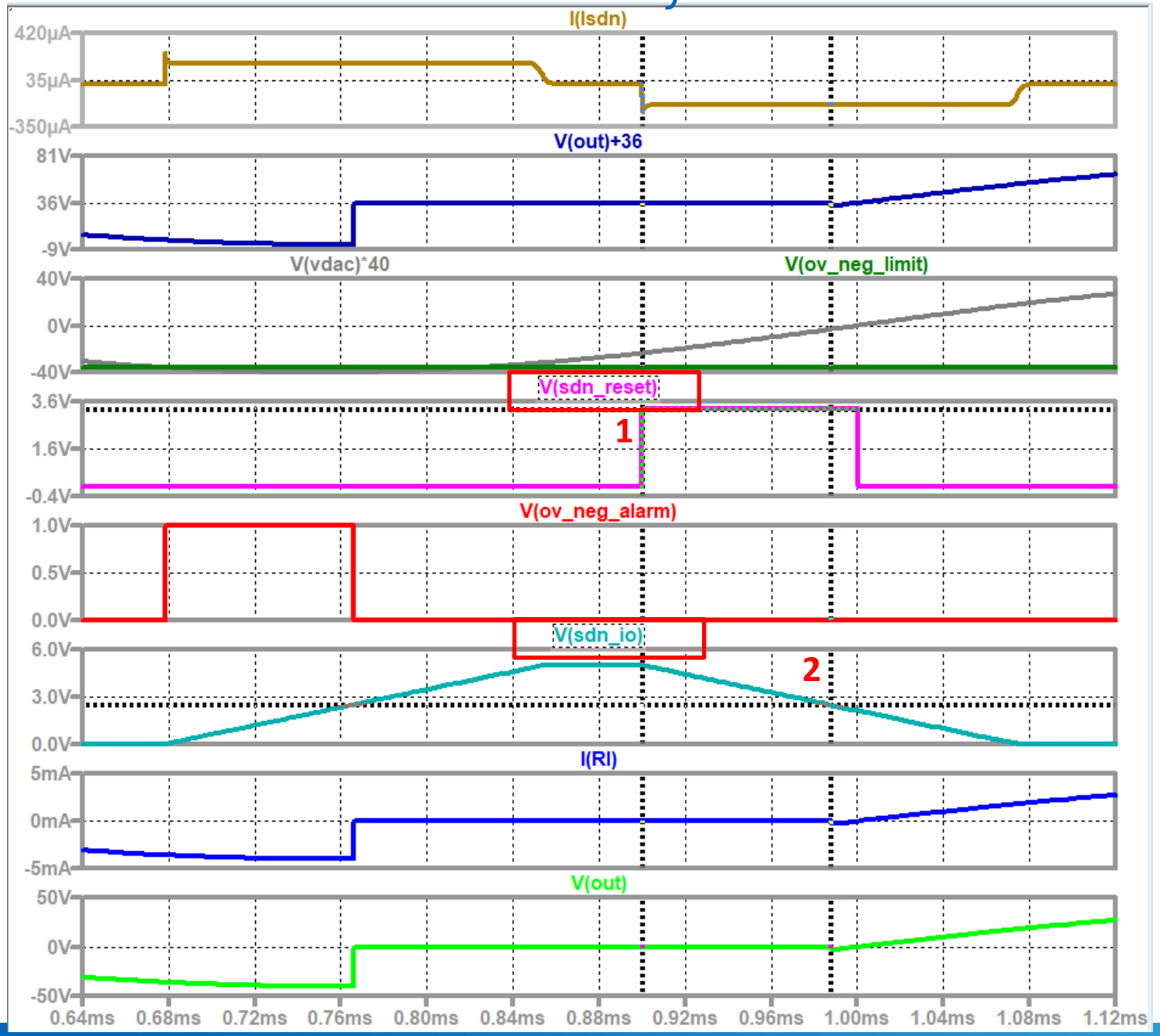
Diff (Cursor2-Cursor1) delta gives us ***the delay from V(OV_NEG_ALARM) going high and SDN_IO >2.5V***
Ideally Should be 88.235us, Sim shows 87.165us.
Small leakage currents and over/under shoots will alter slightly the currents out of SDN_IO. Internal Fault Detect Timing delays will also contribute slightly to the accuracy of this delay.



As close to 0V to 1V step as possible.

As close to 2.5V as possible.

SDN_IO Fault Detect Delay



SDN_IO Delay Timing:

$$Isdn = Csdn * \frac{\Delta Vsdn}{\Delta tdly}$$

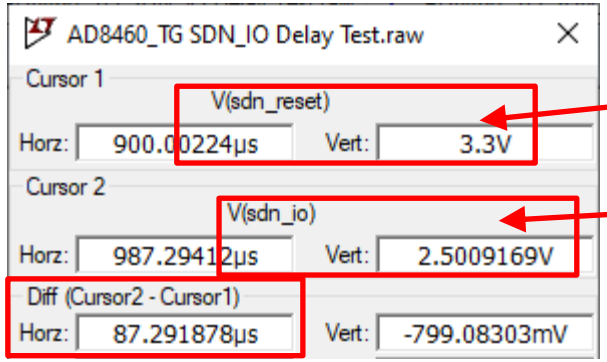
$$Csdn = \frac{170\mu A * tdly}{2.5V}$$

$$tdly = \frac{2.5V * Csdn}{170\mu A}$$

$$tdly = \frac{2.5V * 6nF}{170\mu A} = 88.235\mu s$$

SDN_IO with External Cap:
<2.5V = No Fault Detected
>2.5V = Fault Detected

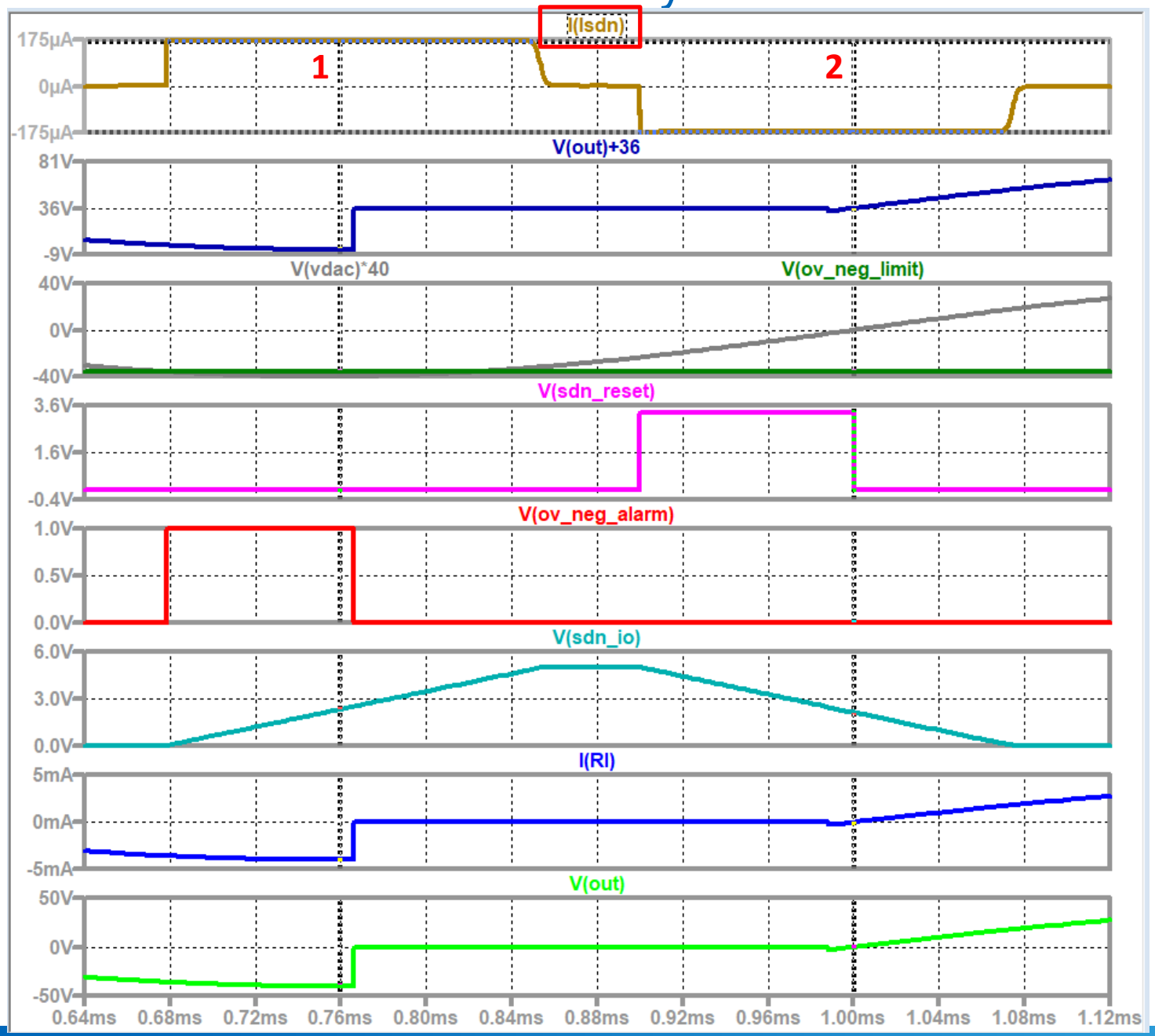
Diff (Cursor2-Cursor1) delta gives us the ***delay from V(SDN_RESET) going high and SDN_IO <2.5V***
Ideally Should be 88.235us, Sim shows 87.292us.
Small leakage currents and over/under shoots will alter slightly the currents out of SDN_IO. Internal Fault Detect Timing delays will also contribute slightly to the accuracy of this delay.



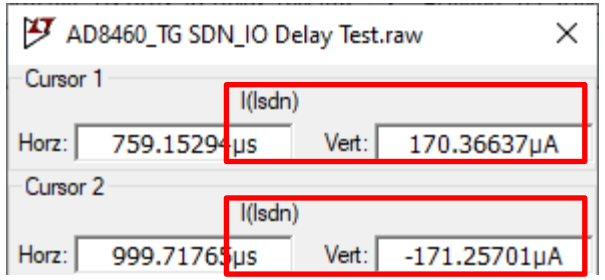
0V to 3.3V step as possible

As close to 2.5V as possible.

SDN_IO Fault Detect Delay



Cursor 1: SDN_IO source current check.
Should be 170uA.



SDN_IO with External Cap:
<2.5V = No Fault Detected
>2.5V = Fault Detected

Cursor 2: SDN_IO sink current check.
Should be -170uA.

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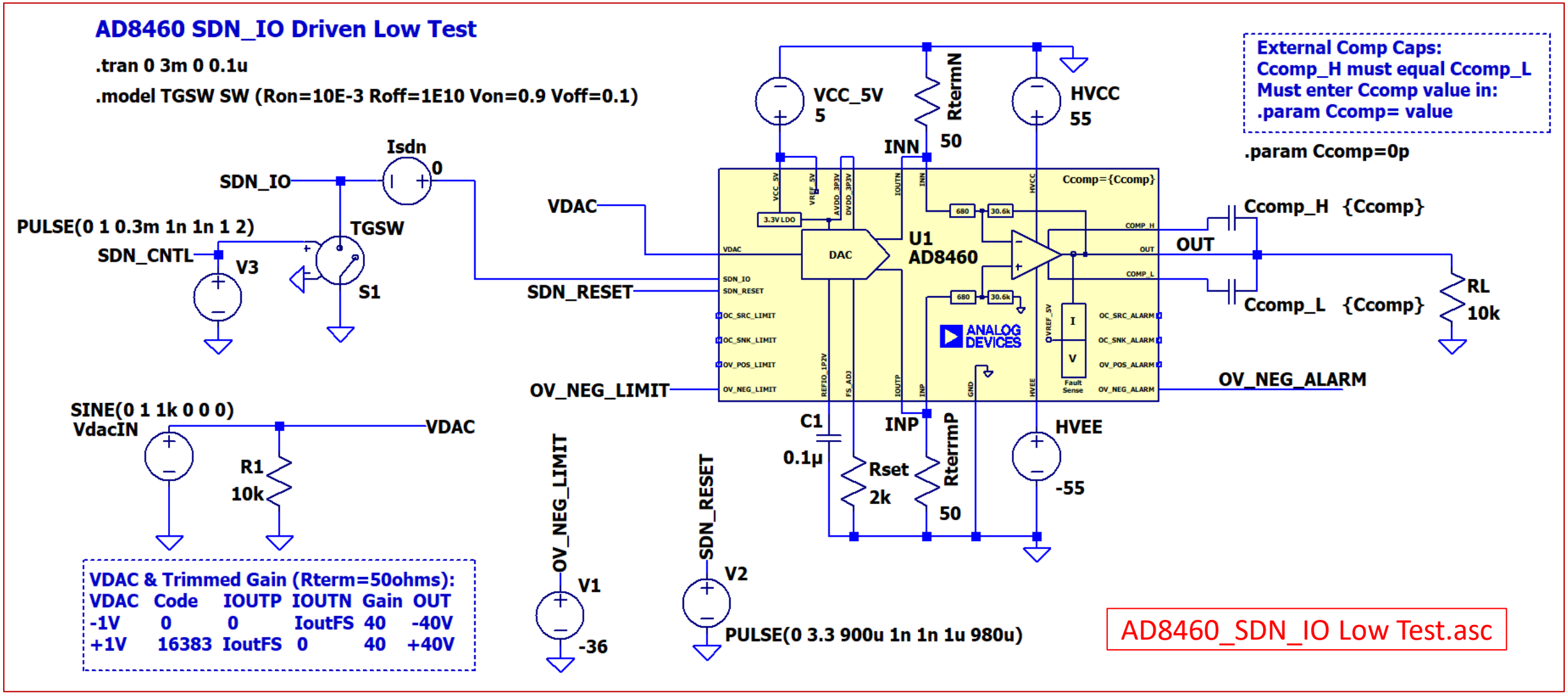
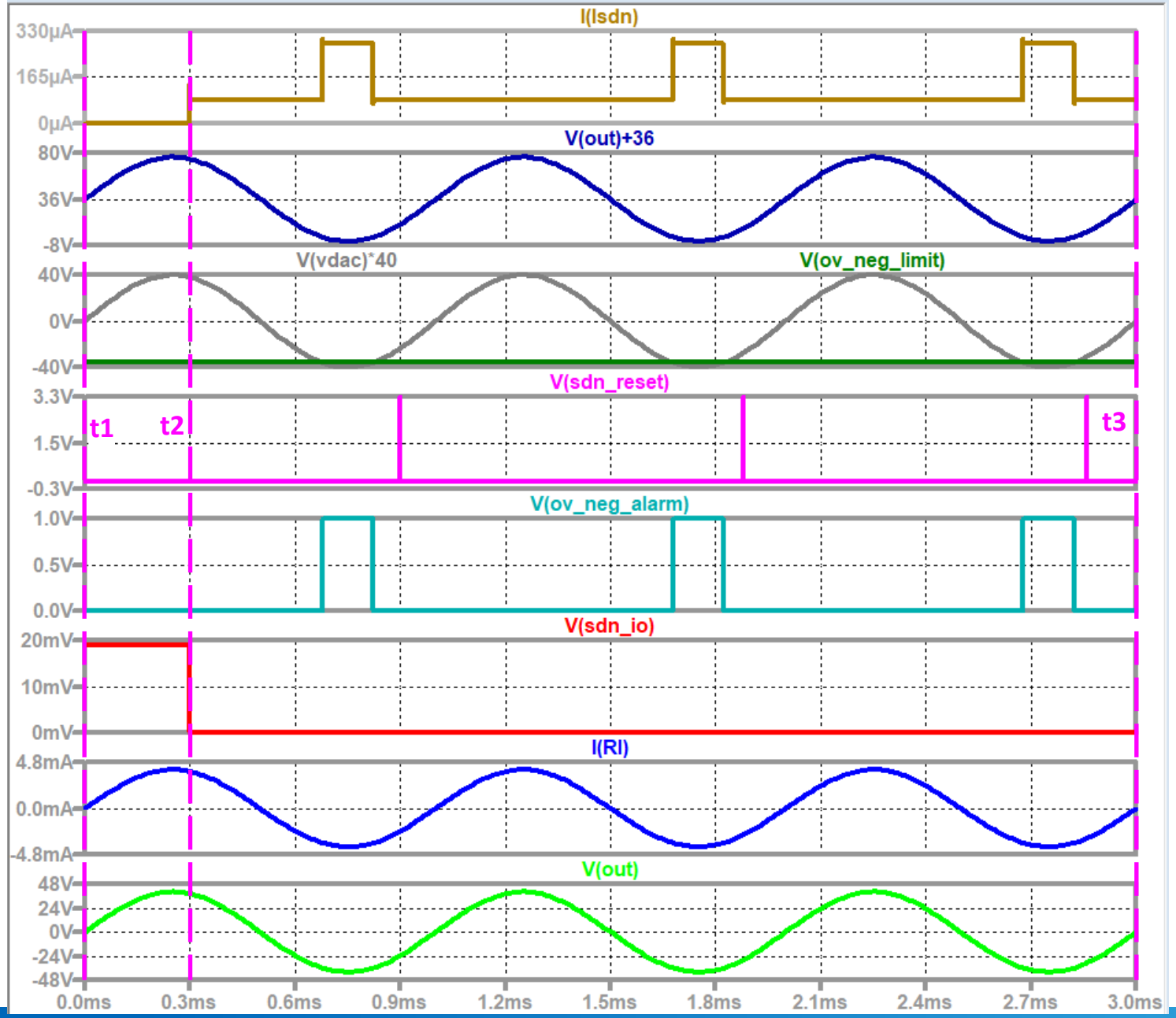
SDN_IO Externally Driven Low



SDN_IO Externally Driven Low



***SDN_IO* Held Low**

SDN_IO forced low means Power Op Amp is always enabled, regardless of any faults.

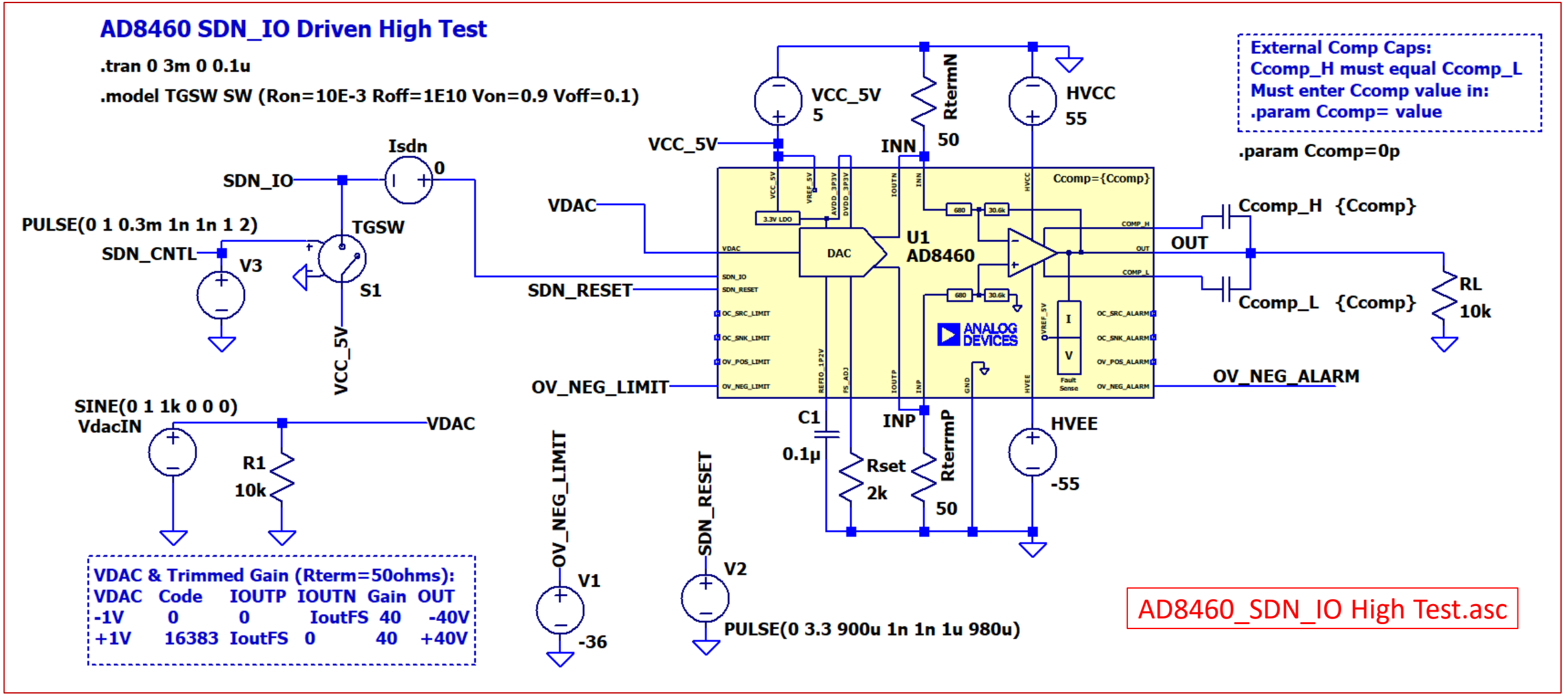
t1: V(SDN_IO) is externally high impedance and so it is internally pulled down close to GND (20mV).

t2: V(SDN_IO) is externally driven to GND with a low on-resistance switch.

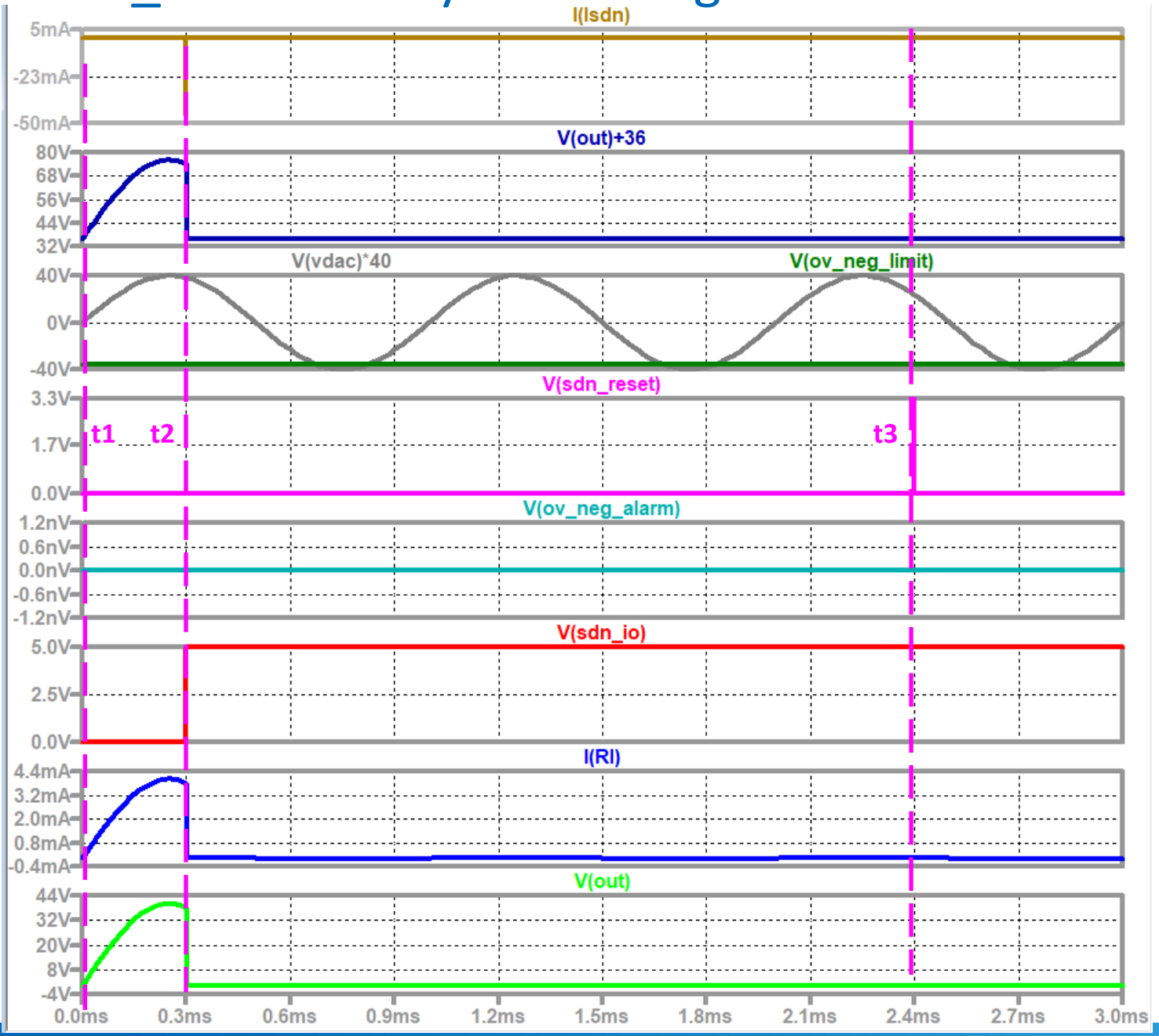
t2-t3: V(SDN_IO) is externally held at GND with a low on-resistance switch. V(OV_NEG_ALARM) going high shows many OverVoltage Negative Faults but the Power Op Amp stays enabled, as seen by correct waveforms on V(OUT) and I(RL).

SDN_IO:
0V = No Fault Detected
5V = Fault Detected

SDN_IO Externally Driven High



SDN_IO Externally Driven High



***SDN_IO* Held High**

SDN_IO forced high means Power Op Amp is always disabled, regardless of any faults.

t1: V(SDN_IO) is externally high impedance and so it is internally pulled down close to GND (20mV).

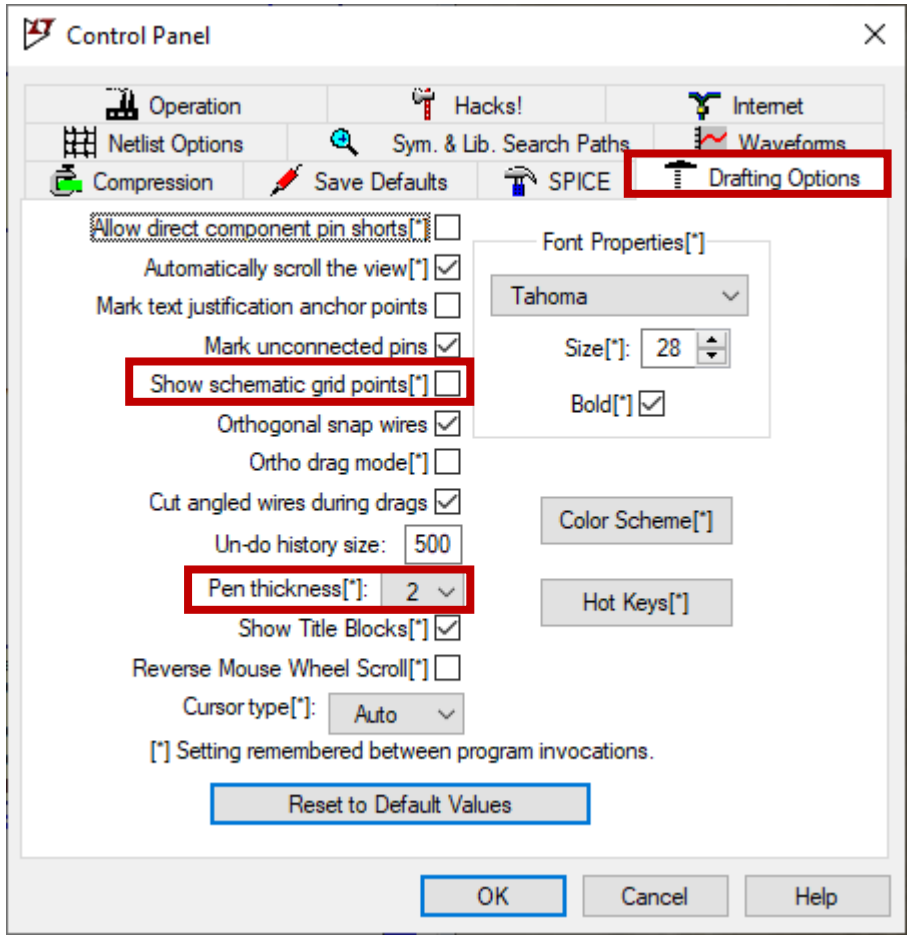
t2: V(SDN_IO) is externally driven to 5V with a low on-resistance switch. Power Op Amp is disabled as seen on I(RL) and V(OUT) going to zero.

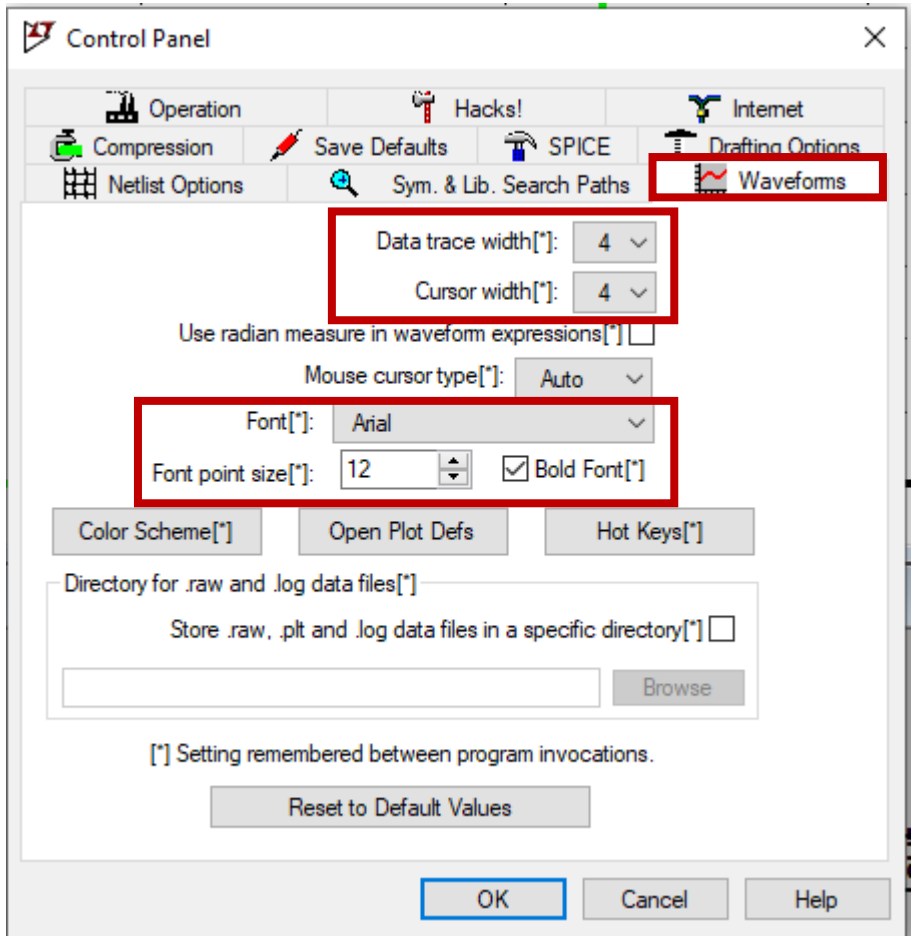
t3: V(SDN_RESET) is pulsed high which has no effect on enabling Power Op Amp since SDN_IO is forced high.

SDN_IO:
0V = No Fault Detected
5V = Fault Detected

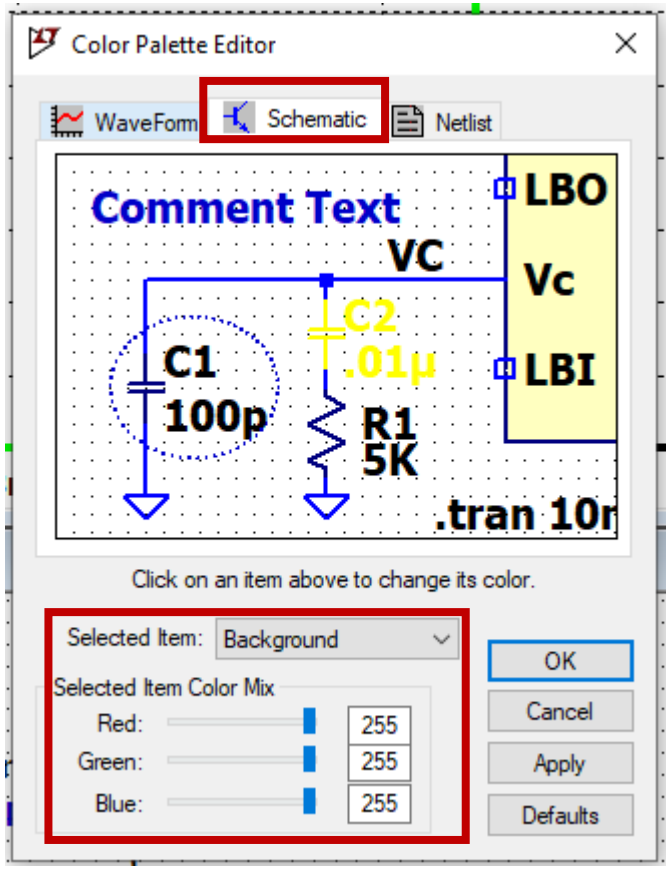
Appendix:
LTspice Schematic and Plot Images

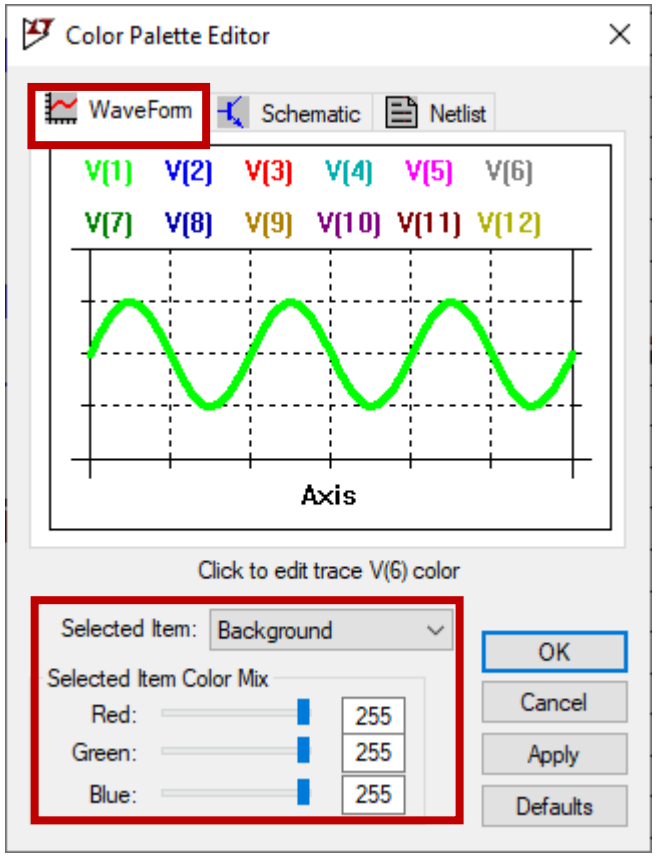
LTspice Schematic & Plot Settings for Images in this Presentation





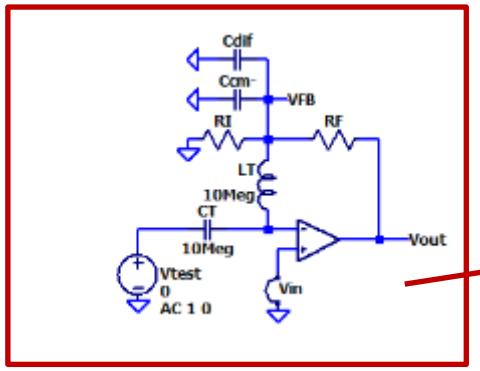
LTspice Schematic & Plot Settings for Images in this Presentation



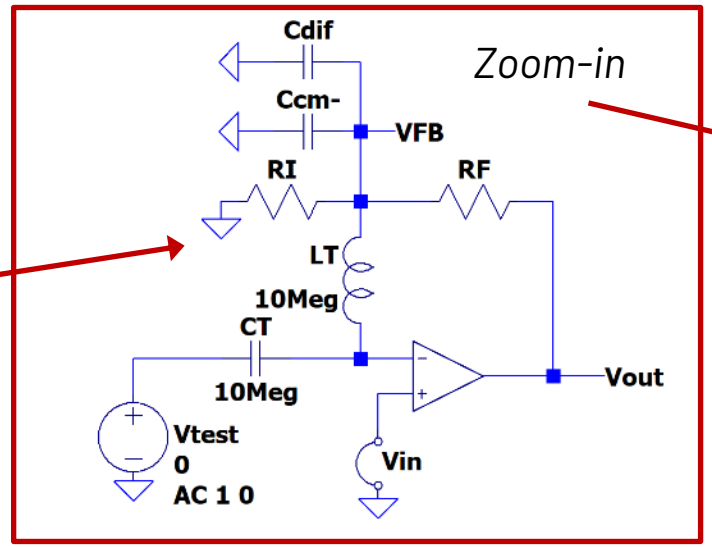


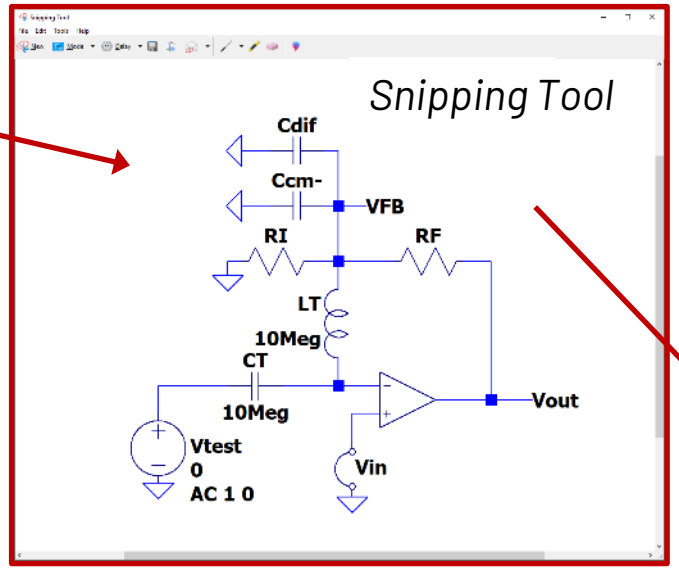
LTspice Schematic & Plot Settings for Images in this Presentation

***For best image resolution**, Zoom-in on Desired Final Image, use Snipping Tool to copy Zoom-in image, paste as Bitmap or Device Independent Bitmap into document.*

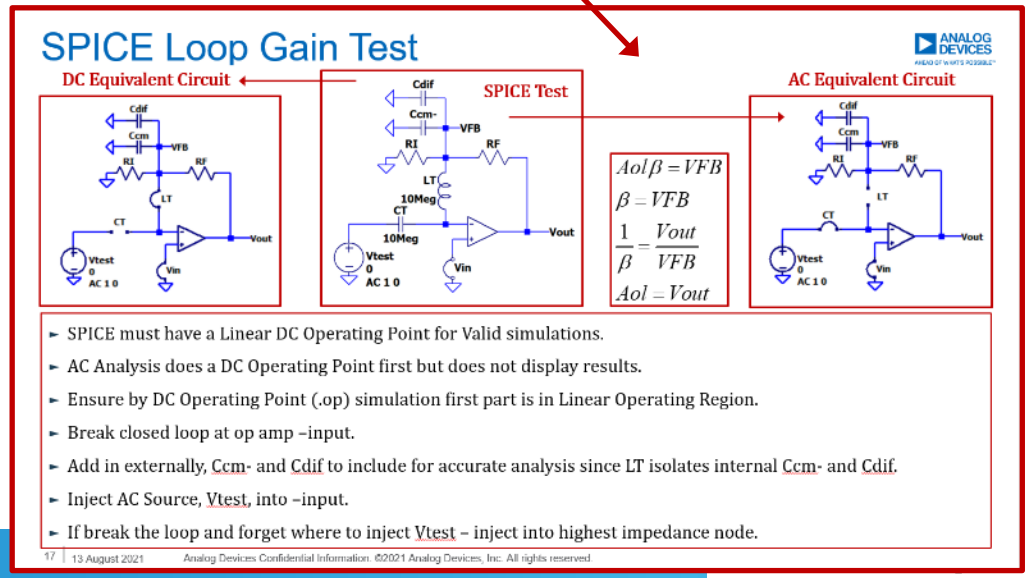


Desired Final Image



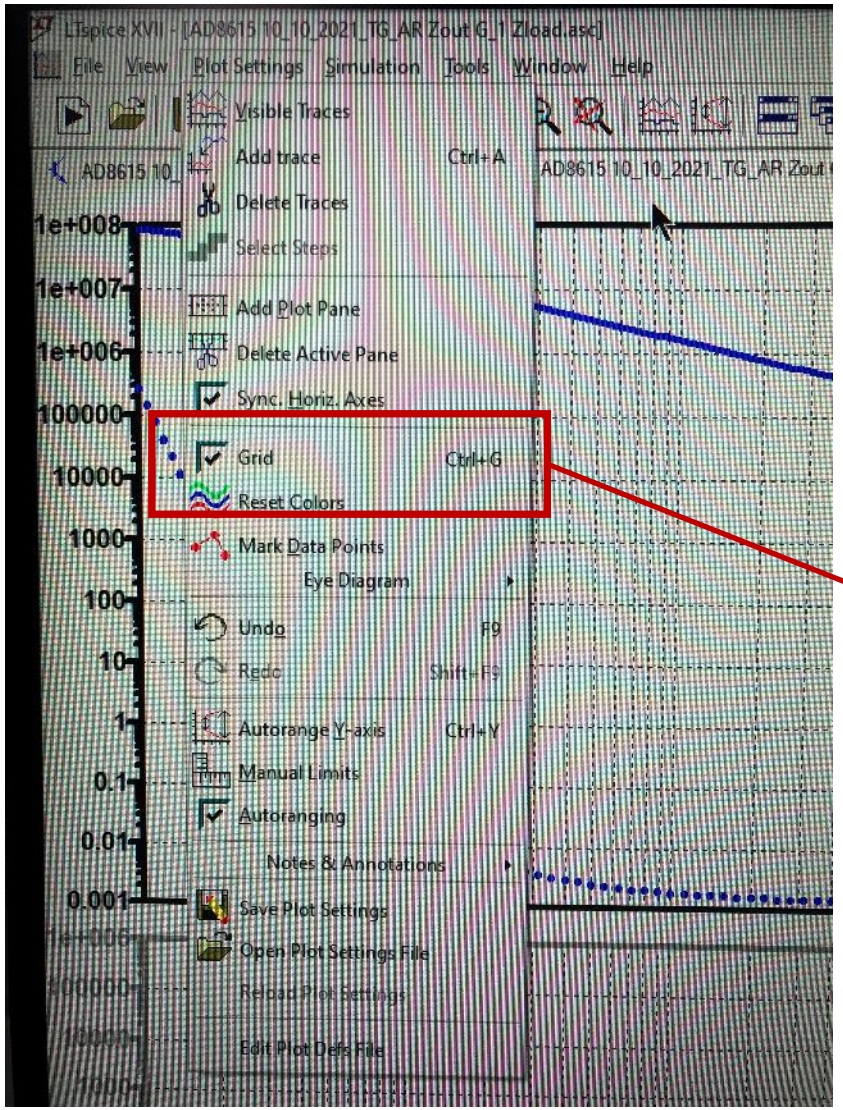


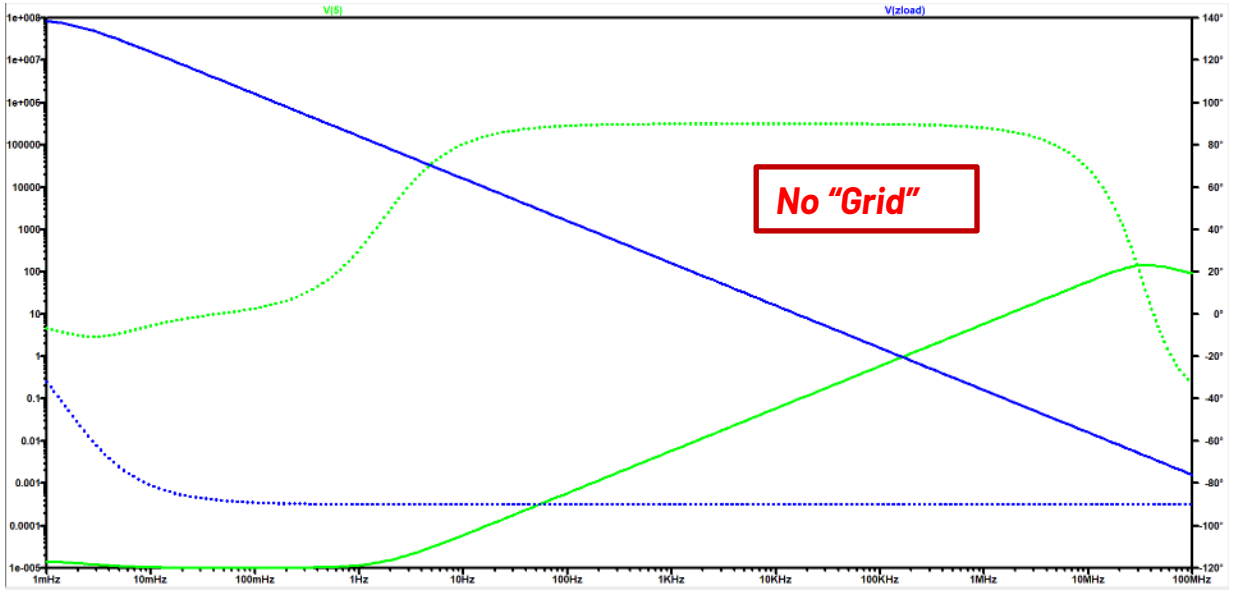
Paste into Document as Bitmap or Device Independent Bitmap and re-size as desired

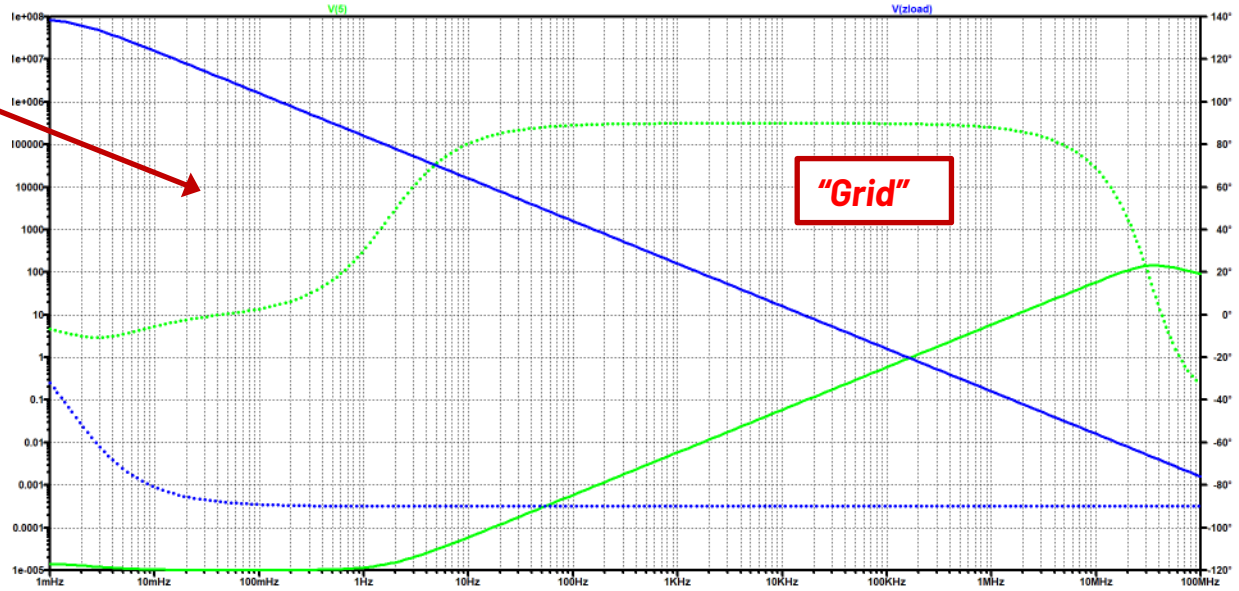


LTspice Schematic & Plot Settings for Images in this Presentation

"Plot Settings" → Turn "Grid" ON.





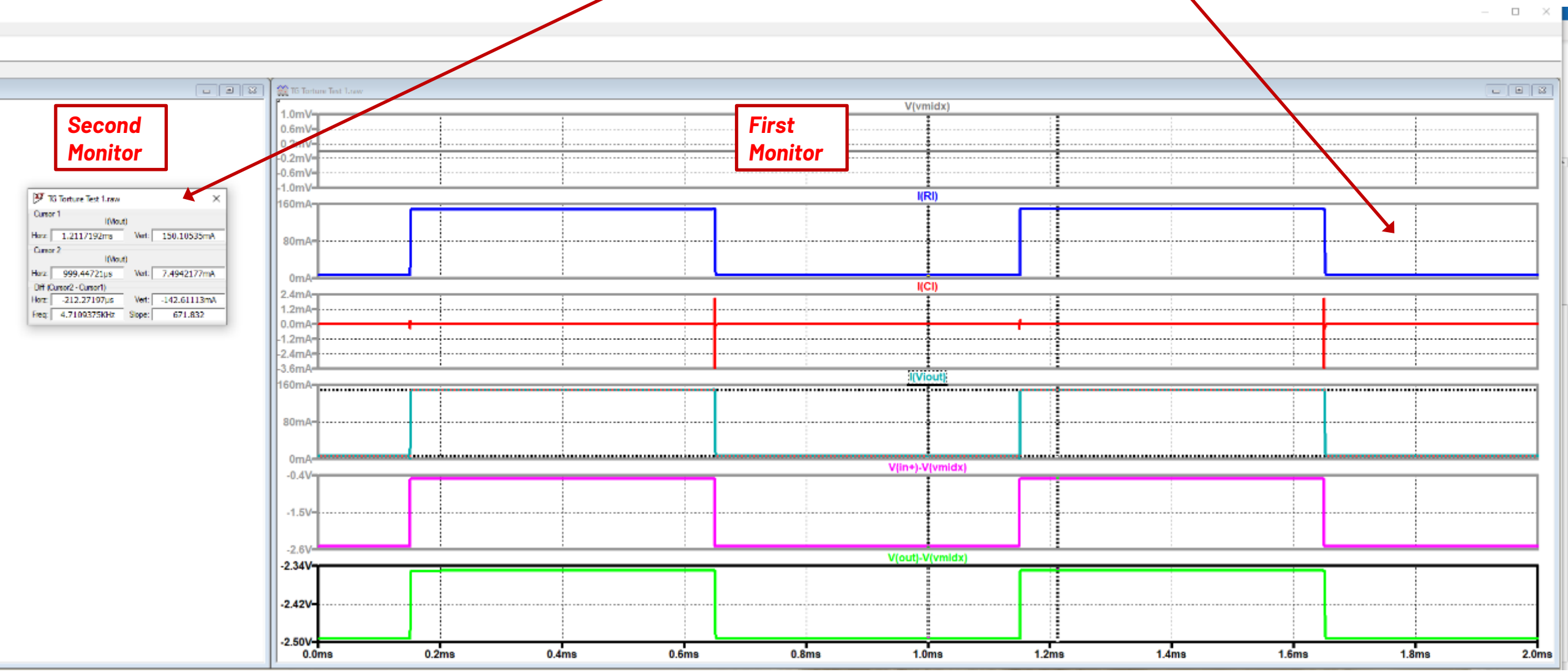


LTspice Schematic & Plot Settings for Images in this Presentation

Do NOT "Snippet Image" with Cursor window on plot. Move Cursor window off-screen and copy just plot window with waveforms

Second Monitor

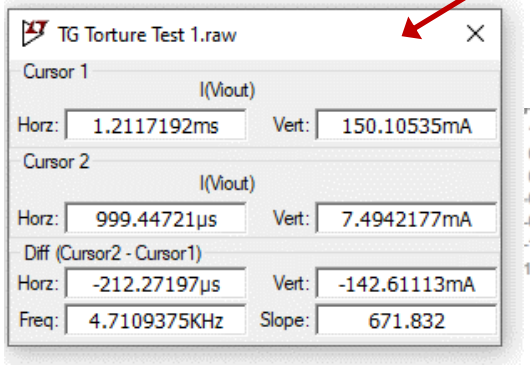
First Monitor

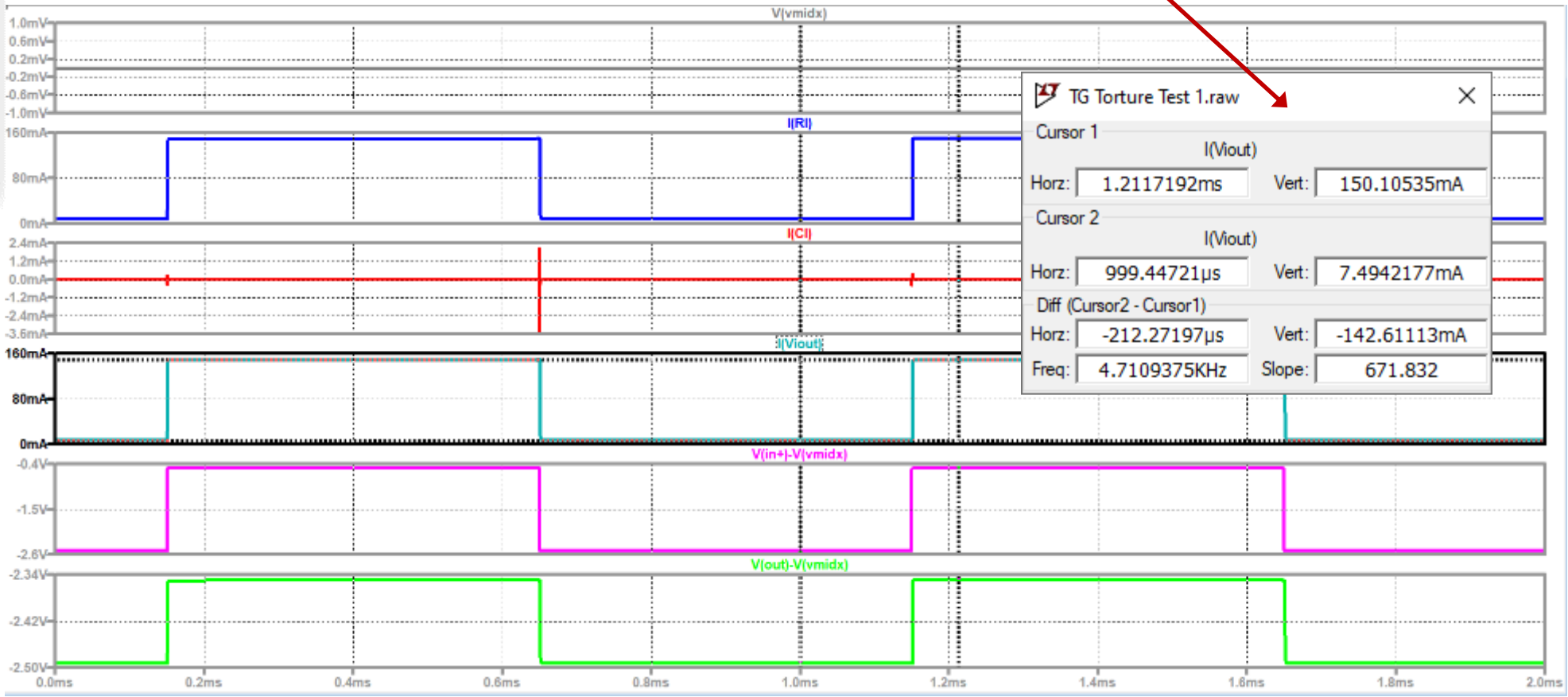


LTspice Schematic & Plot Settings for Images in this Presentation

Click on pop-up cursor window and use "ALT+PRNT SCRN" to copy cursor pop-up window.

Use "CTRL+V" to paste into Word, PowerPoint.
Re-size as desired for best clarity.





LTspice Schematic & Plot Settings for Images in this Presentation

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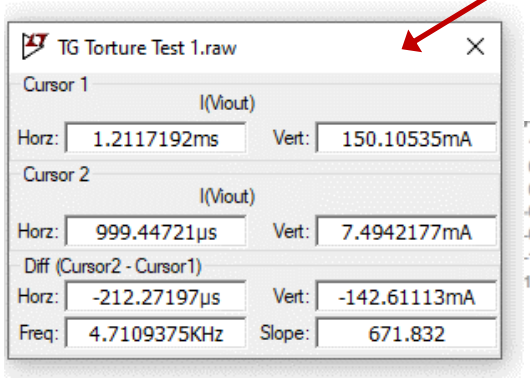
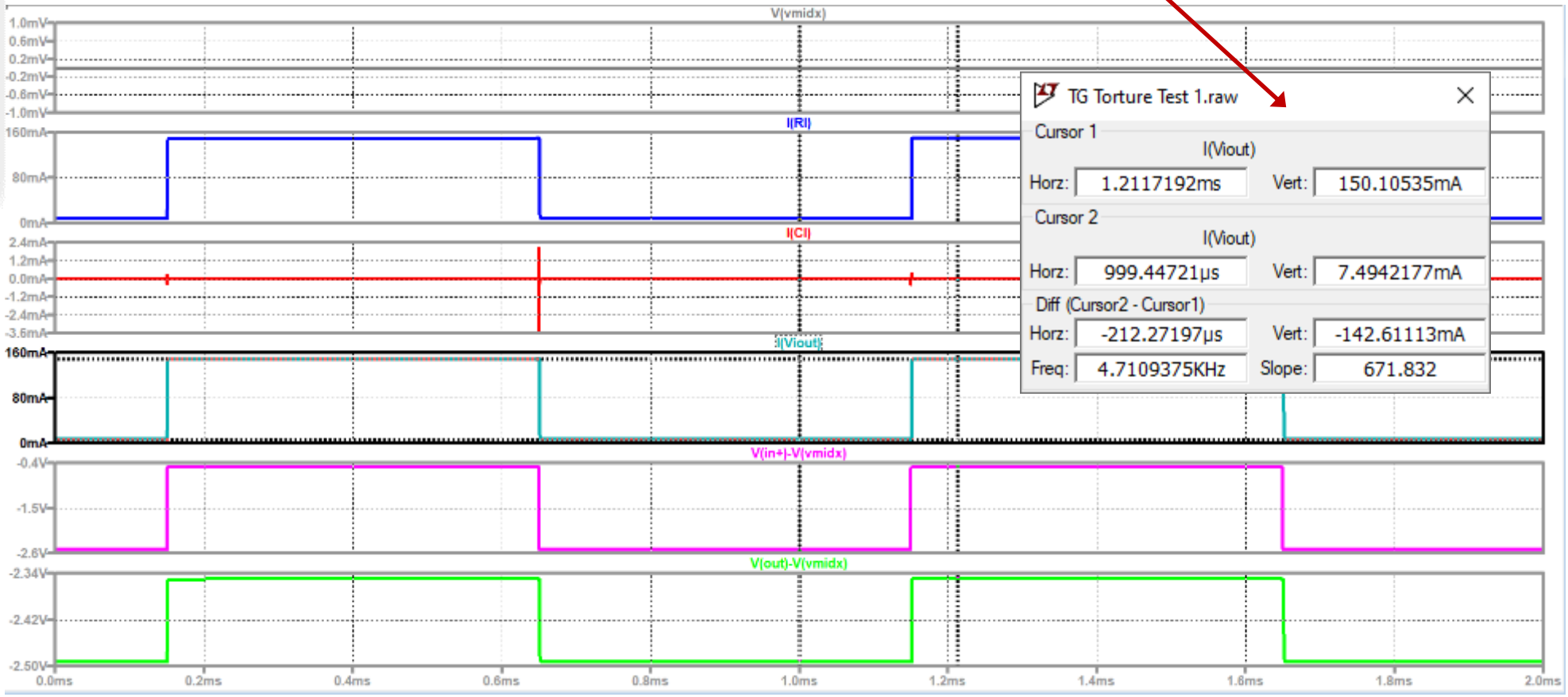
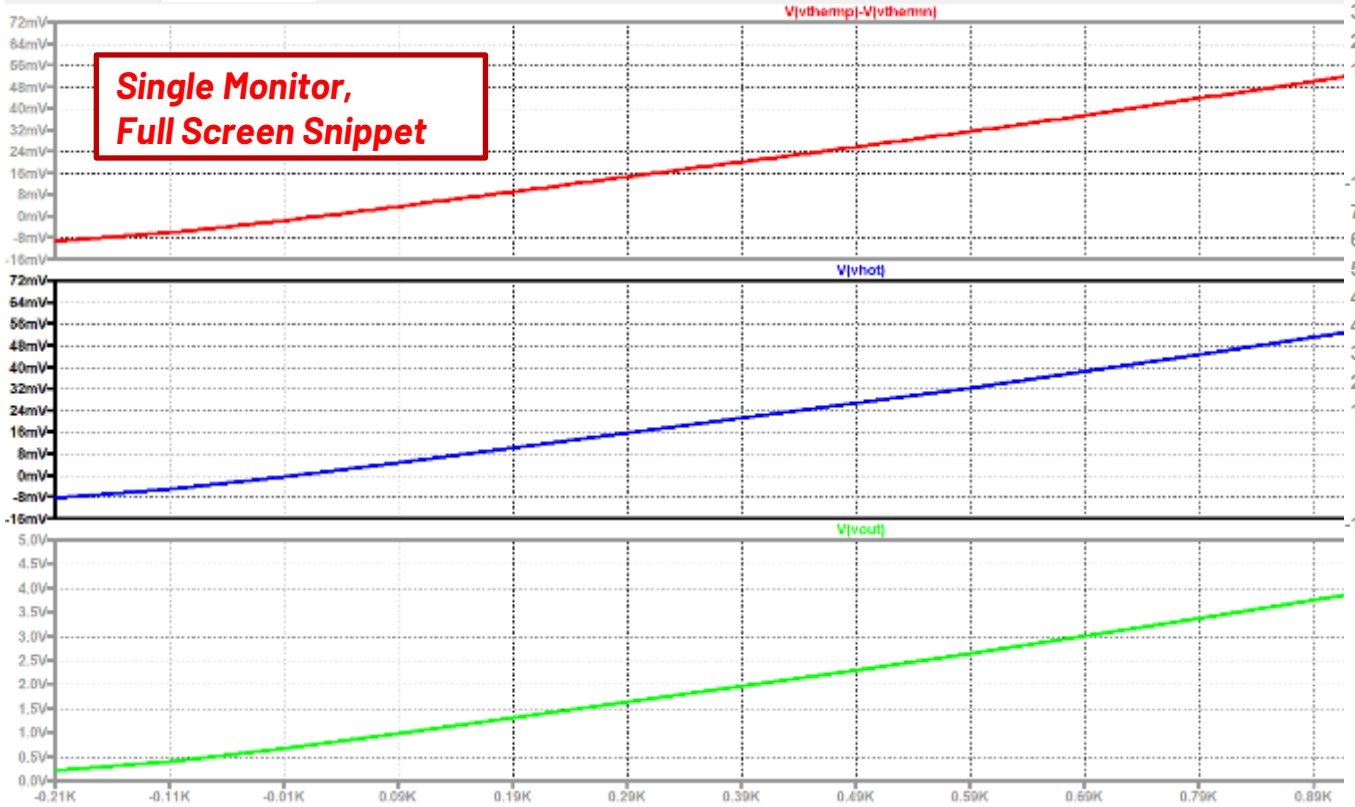




LTspice Schematic & Plot Settings for Images in this Presentation

Sometimes a Snippet image is better captured not on a Single Monitor Full Screen Snippet BUT rather use a Single Monitor, Window, Tile Vertically Snippet of the Plot Window.

Single Monitor,
Full Screen Snippet



Single Monitor, Window,
Tile Vertically Snippet