AD7401 HDL Driver

Revision history

Date	Rev	Description
2/19/2013	0.1	Document creation

Contents

1. Introduction

This document describes the HDL driver for the AD7401 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

2. Architecture

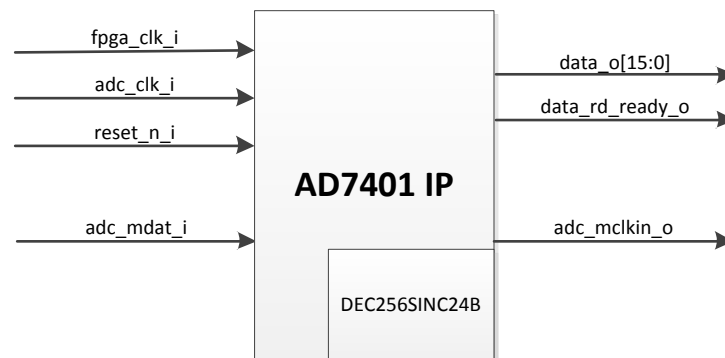Fig. 1 presents the block diagram of the AD7401 IP.

Fig. 1 AD7401 IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input.
ADC_CLK_I	IN	1	Clock to be sent to the AD7401
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
DATA_O	OUT	16	Outputs the data read from the ADC.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7401. The IP continuously reads the conversion results from the AD7401 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
Ad7401 control and data ports			
ADC_MDAT_I	IN	1	The single bit modulator output is supplied to this pin as serial data stream. The bits are clocked out on the rising edge of the ADC_MCLKOUT_I pin and are valid on the following MCLKOUT rising edge
ADC_MCLKIN_O	OUT	1	Master clock logic input of the AD7401. The bit stream from the modulator is valid on the rising edge of MCLKIN.

Table 1 IO ports
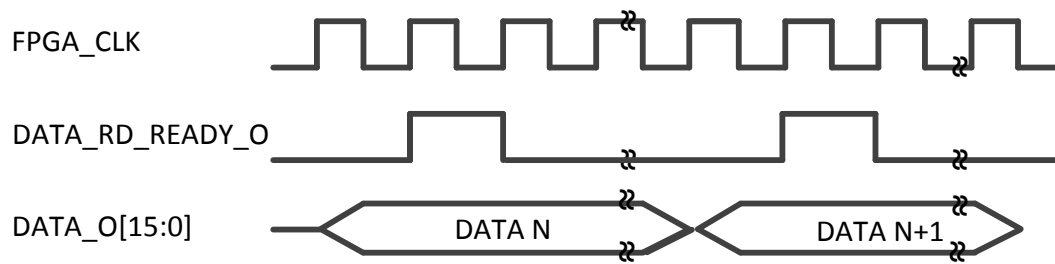
Fig. 2 presents the timing diagram for read operations.

Fig. 2. Read operations timing diagram

DEC256SINC24B submodule

The DEC256SINC24B module is a submodule of AD7401 and it implements the SINC3 filter needed for acquiring the data. The implementation is described in the AD7401 datasheet.