

## **AD7091R HDL Driver**

### **Revision history**

<b>Date</b>	<b>Rev</b>	<b>Author</b>	<b>Description</b>
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## 1. Introduction

This document describes the HDL driver for the AD7091R part. The driver is written in Verilog and can be integrated in designs with or without softcores.

## 2. Architecture

Fig. 1 presents the block diagram of the AD7091 IP.

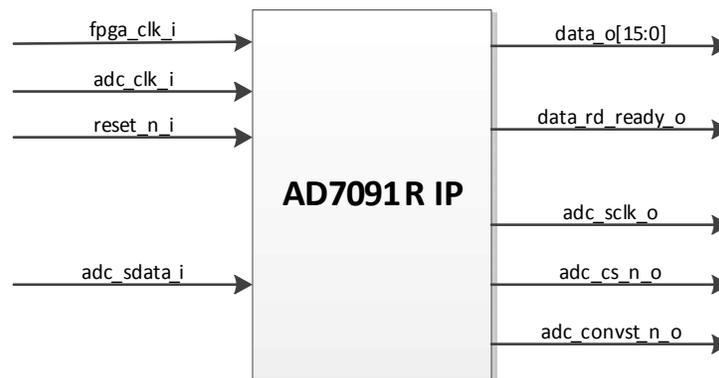


Fig. 1 AD7091R IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
<i>Clock and reset ports</i>			
FPGA_CLK_I	IN	1	Main clock input.
ADC_CLK_I	IN	1	Clock to be sent to the ADC during the conversion process.
RESET_N_I	IN	1	Active low reset signal.
<i>IP control and data ports</i>			
DATA_O	OUT	16	Outputs the data read from the ADC and the channel ID to which the read data corresponds. The channel ID is stored on the 4 most significant bits and the read data is stored on the 12 least significant bits.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7091. The IP continuously reads the conversion results from the AD7091 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
<i>Ad7091 control and data ports</i>			
ADC_SDATA_I	IN	1	ADC Serial Data Output. The conversion result is output on this pin. It is synchronized to SCLK.
ADC_SCLK_O	OUT	1	ADC Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.

ADC_CS_N_O	OUT	1	ADC Chip Select. The serial bus is enabled when CS is held low and CS is used to frame the output data on the SPI.
ADC_CONVST_N_O	OUT	1	ADC Convert Start. This is an edge triggered logic input. The falling edge of CONVST place the track-and-hold into hold mode and initiates a conversion.

Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

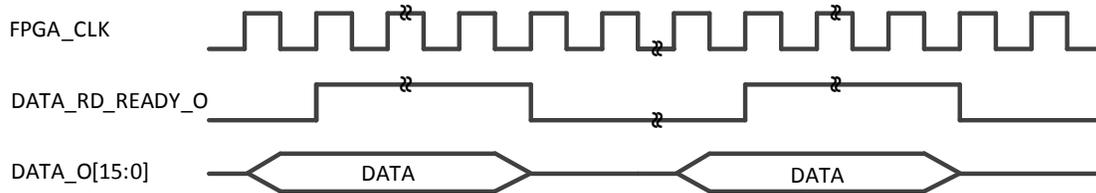


Fig. 2. Read operations timing diagram

**Note:** The driver is intended to be used for AD7091R ADCs configured without busy indicator.