AD7492 HDL Driver

Revision history

Date	Rev	Description
05.03.2012	0.1	Document creation

Contents

1. Introduction

This document describes the HDL driver for the AD7492 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

2. Architecture

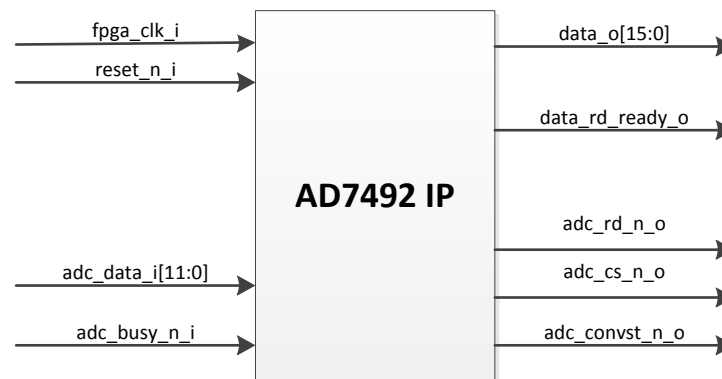Fig. 1 presents the block diagram of the AD7492 IP.

Fig. 1 AD7492 IP

Table 1 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input.
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
DATA_O	OUT	16	Outputs the data read from the ADC. The first most significant 4 bits are always 0.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7492. The IP continuously reads the conversion results from the AD7492 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
Ad7492 control and data ports			
ADC_DATA_I	IN	12	ADC Data Bits. Parallel digital inputs that provide the conversion result for the part.
ADC_BUSY_N_I	IN	1	BUSY input. Logic input indicating the status of the conversion process. The BUSY signal goes high after the falling edge of ADC_CONVST_N_O and stays high for the duration of the conversion. Once the conversion is complete and the conversion result is in the output register, the BUSY

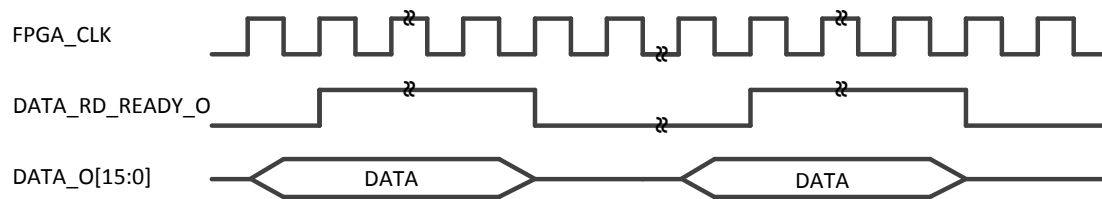|			
			line returns low. The track/hold returns to track mode just prior to the falling edge of BUSY and the acquisition time for the part begins when BUSY goes low.
ADC_RD_N_O	OUT	1	ADC Read. Logic output used in conjunction with ADC_CS_N_O to access the conversion result. The conversion result is placed on the data bus following the falling edge of both ADC_CS_N_O and ADC_RD_N_O. The two signals are connected to the same AND gate.
ADC_CS_N_O	OUT	1	ADC Chip Select. Active low logic output used in conjunction with ADC_RD_N_O to access the conversion result.
ADC_CONVST_O	OUT	1	ADC Conversion Start. Logic output used to initiate conversion on AD7492.

Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

Fig. 2. Read operations timing diagram