



AHEAD OF WHAT'S POSSIBLE™

Stability Analysis of Voltage Feedback Opamps

Ed Mullins, Principal Applications Engineer

What do you want to get out of this training?

What do I want to get out of this training?

- ▶ To help you achieve your objectives
- ▶ To “Train the Trainer”
- ▶ To allow each of you to have higher levels of engagement with your customers
- ▶ To create a closer partnership between the field and the PAG BU
- ▶ To be invited to virtually attend an occasional customer visit at your discretion – I am always available – please take advantage of me
- ▶ My ultimate goal is to increase ADI’s market share and profitability, and have plenty of fun along the way

Who Can Benefit from this type of Training

▶ ADI Employees:

- FAE's, Sales, Mgt, Recent Hires, New in Role

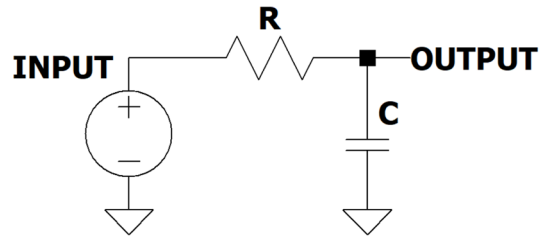
▶ Customers:

- New and Recent College Grads
- Experienced Engineers who need a refresher
- Engineers new to the company or role
- Experienced engineers who do not need this training, yet if they attend, they will be identified as the internal experts, your "go-to" people

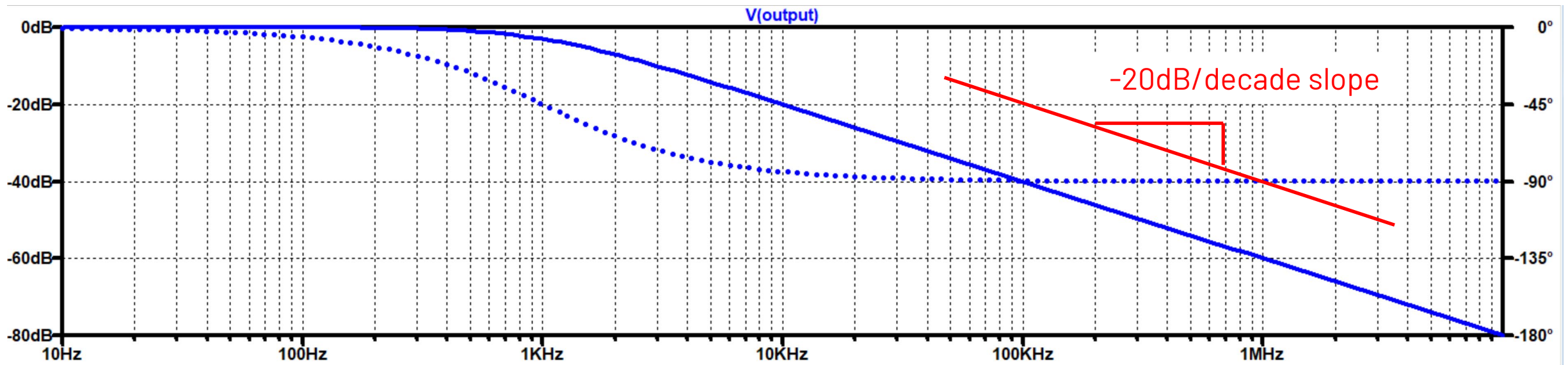
- ▶ Review of Bode Plots
 - Magnitude and Phase Response
- ▶ Voltage Feedback Model
 - Definitions
 - Analysis of Closed Loop Gain
 - Stability Criteria
 - Rate of Closure
- ▶ Opamp Gain and Phase
 - Ideal
 - Actual
- ▶ Phase Margin
 - Definition and examples
- ▶ Putting it All Together
 - Apply the concepts to plot A_{ol} and A_{cl} to determine level of stability in any opamp circuit : Step-by -Step
 - Practical Example 1: Transimpedance amplifier
 - Practical Example 2: Driving Capacitive Loads
 - LTSPICE Simulation Techniques
- ▶ Wrapping Up
 - Discussion, Q/A

Bode Plot Review

Rule of Thumb
- 3dB and 45° of phase shift occurs at each pole frequency
-20dB/decade slope



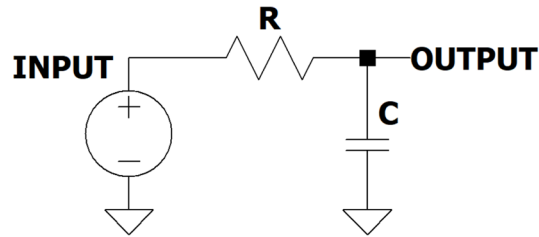
$$f_{3dB} = \frac{1}{2\pi RC}$$



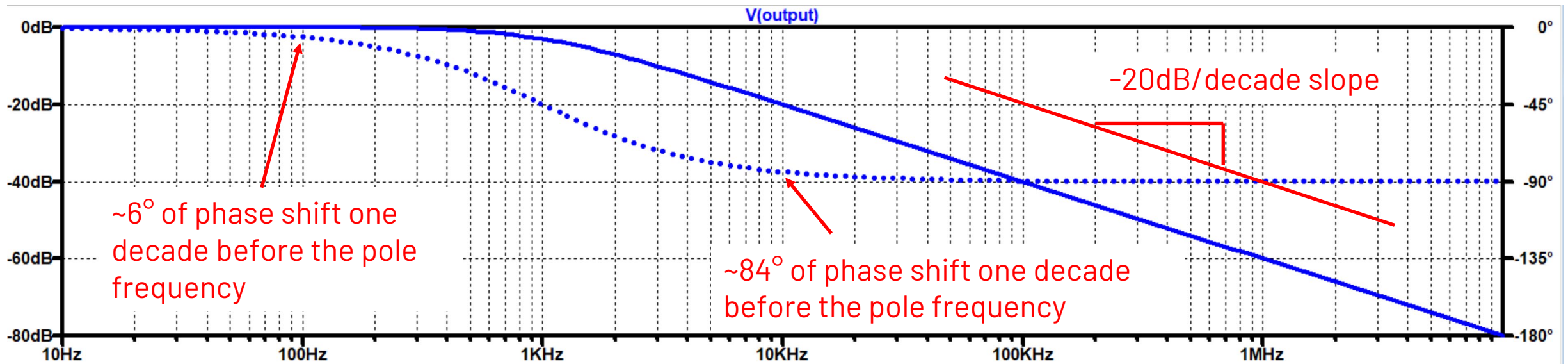
Bode Plot Review

Rule of Thumb

0° phase shift occurs *one decade* before and 90° occurs *one decade* after the pole frequency

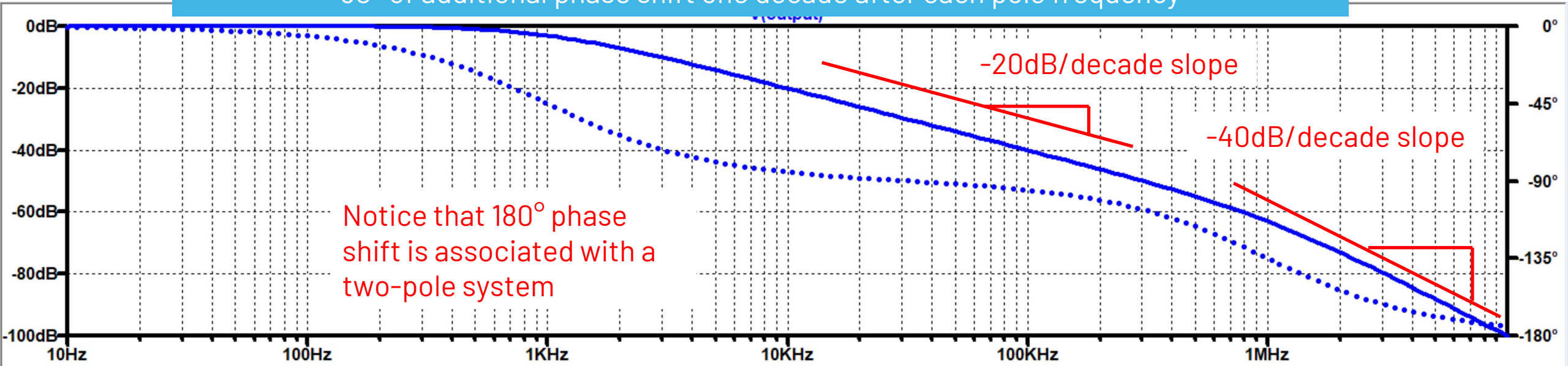


$$f_{3dB} = \frac{1}{2\pi RC}$$



Let's Add a Second Pole

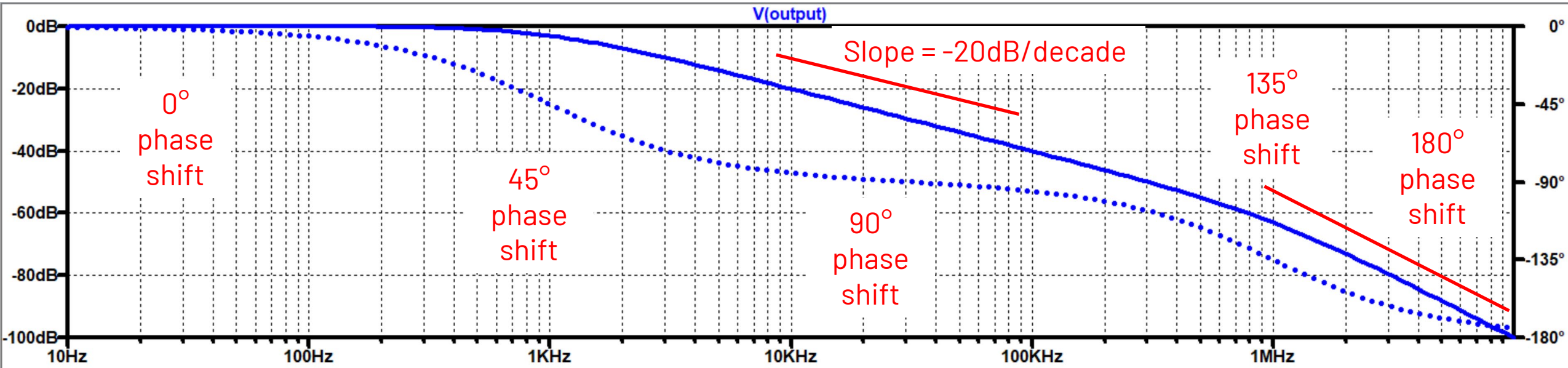
Rules of Thumb
45° of phase shift at each pole frequency
0° phase shift one decade before the pole frequency
90° of additional phase shift one decade after each pole frequency



Notice that 180° phase shift is associated with a two-pole system

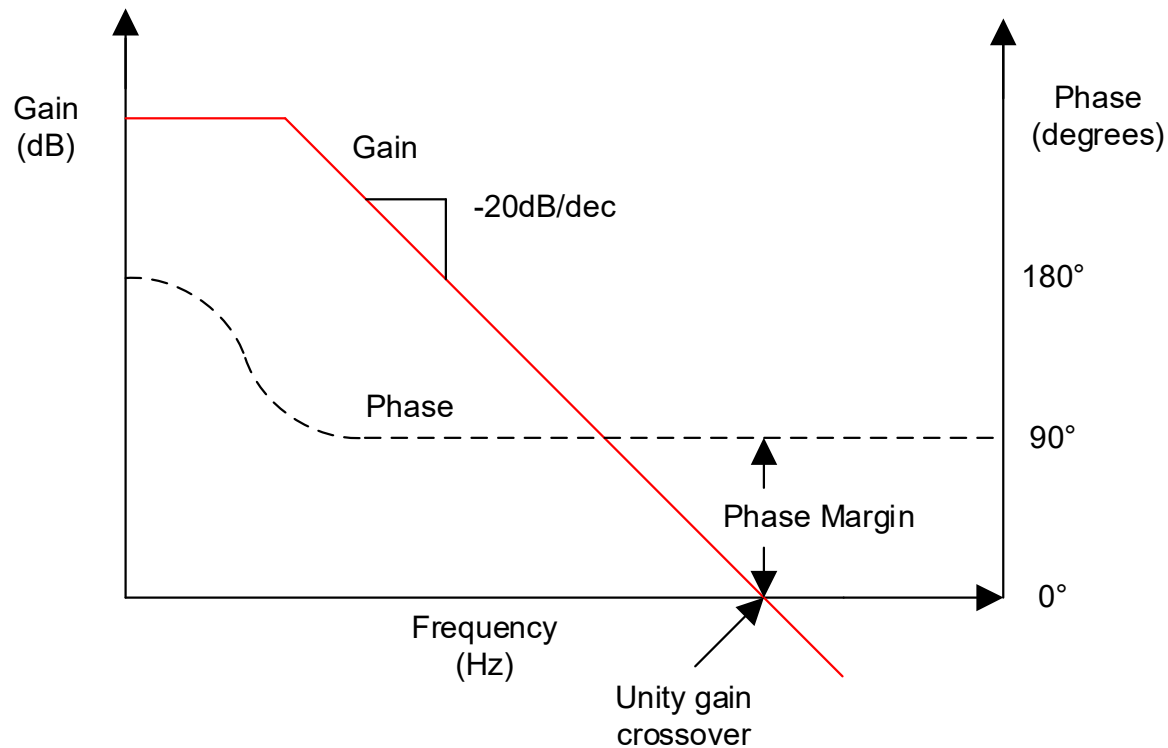
Analysis by Inspection

Slope = 0dB/decade



Slope = -40dB/decade

Ideal 1st Order Open Loop Gain



Single pole example

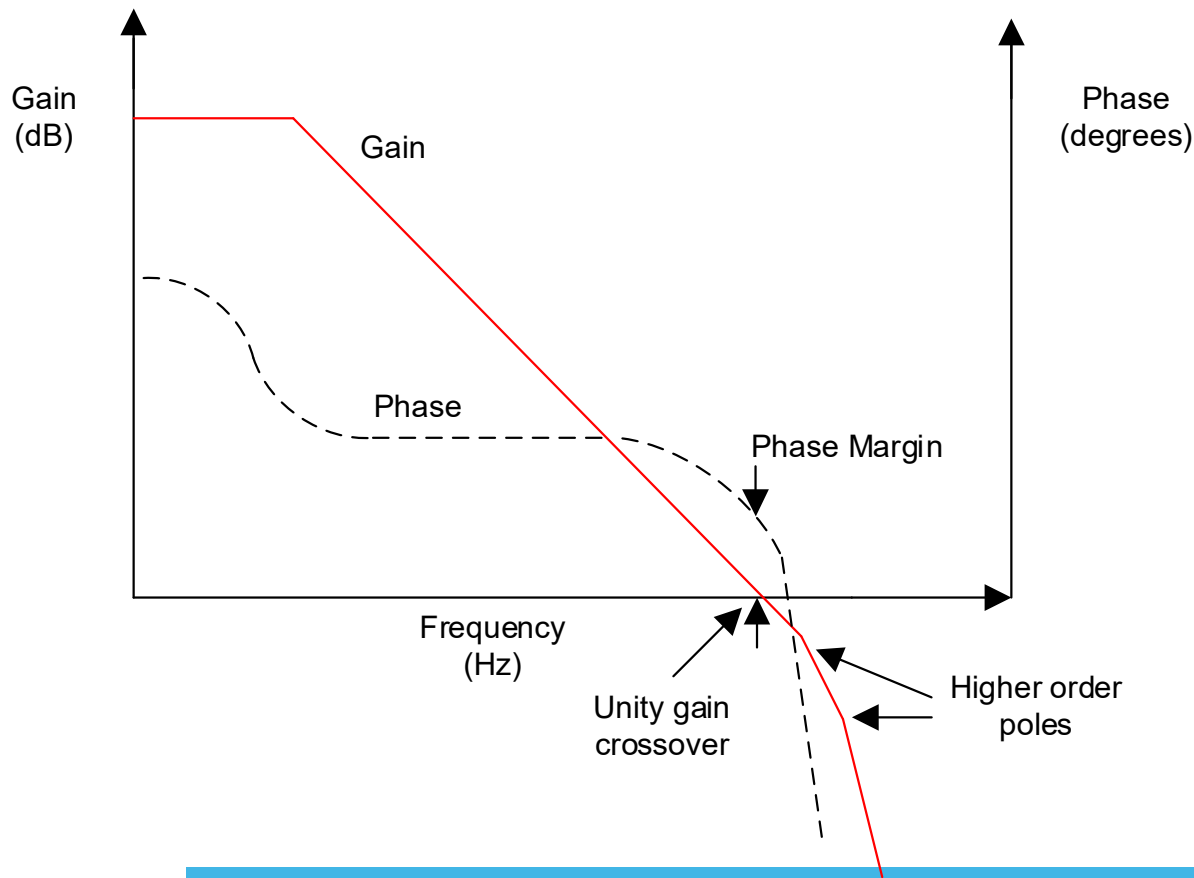
Phase margin definition:

180° - the amount of phase shift the opamp has undergone at the unity gain crossover frequency

Rules of Thumb

An Ideal opamp will have 90° of phase shift from the dominant pole with a constant -20dB/decade slope resulting in 90° of phase margin

Actual Open Loop Gain



Phase margin from higher order poles occurs after the unity gain crossover and reduces the phase margin at crossover

Rules of Thumb

The opamp will have 90° of phase shift from the dominant pole.
The opamp will have additional phase shift from the higher order poles.
A typical opamp will generally have around 65° of phase margin

Voltage Feedback Model

Definitions

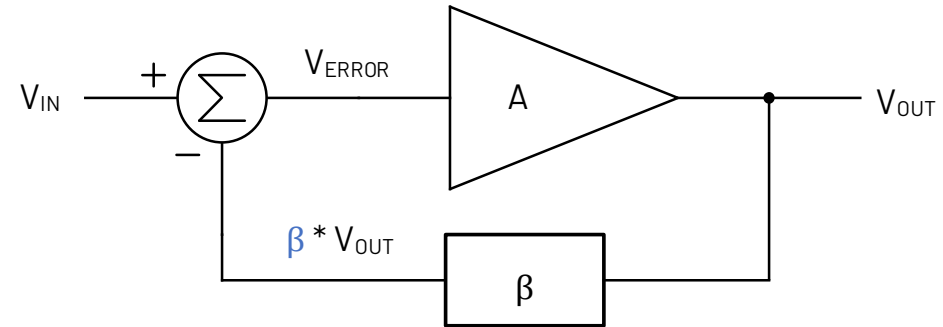
$A = A_{OL}$ = Open Loop Gain

β = Amount of output fed back to the input

A_{CL} = Closed Loop Gain

$A\beta$ = Loop Gain

$\frac{1}{\beta}$ = Ideal Closed Loop Gain



$$V_{OUT} = V_{ERROR} \times A$$

$$V_{ERROR} = V_{IN} - \beta \times V_{OUT}$$

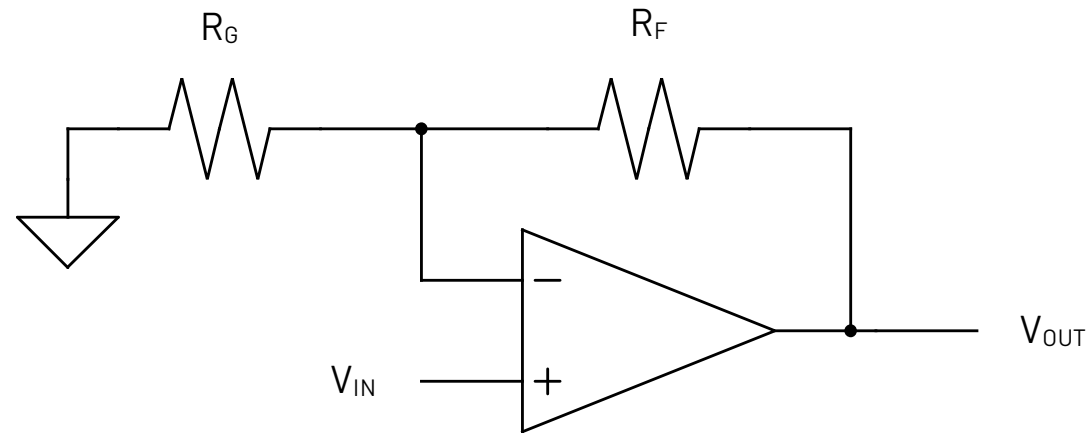
$$V_{OUT} = A \times V_{IN} - A \times \beta \times V_{OUT}$$

$$V_{OUT} \times (1 + A\beta) = A \times V_{IN}$$

$$\text{Closed Loop Gain} = \frac{V_{OUT}}{V_{IN}} = \frac{A}{(1 + A\beta)} = A_{CL}$$

Ideal Closed Loop Gain

Let's determine the ideal closed loop gain when the opamp is assumed to be ideal with infinite open loop gain:



$$A_{CL} = \frac{A}{(1 + A\beta)}$$

$$\lim_{A \rightarrow \infty} A_{CL} = \frac{\infty}{1 + \infty\beta} = \frac{1}{\beta}$$

$$A_{CL} = 1 + \frac{R_F}{R_G} = \frac{1}{\beta}$$

$$A_{CL} = \frac{A}{(1 + A\beta)}$$



$$\lim_{A\beta \rightarrow -1} A_{CL} = \frac{A}{1 + (-1)} = \frac{A}{0} = \infty$$



$$|A\beta| = -1$$

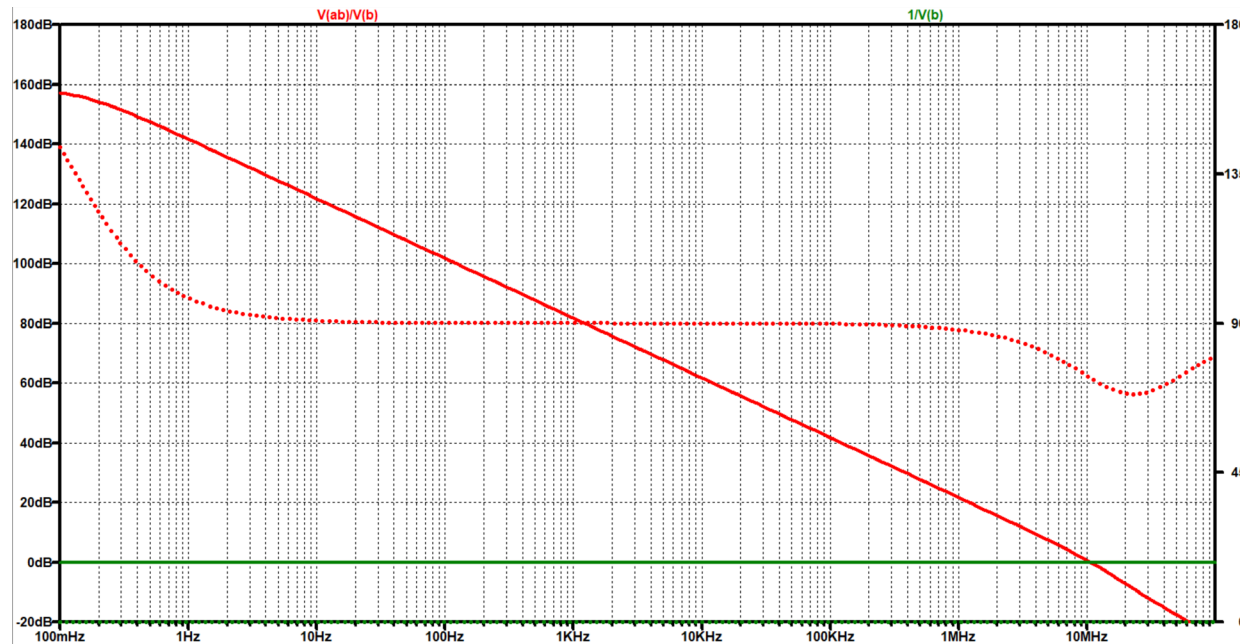
$$|A\beta| = 1 \angle 180^\circ$$

$$|A\beta| = -1$$

$$|A| = \left| \frac{1}{\beta} \right| \angle 180^\circ$$

Rule of Thumb

To determine the stability of the amplifier circuit, plot the Aol and Acl and look at the phase margin at their intercept

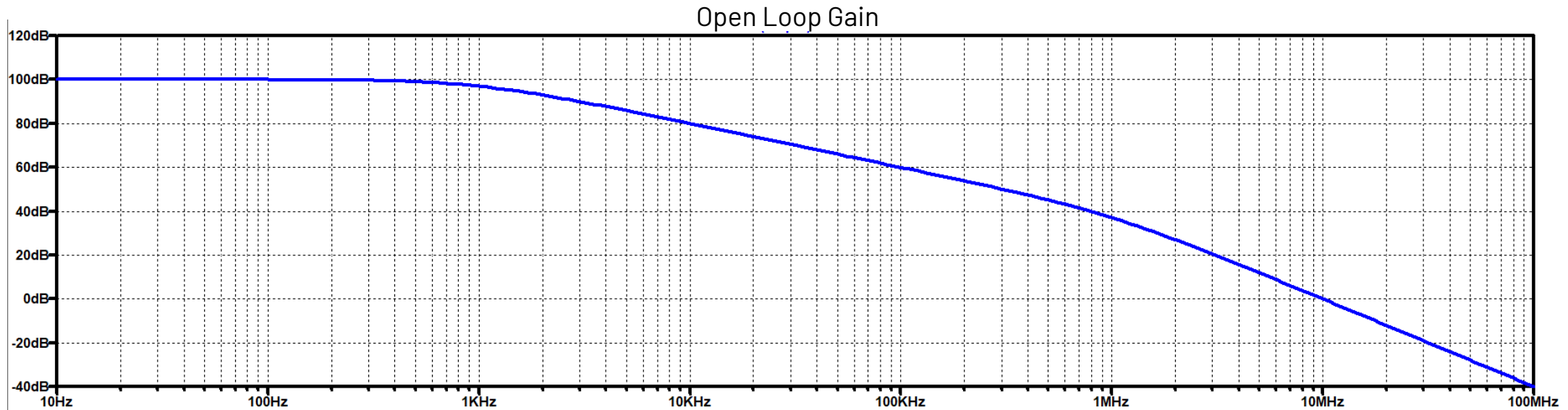


Rate of
closure
indicates
phase

Rules of Thumb

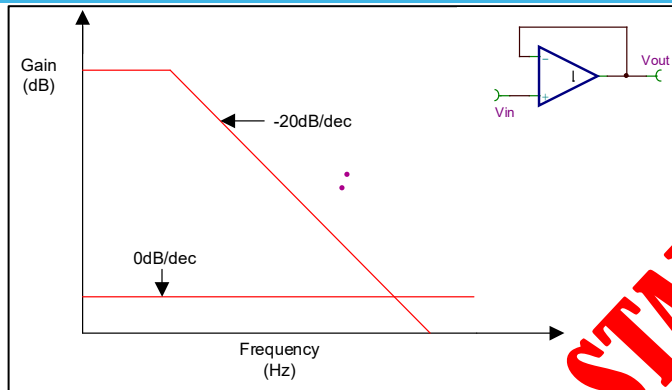
Phase margin goes hand in hand with the rate of closure between the A_{OL} and A_{CL} curves
To determine the stability of the amplifier circuit, plot the A_{OL} and A_{CL} and look at the phase margin (rate of closure) at their intercept

If the rate of closure is 20dB/dec the system is stable
If the rate of closure is 40dB/dec the system is unstable

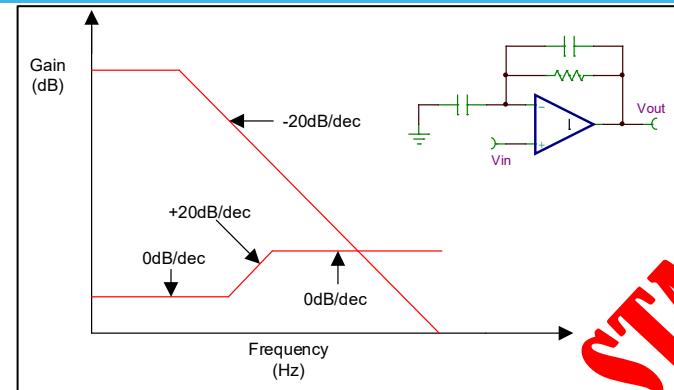


- ▶ What is the slope from 10Hz to 1kHz?
- ▶ What is the slope from 1kHz to 1MHz?
- ▶ What is the slope from 1MHz to 100MHz?
- ▶ Phase shift at 100Hz?
- ▶ Phase shift at 1kHz?
- ▶ Phase shift at 10kHz?
- ▶ Phase shift at 100kHz?
- ▶ Phase shift at 1MHz?
- ▶ Phase shift at 10MHz?
- ▶ What is DC Open Loop Gain in V/V?
- ▶ What is GBP at 40dB?
- ▶ What is UGF?
- ▶ What is Phase Margin?
- ▶ Is this opamp Unity Gain Stable?
- ▶ Assume this opamp is placed in an inverting configuration. What is the phase margin in a gain of -99V/V?

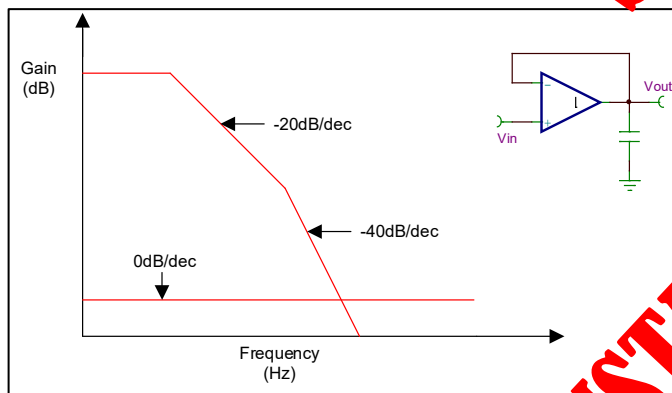
A single pole system has a slope of -20dB/decade with a total of 90° of phase shift
A two pole system has a slope of -40dB/decade with a total of 180° of phase shift
If a system has a 20dB/dec rate of closure it is stable
If a system has a 40dB/dec rate of closure it is unstable



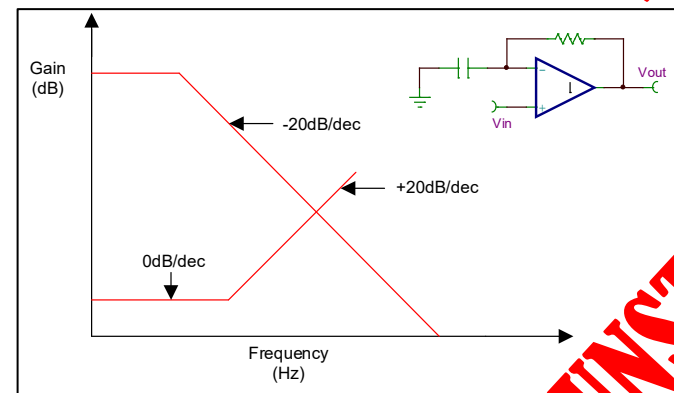
STABLE



STABLE

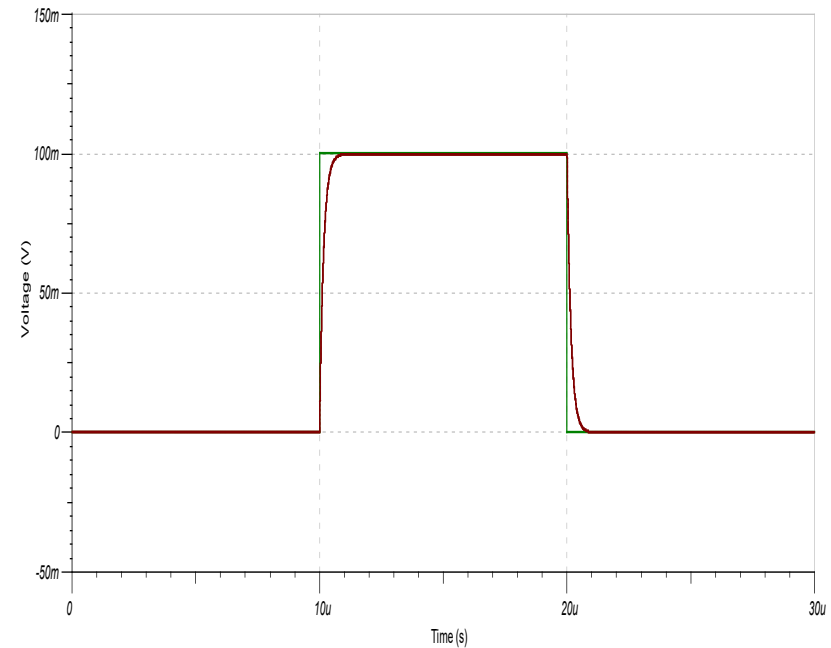
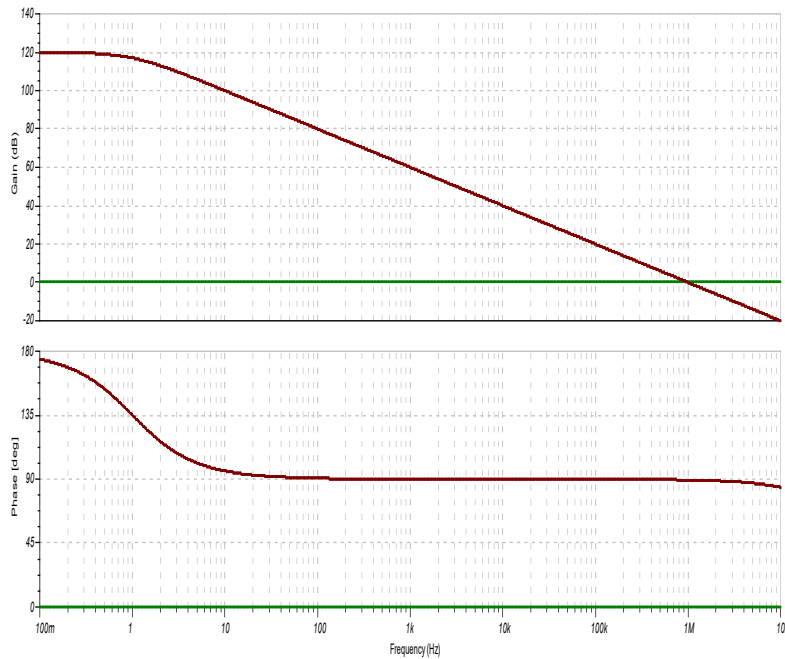
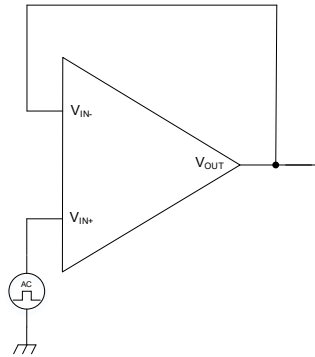


UNSTABLE

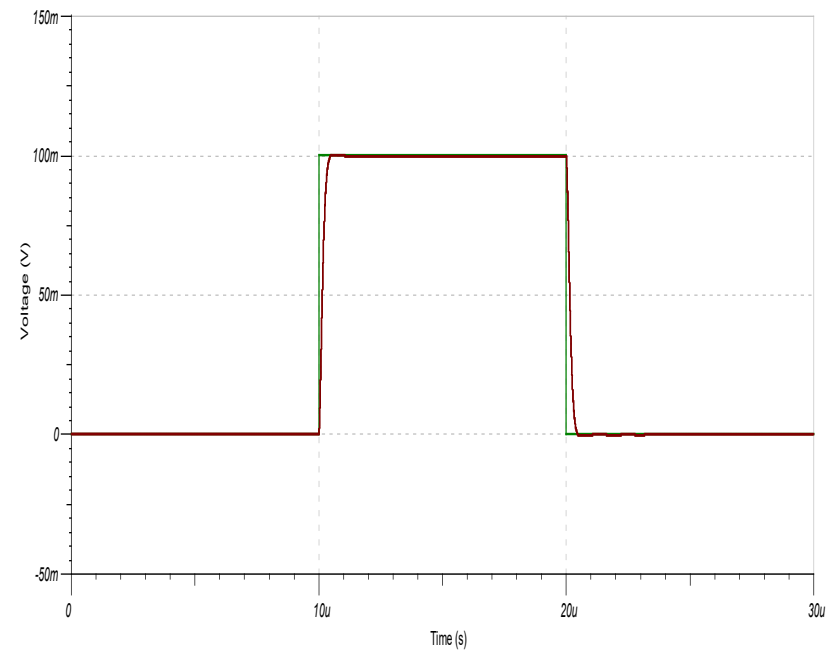
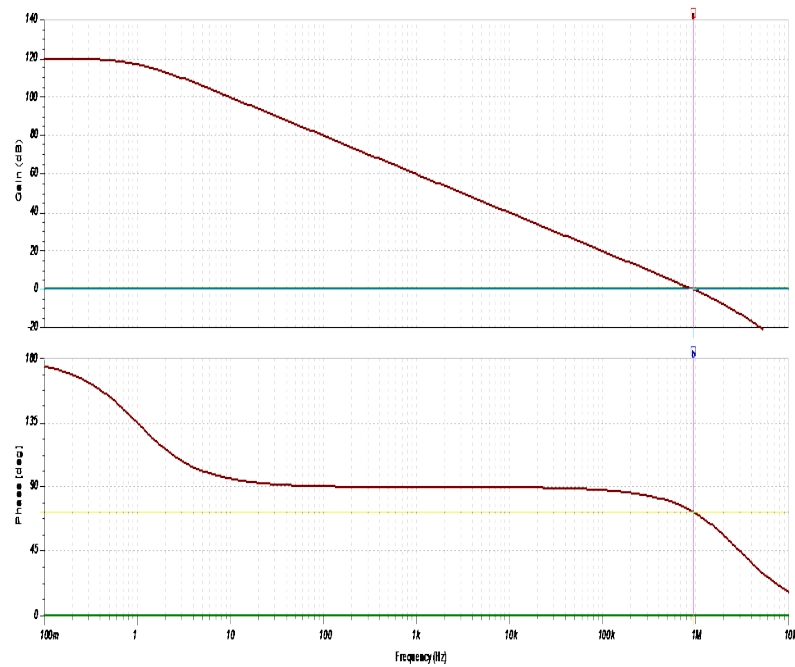
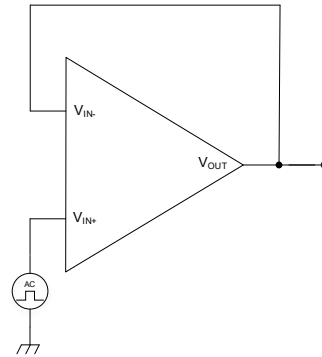


UNSTABLE

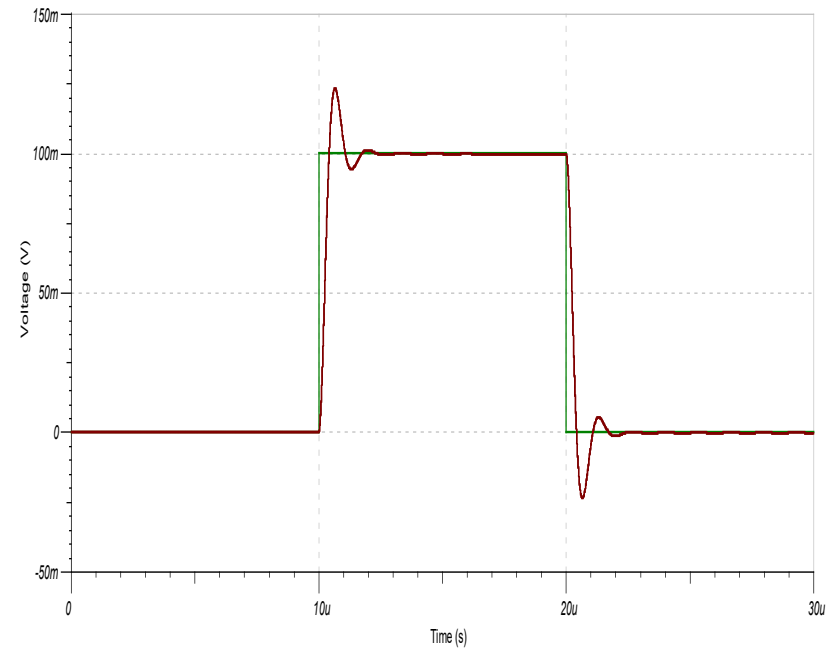
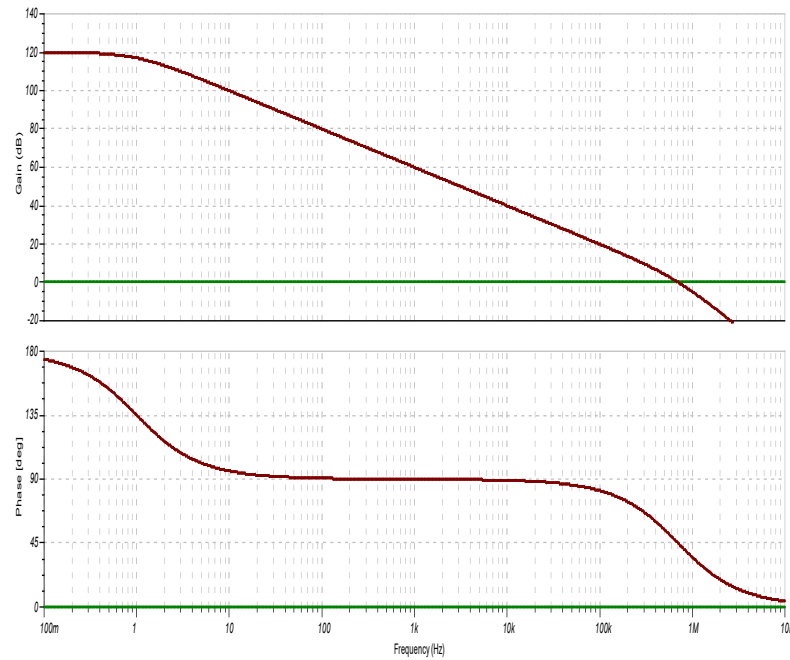
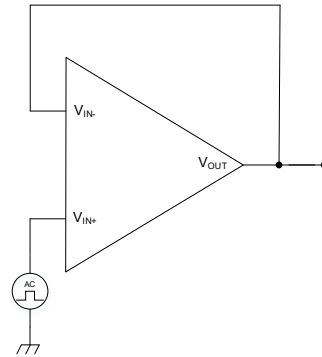
90° Phase Margin



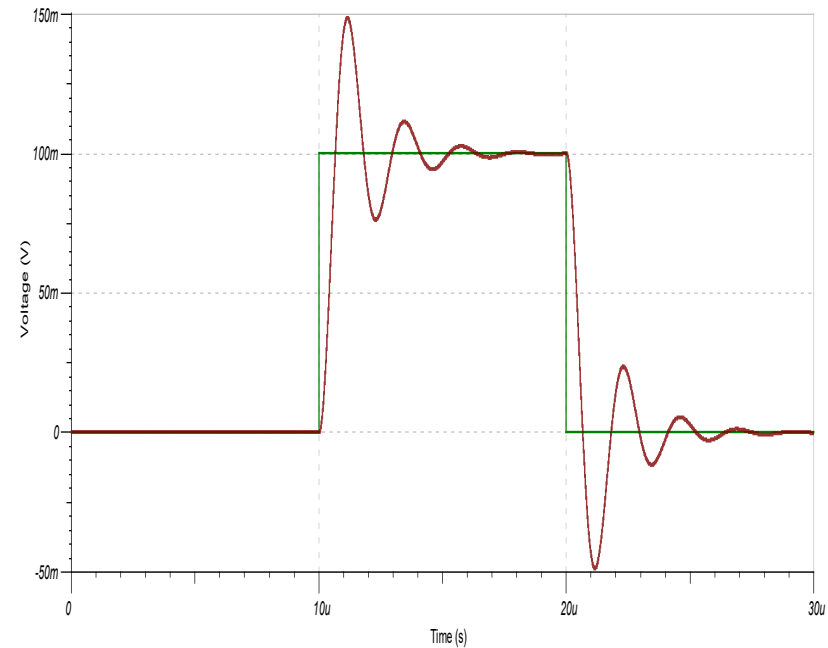
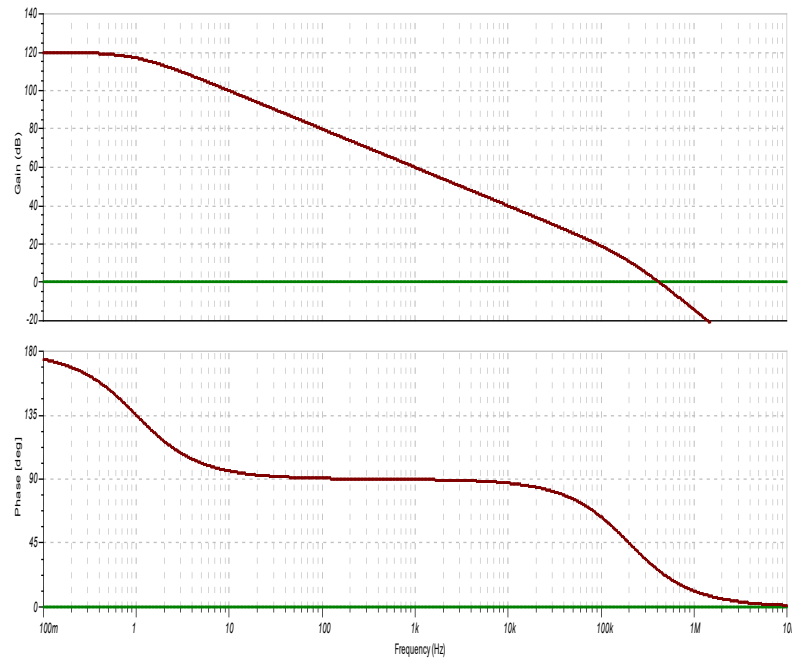
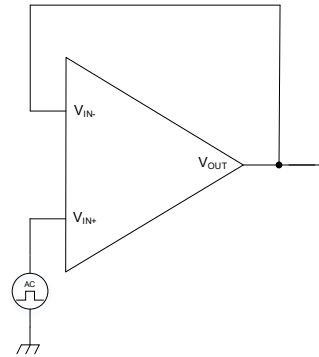
70° Phase Margin




45° Phase Margin

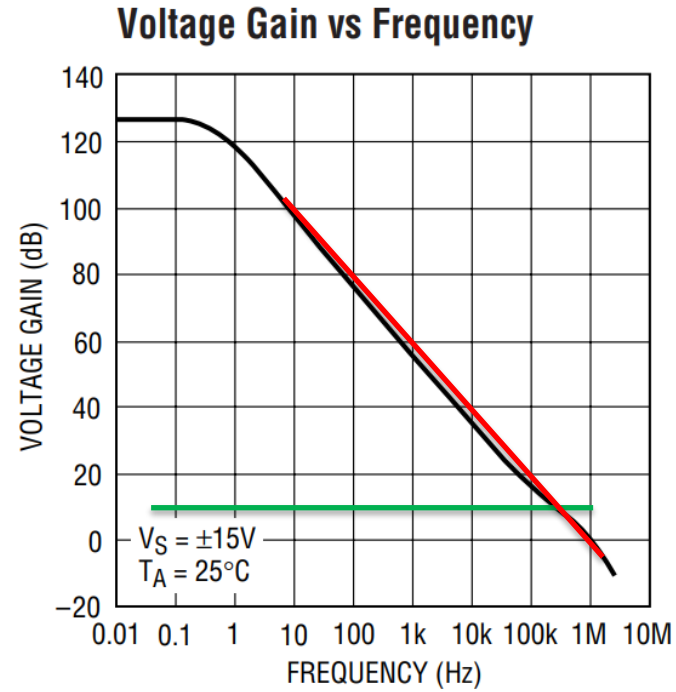
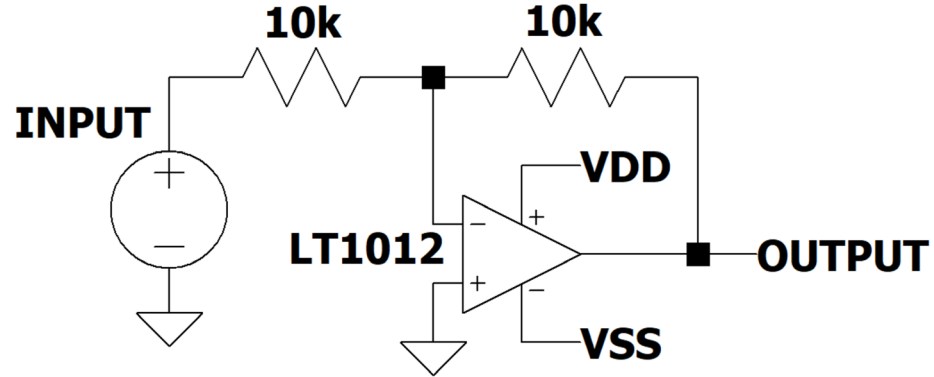


25° Phase Margin



Putting it All Together

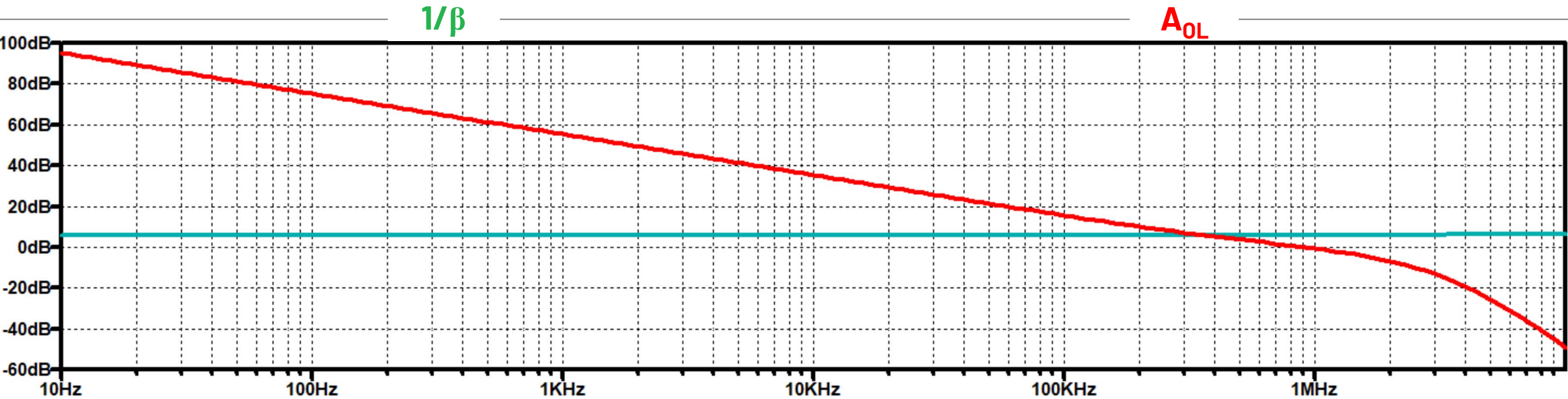
1. Sketch the open loop gain (A_{ol}) vs frequency (data is usually available in the device data sheet)
2. Sketch the closed loop gain (A_{cl}) vs frequency (requires a quick intuitive analysis)
3. Observe the Rate of Closure at the intersection of the closed loop gain and open loop gain
4. If stable 
5. If unstable determine how to modify the circuit to ensure a 20dB/dec rate of closure
6. Estimate or simulate transient response



— A_{OL}
— A_{CL}

Stable or Unstable?

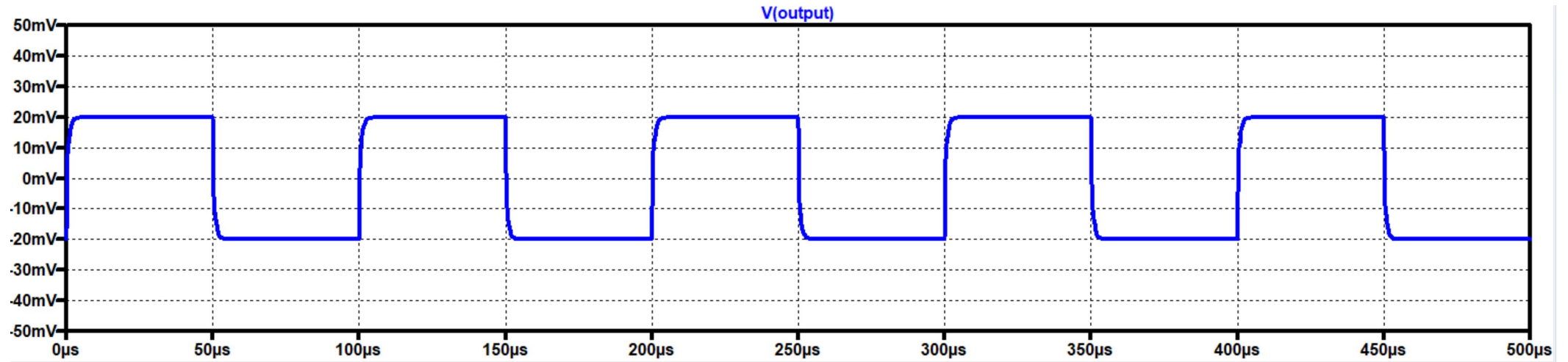
Analyze through Simulation of A_{OL} and $1/\beta(A_{CL})$



Rate of closure is 20dB/dec => Stable

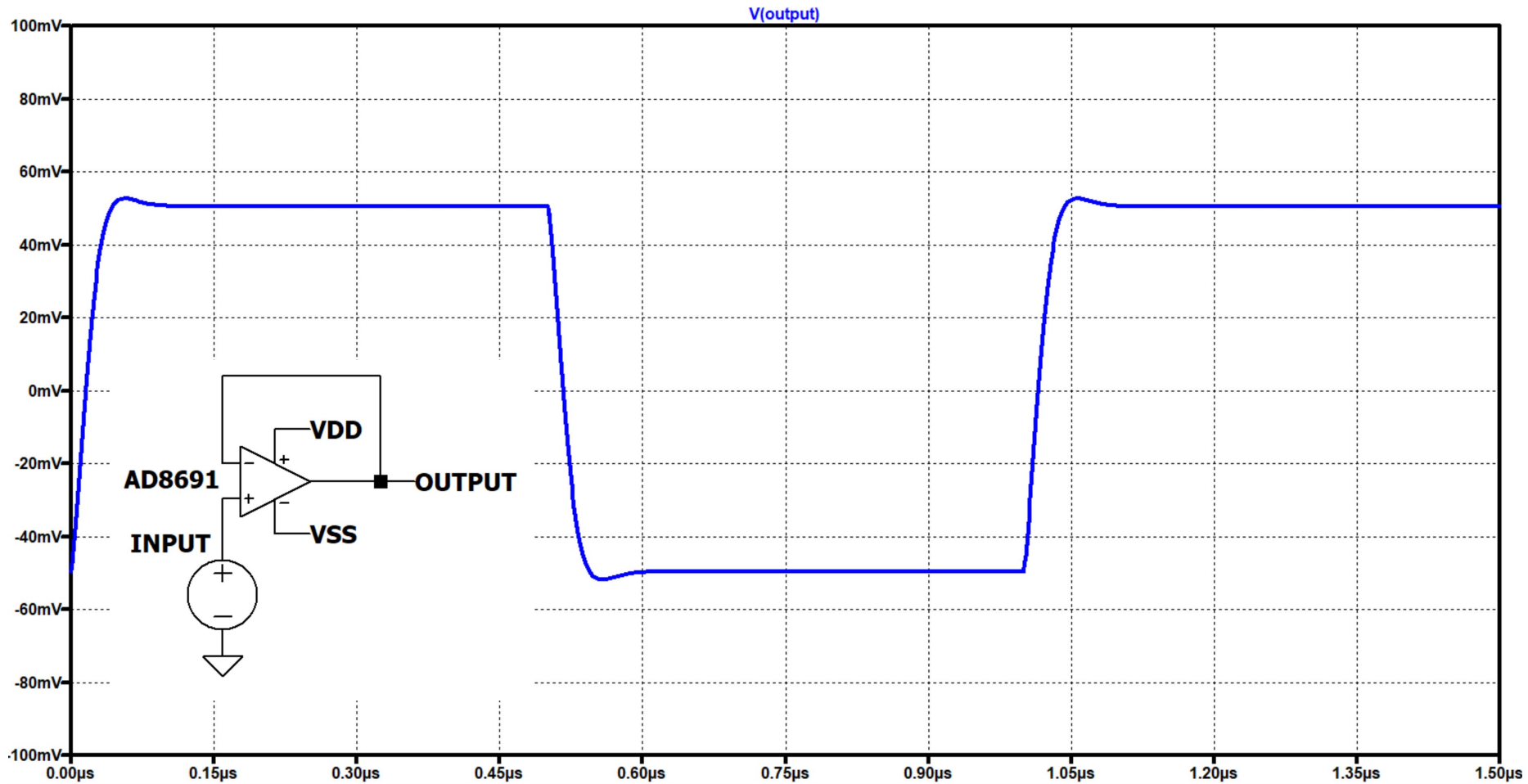


Transient Response

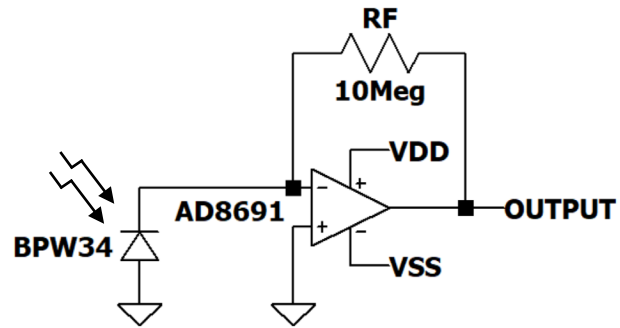


Example 1: TIA

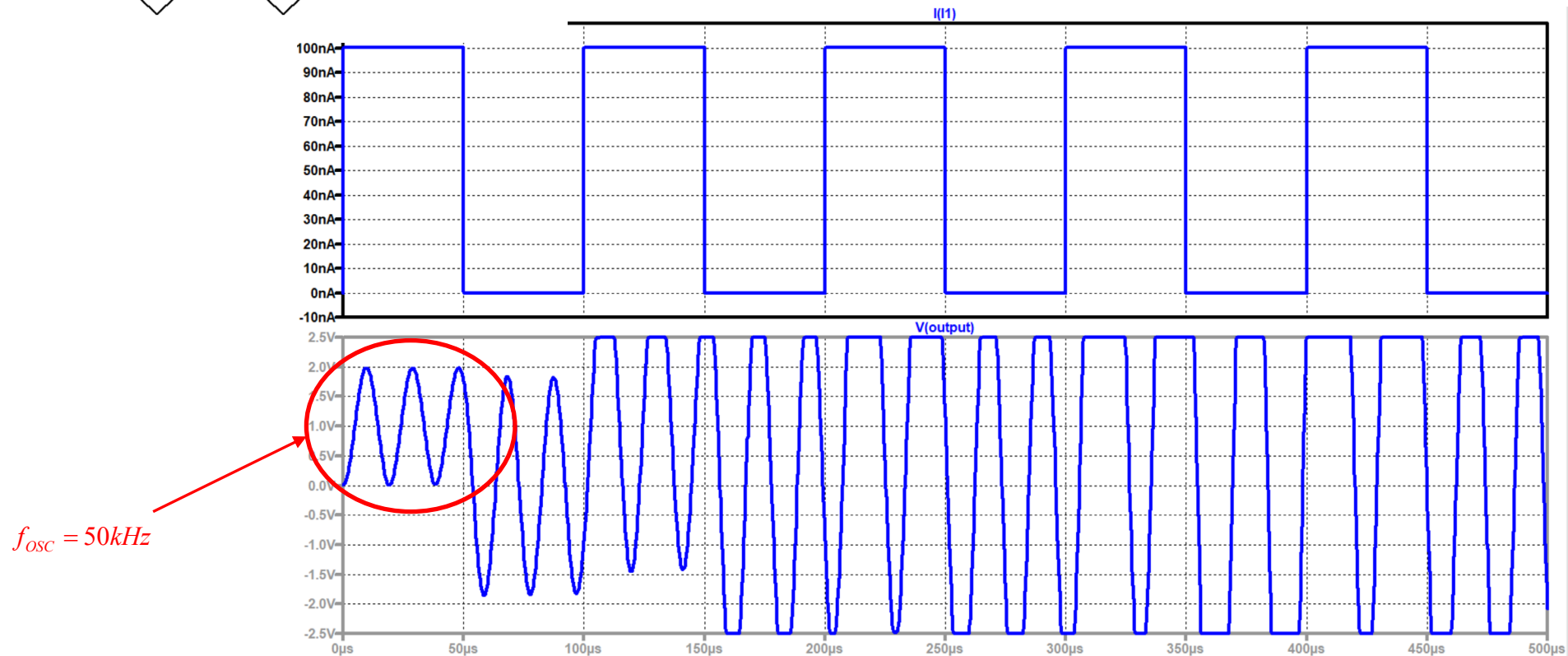
Seems stable, what could possibly go wrong? So let's build a photodiode amplifier!



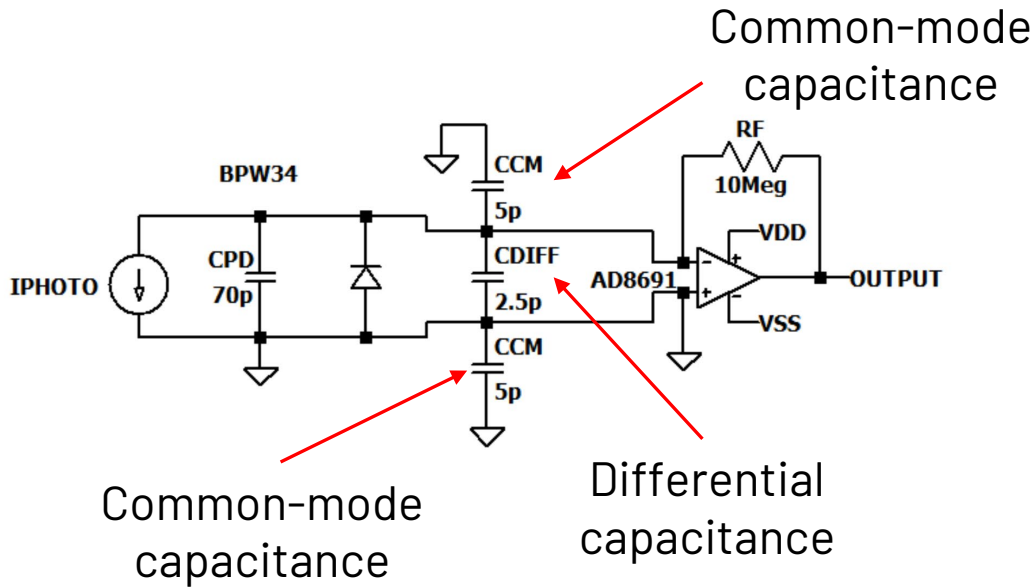
Example 1: TIA



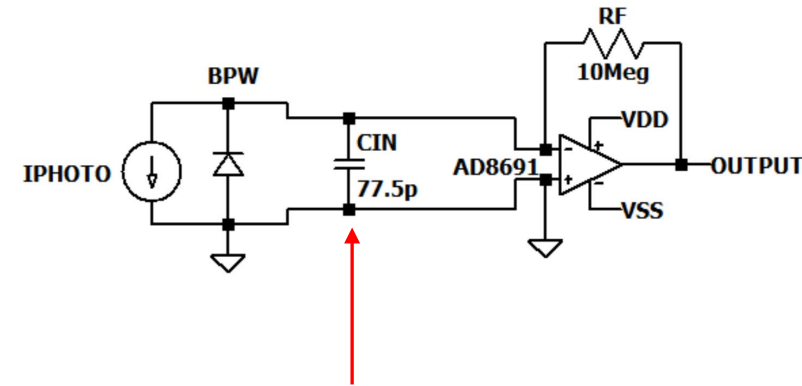
Hmmm! Not stable in the application! Let's have a look under the hood...



Example 1: TIA



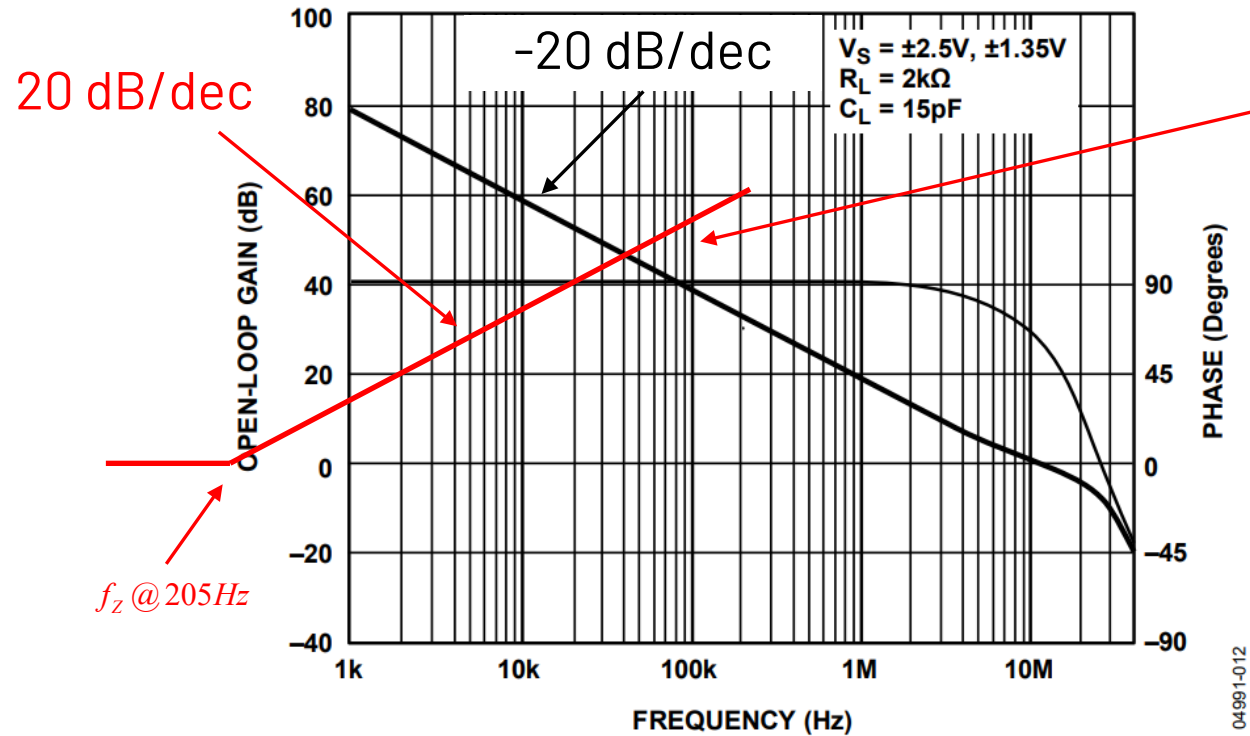
(note: this capacitance is not relevant as it has ground connected to both sides)



$$C_{IN} = C_{PHOTO} + C_{CM} + C_{DIFF}$$

Draw the “parasitic” opamp input capacitances and photodiode capacitance on the schematic, get values from data sheets, simplify and analyze by hand

Example 1: TIA



AOL and ACL
intercept at
50kHz!
Rate of
closure =
40db/dec
→ unstable

$$A_{CL} = 1 + \frac{Z_F}{Z_G}$$

$$Z_F = R_F$$

$$Z_G = \frac{1}{2\pi f C_{IN}}$$

$$A_{CL \lim_{f \rightarrow 0}} = 1$$

$$A_{CL \lim_{f \rightarrow \infty}} = \infty$$

$$f_z = \frac{1}{2\pi R_F C_{IN}} = \frac{1}{2\pi \times 10M\Omega \times 77.5pf} = 205Hz$$

- 1) Get the Open Loop Gain plot from the data sheet
- 2) Add closed loop gain to the plot

Example 1: TIA

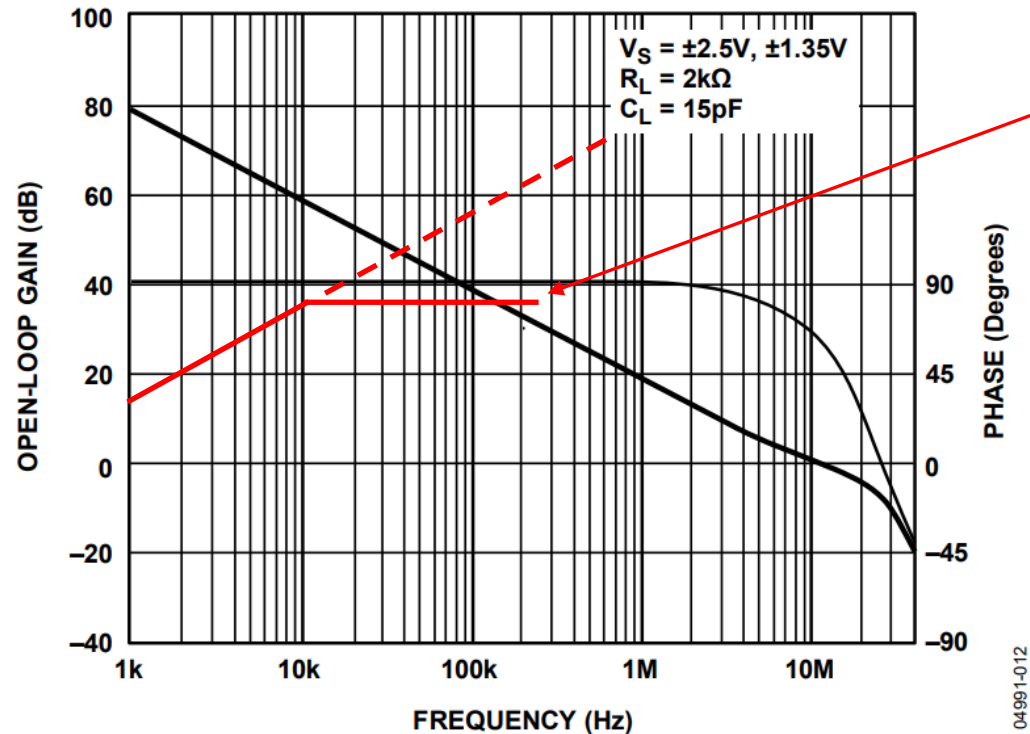


Figure 14. Open-Loop Gain and Phase vs. Frequency

Solution:

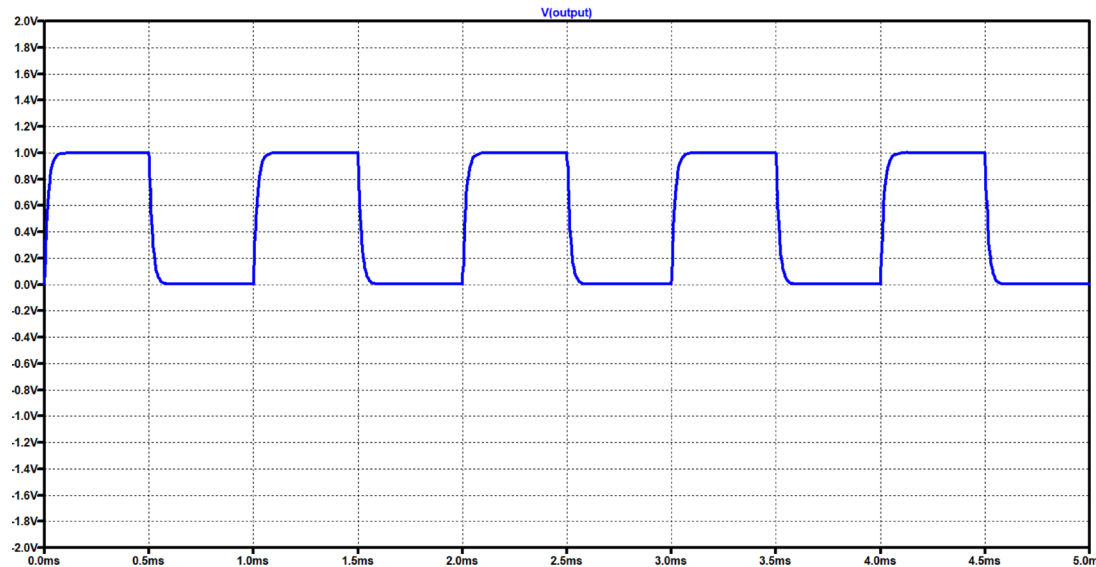
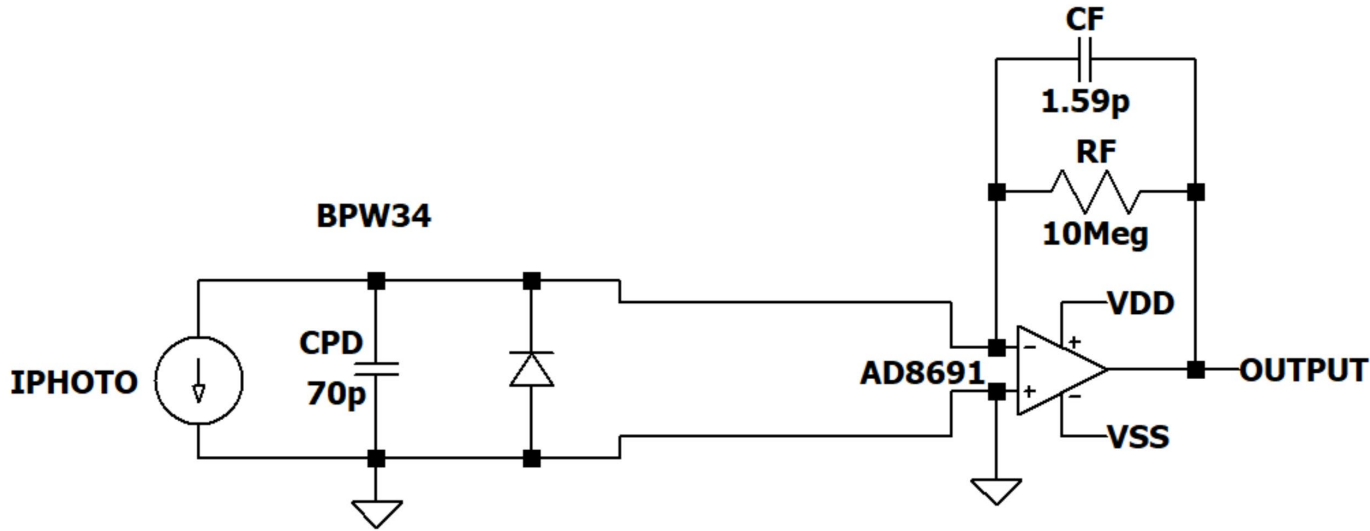
Change rate of closure by adding a capacitor in parallel with R_F to flatten the gain at high frequency

Now the rate of closure is 20 dB/dec

$$C_F = \frac{1}{2\pi f R_F} = 1.59 \text{ pf}$$

- 1) Get the Open Loop Gain plot from the data sheet
- 2) Add the new closed loop gain to the plot

Example 1: TIA



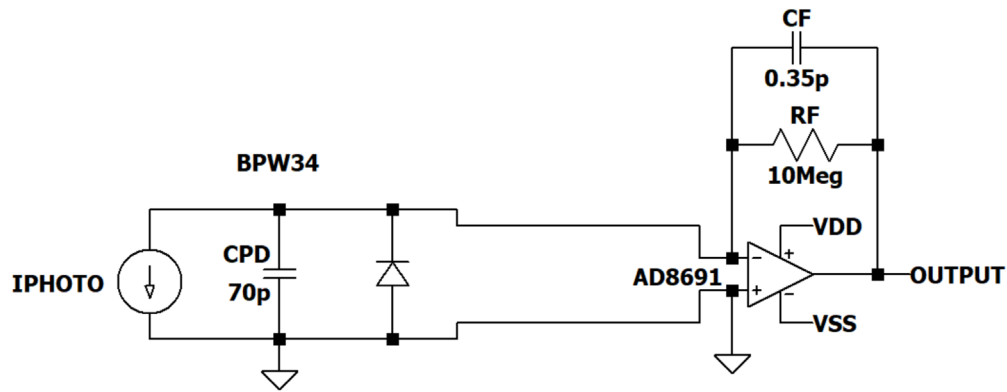
Result:

The compensated circuit is very stable

Notice that the bandwidth of the circuit is determined by

$$R_F // C_F$$

Example 1: TIA

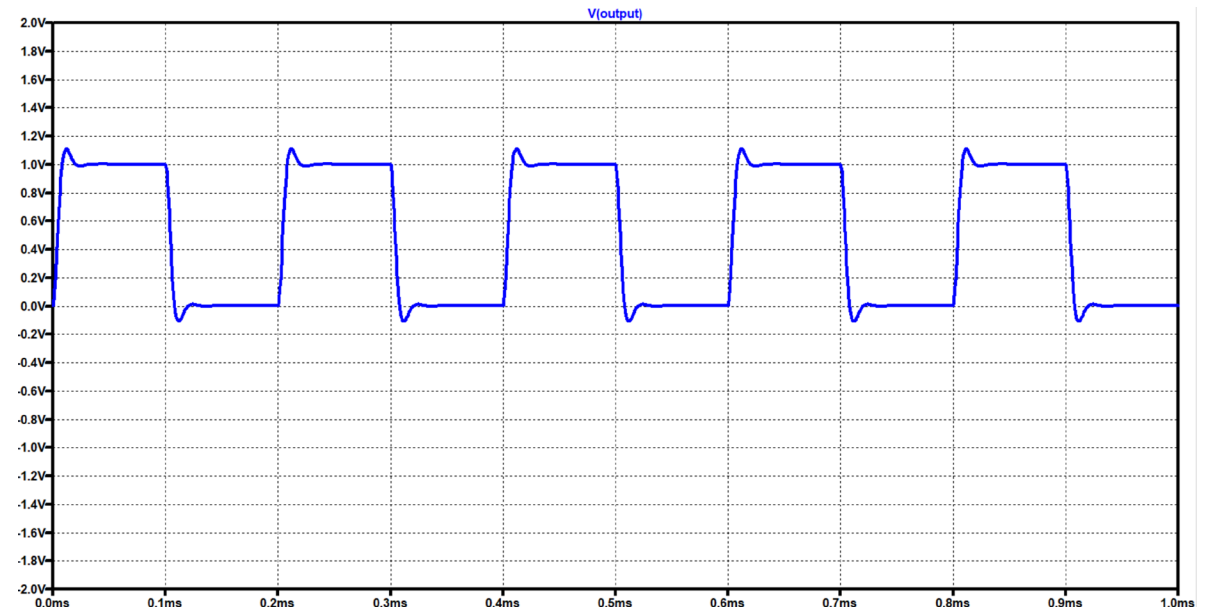
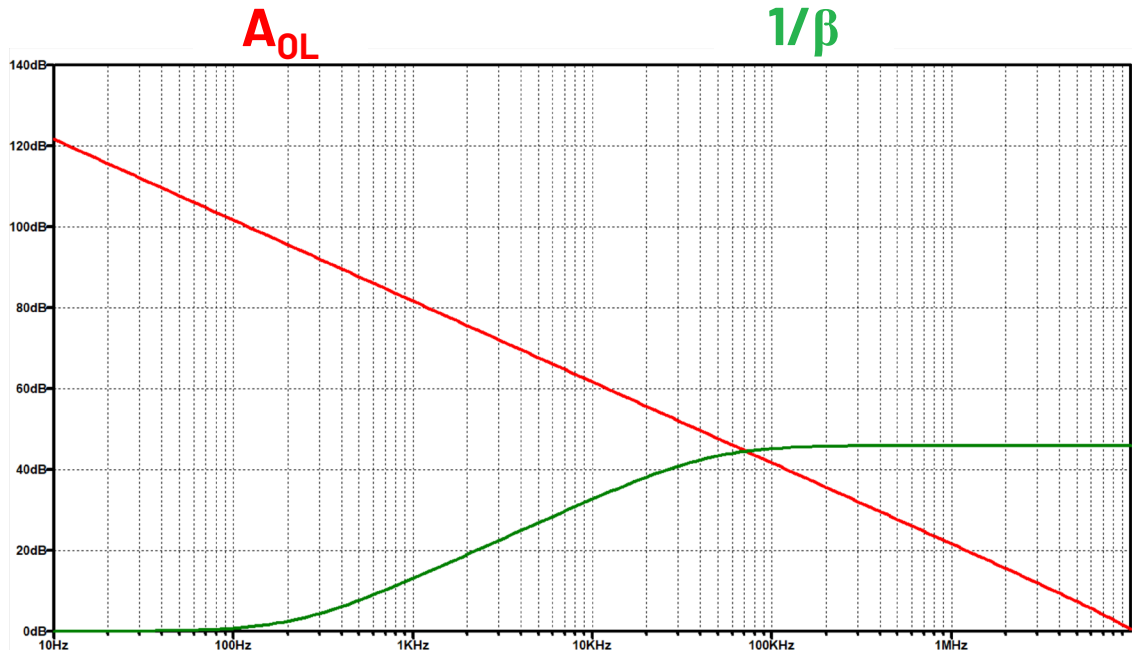


For maximum bandwidth while still maintaining 45° of phase margin use the following equation:

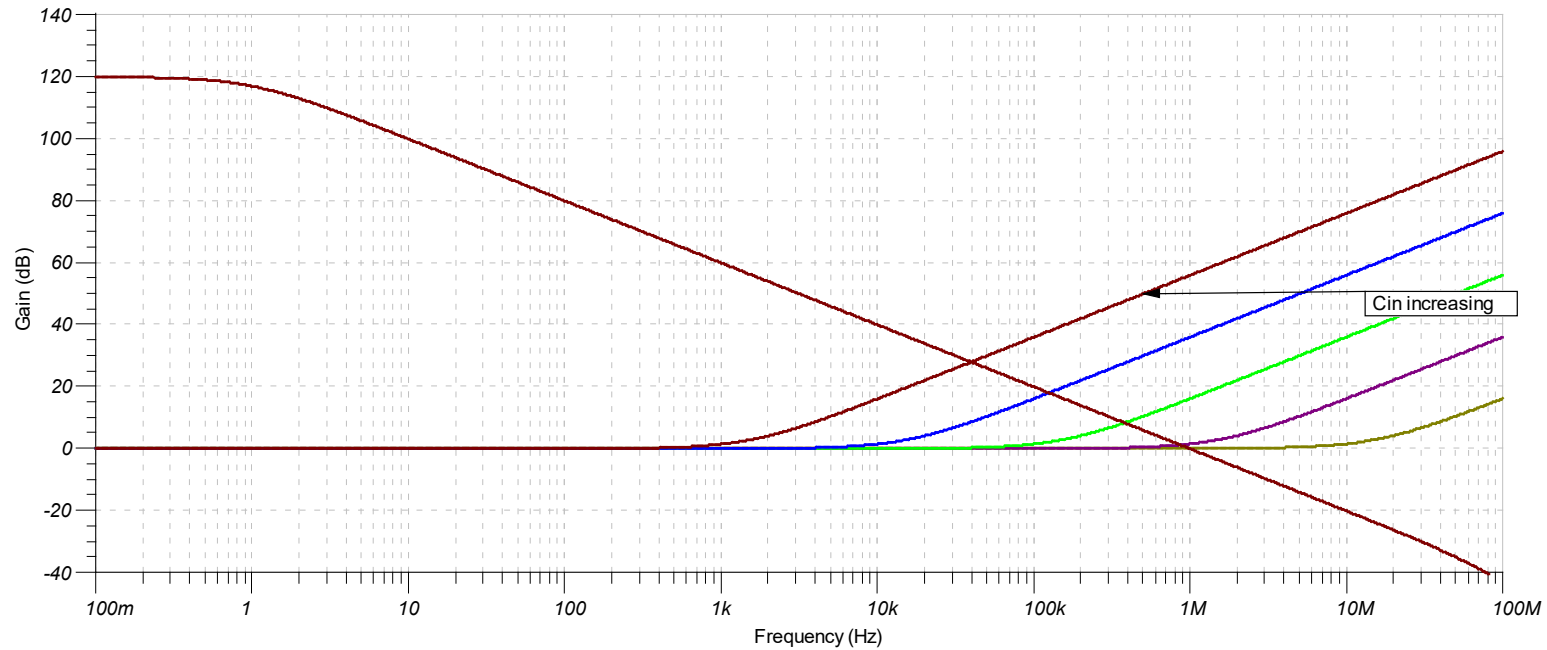
$$f_{COMP} = \sqrt{f_z f_U}$$

f_z = zero frequency as a result of the photodiode capacitance reacting with the feedback resistor

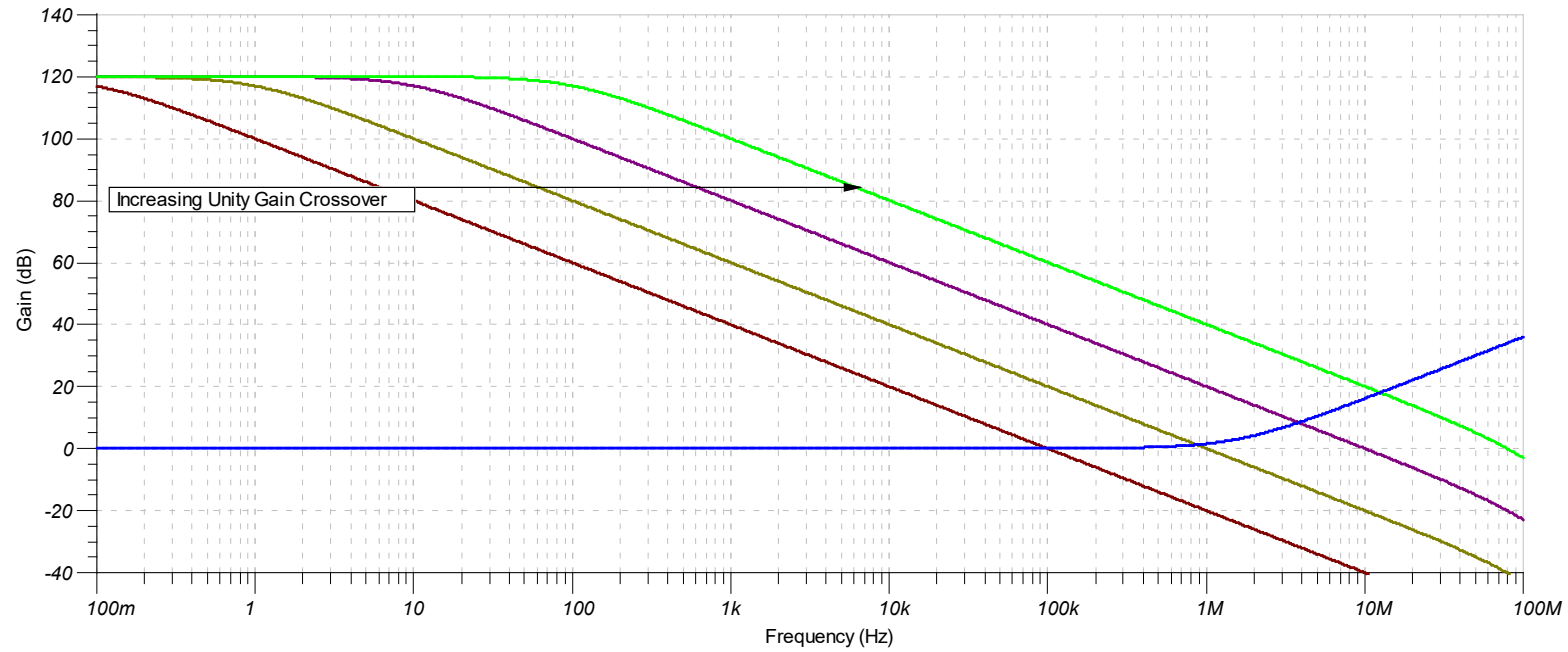
f_U = unity gain frequency of the amplifier



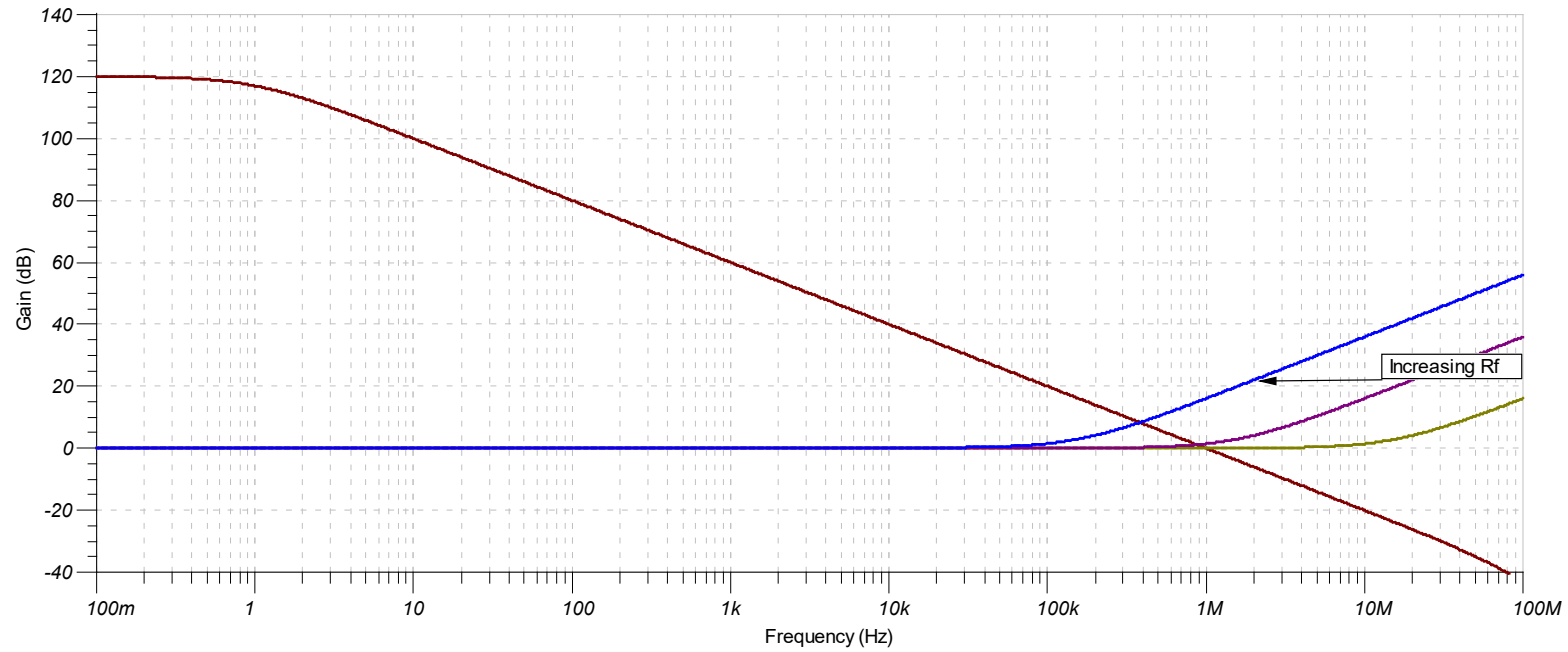
Increasing C_{in}



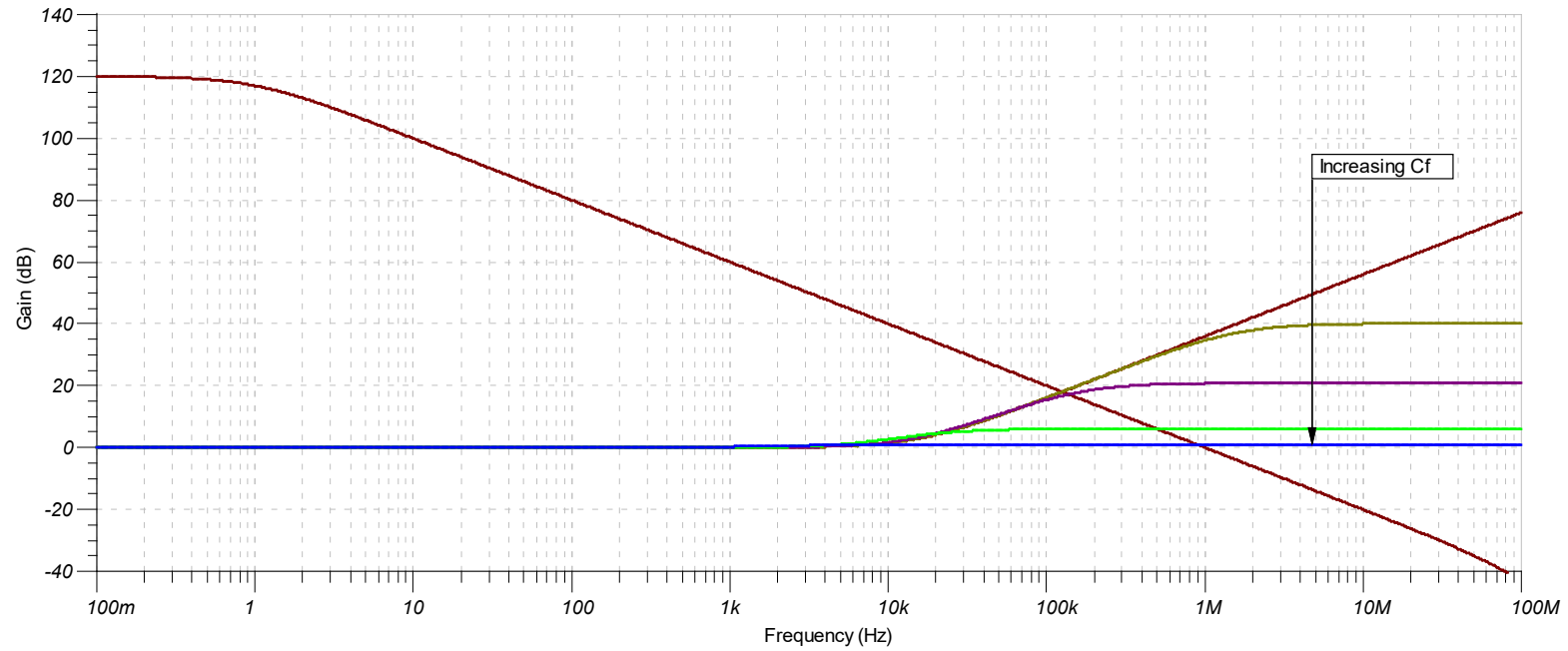
Increasing Opamp BW



Increasing Rf

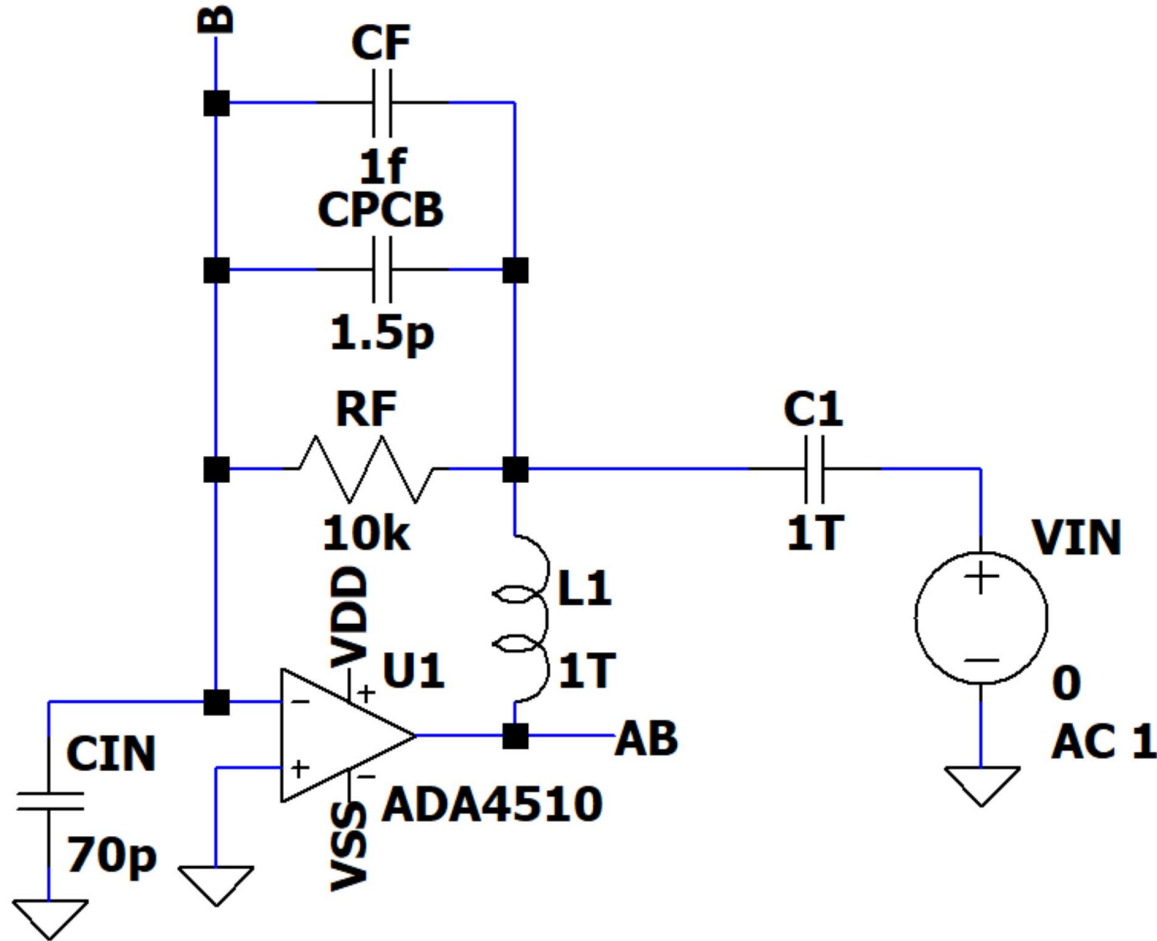


Increasing Cf



- ▶ Input capacitance (on the inverting input) reacts with feedback resistance to create a zero in the feedback and reduces the circuit phase margin
- ▶ Large value feedback resistors react at lower frequencies than lower values resistors
- ▶ Input capacitance can come from PCB traces, wires and cables, protection devices such as diodes, the opamp itself, sensors
- ▶ Placing a capacitor across the feedback resistor adds a zero into the feedback loop and increases the circuit phase margin
- ▶ Opamp circuits will require stability analysis and compensation, especially:
 - When opamp UGF is large
 - When feedback resistance is large
 - When the input capacitance at the summing node is large

How Do You Simulate for Stability?

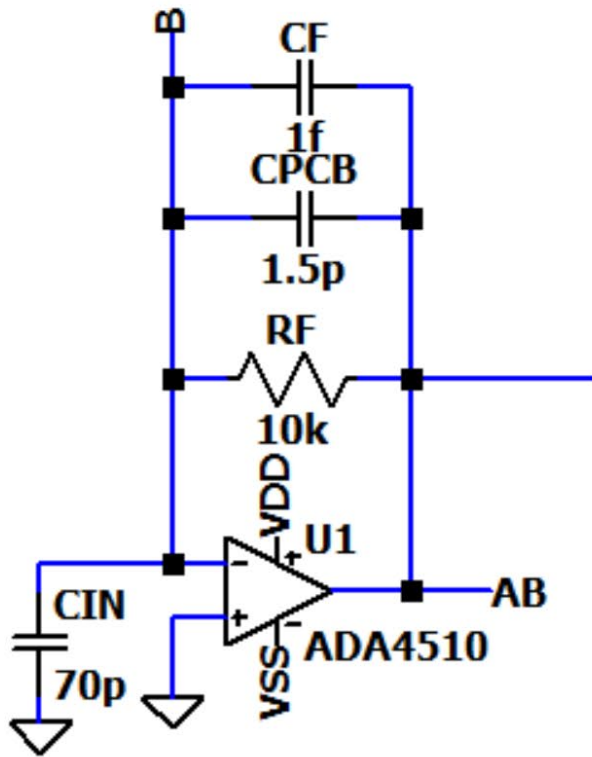


```
.op  
.ac dec 101 1 100MEG  
.options gfarad=0
```

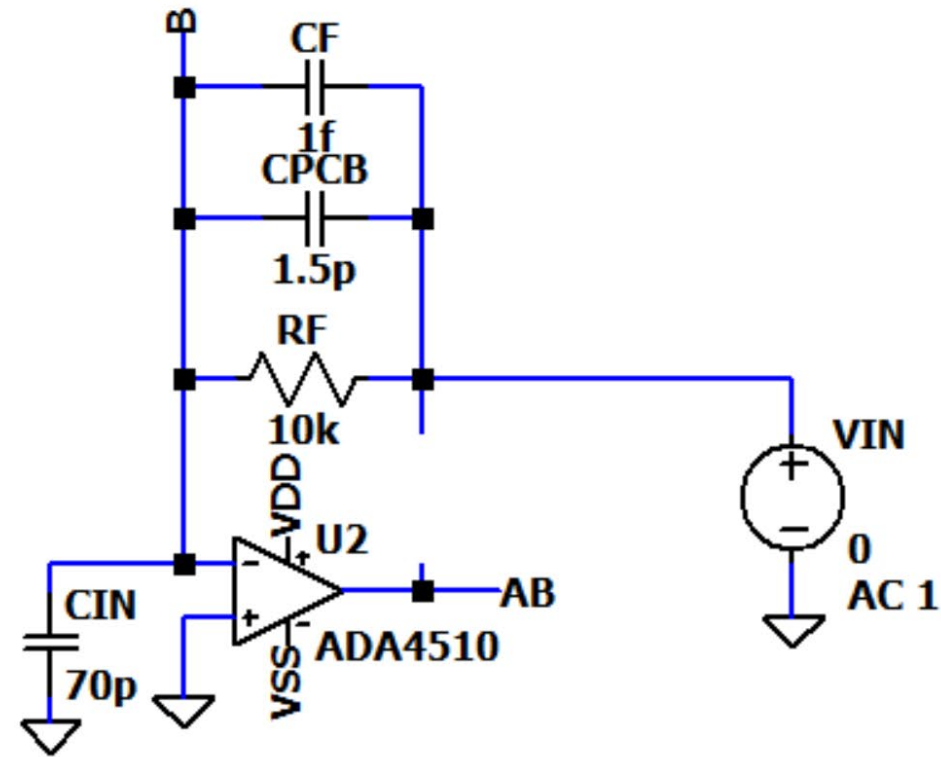
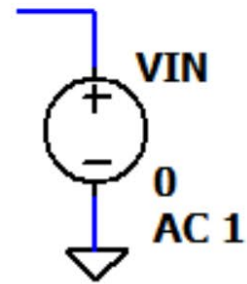
How Do You Simulate for Stability?

- ▶ You must break the loop and simulate in the AC domain
- ▶ At DC the inductor looks like a short and the capacitor appears to be open
- ▶ This allows the circuit to converge at its intended operating point
- ▶ During an “AC” analysis the operating point is first determined, then the circuit is linearized around that operating point, basically think about it as the simulator is taking the tangent to the curve
- ▶ For frequencies above DC, the inductor now appears open and the capacitor appears as a short and the circuit looks like it is in an open loop configuration

How Do You Simulate for Stability?



Equivalent circuit at DC

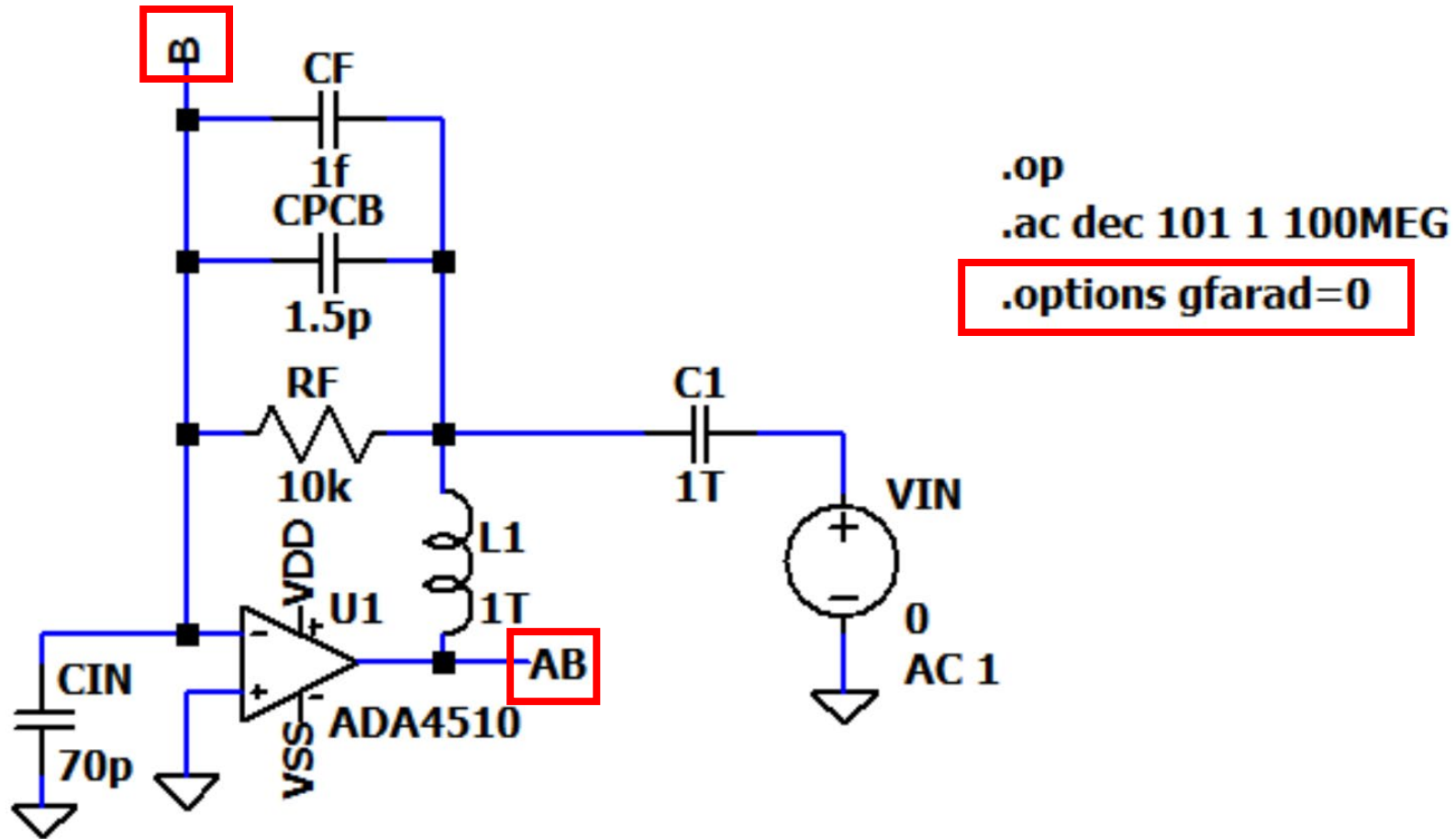


Equivalent circuit at frequencies above DC

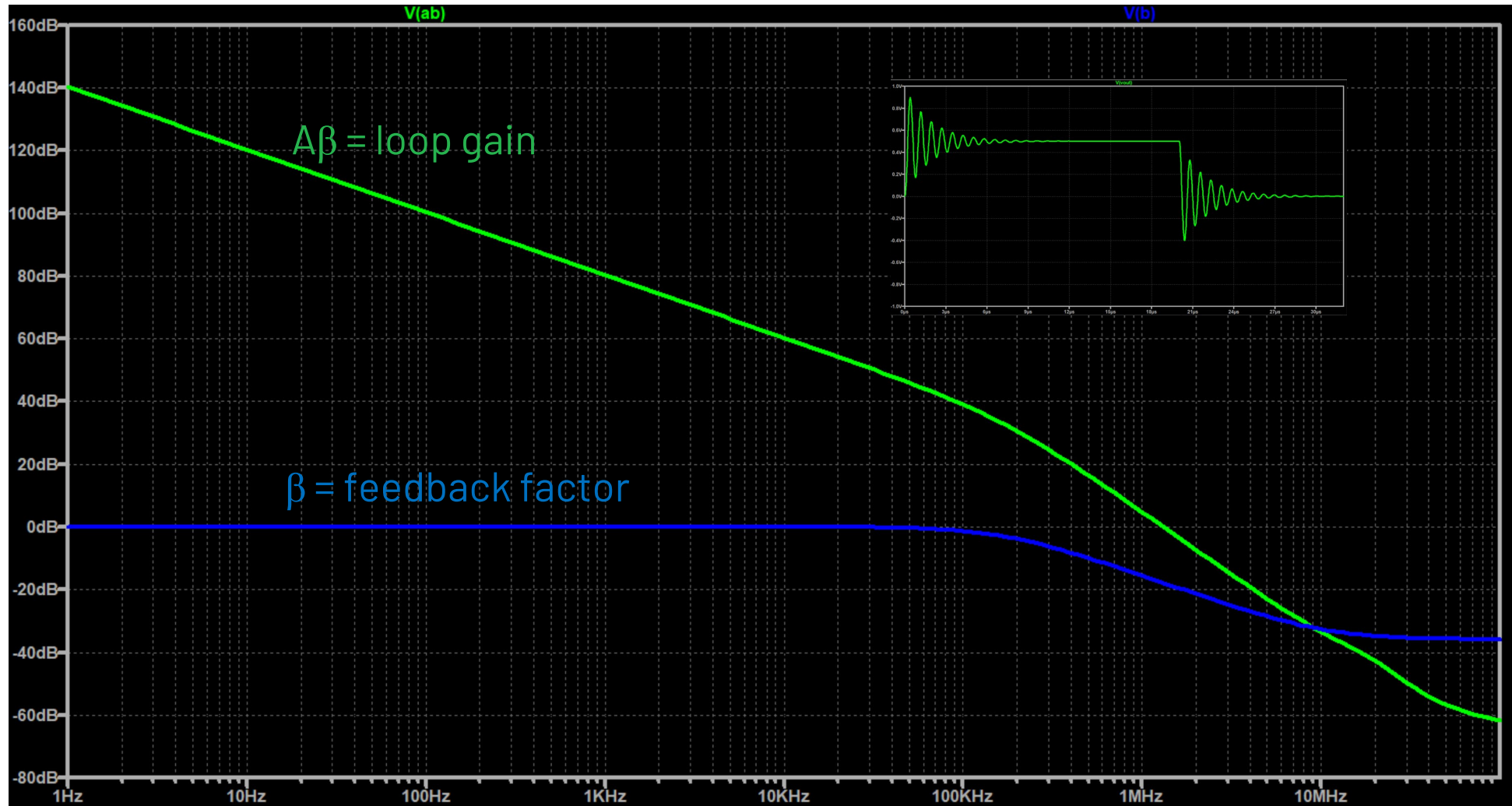
How Do You Simulate for Stability?

- ▶ Label the amplifier output “AB”...this is also known as the “loop gain”
- ▶ Label the summing node “B”...this is also known as the “feedback factor”
- ▶ In the plot window, plot $V(AB)/V(B)$...this is A_{ol}
- ▶ In the plot window, plot $1/V(B)$...this is A_{cl} , or $1/\beta$
- ▶ Review the intercept of A_{ol} and $1/\beta$ for the rate of closure
- ▶ Alternatively, you may plot the loop gain, $V(AB)$, and see where the loop gain crosses 0 dB

How Do You Simulate for Stability?



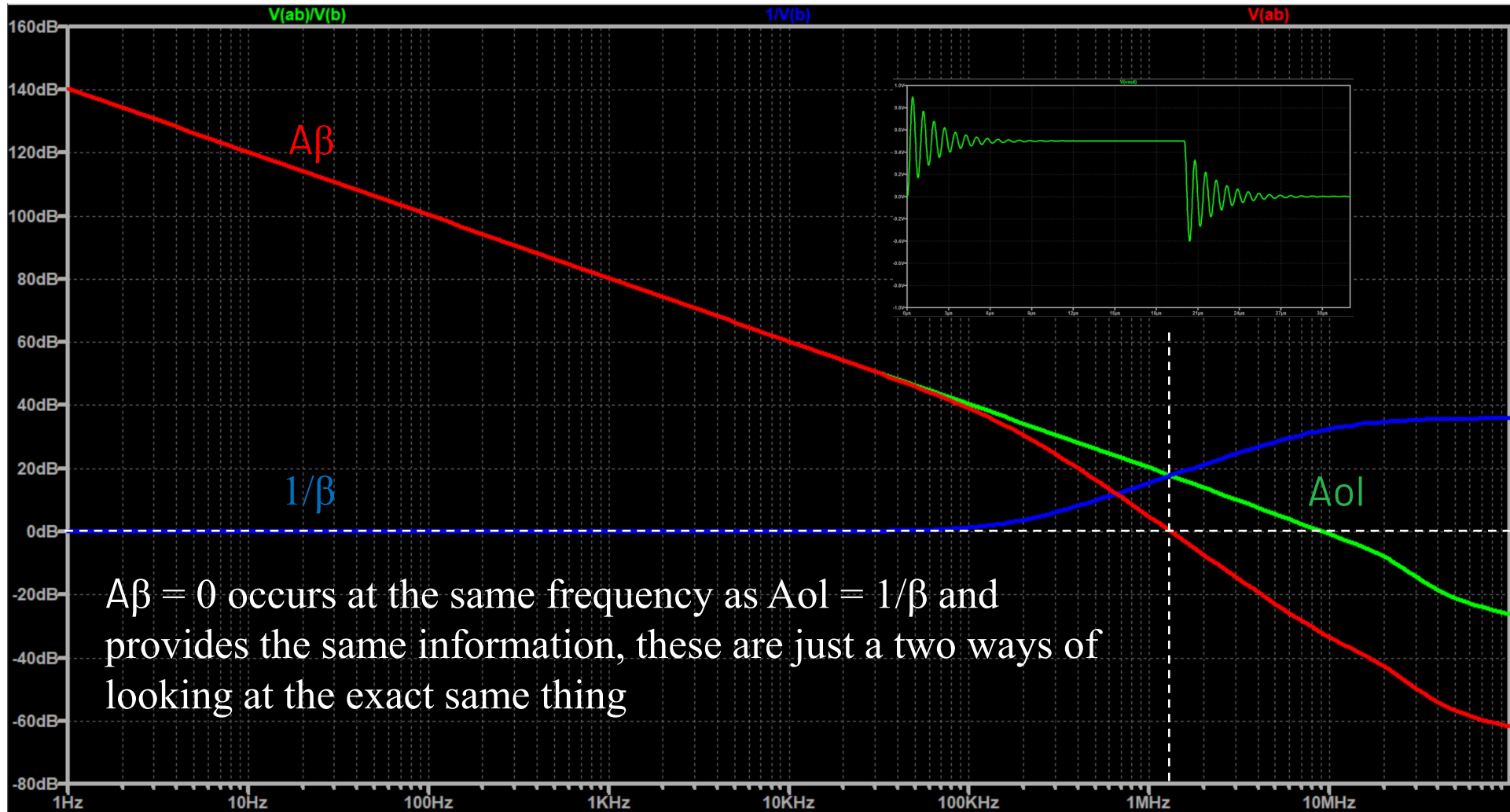
How Do You Simulate for Stability?



How Do You Simulate for Stability?



How Do You Simulate for Stability?



How Do You Simulate for Stability?

- ▶ Now that we know the problem, choose C_f per the following equations:

$$f_{COMP} = \sqrt{f_Z f_U}$$

f_Z = zero frequency as a result of the photodiode capacitance reacting with the feedback resistor

$$f_Z = \frac{1}{2\pi R_F C_{IN}}$$

f_U = unity gain frequency of the amplifier

$$C_F = \frac{1}{2\pi f_{COMP} R_F}$$

How Do You Simulate for Stability?

$$f_Z = \frac{1}{2\pi R_F C_{IN}} = \frac{1}{2\pi \times 10k\Omega \times 100pF} = 159kHz$$

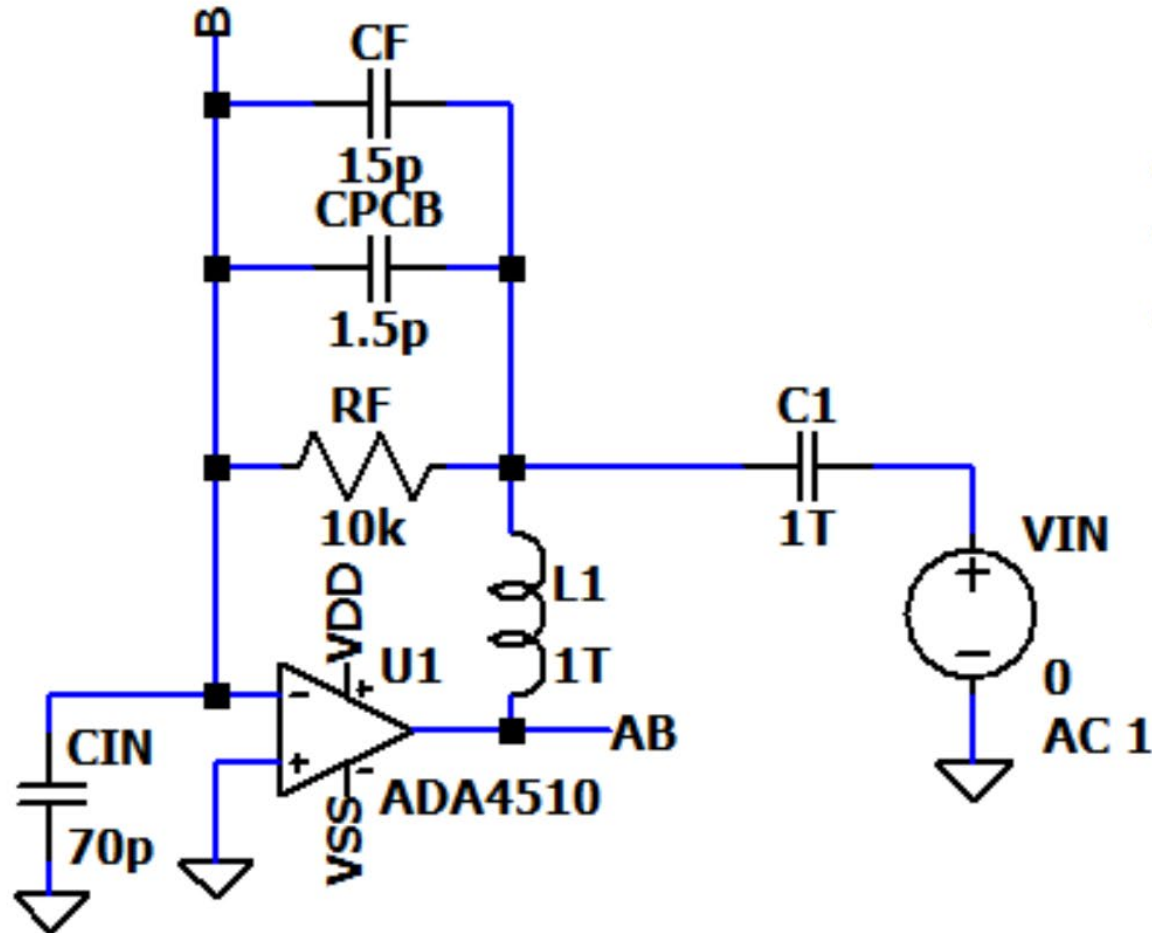
$$f_{COMP} = \sqrt{f_Z f_U} = \sqrt{159kHz \times 10MHz} = 1.26MHz$$

$$C_F = \frac{1}{2\pi f_{COMP} R_F} = \frac{1}{2\pi \times 1.26MHz \times 10k\Omega} = 12.6pF$$

100pF includes photodiode capacitance as well as input capacitance of the opamp

Since I used 15pF for the hardware, we shall simulate with 15pF

How Do You Simulate for Stability?

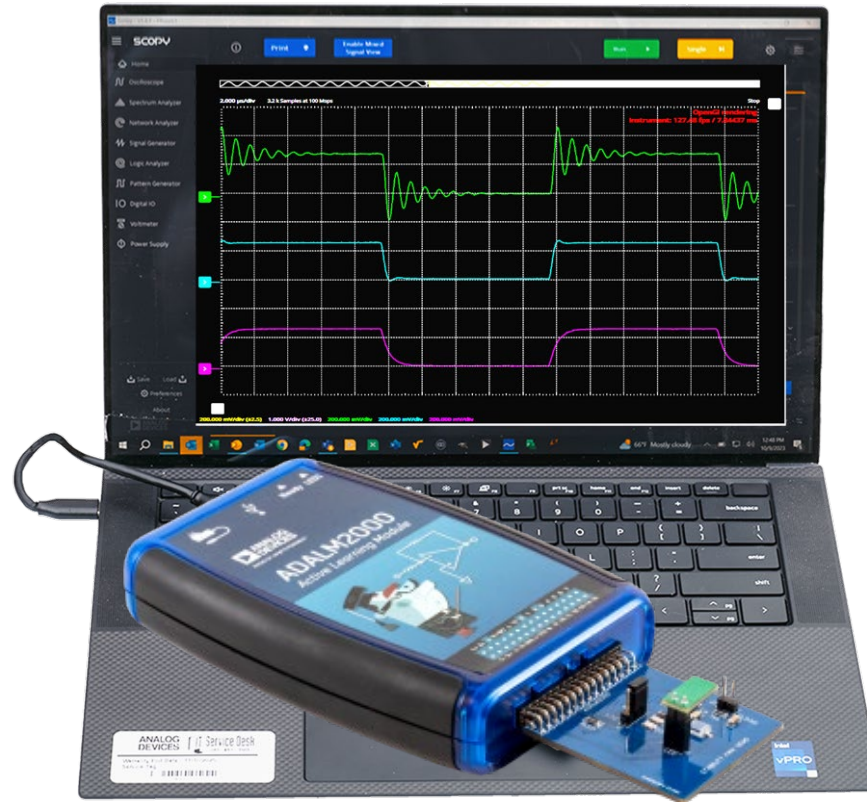


```
.op  
.ac dec 101 1 100MEG  
.options gfarad=0
```

How Do You Simulate for Stability?



Time for a Demo



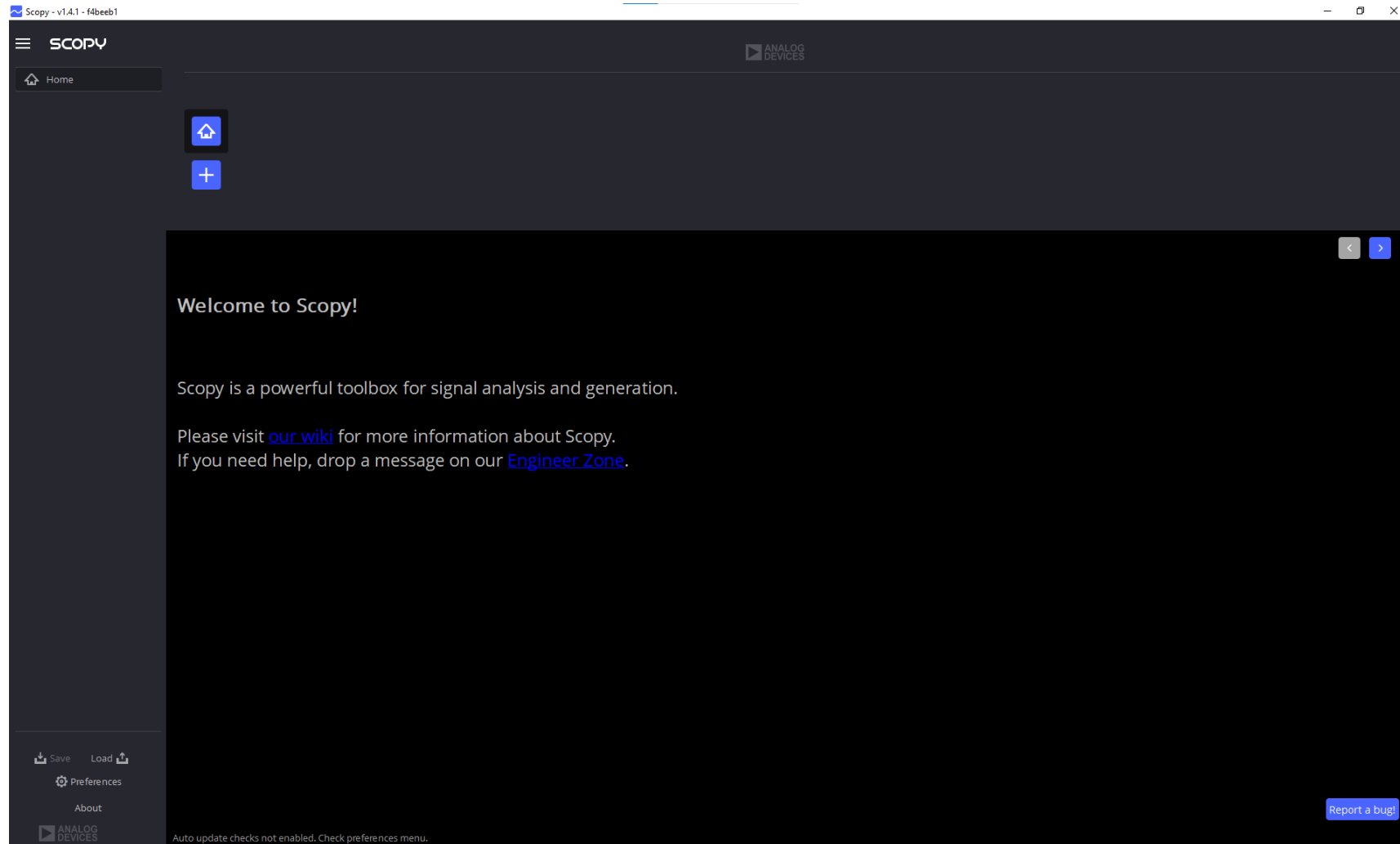
Physically Connect PCB to ADALM2k



Carefully align pins and insert firmly

ADALM2000 should be powered off when connecting or
disconnecting the PCB

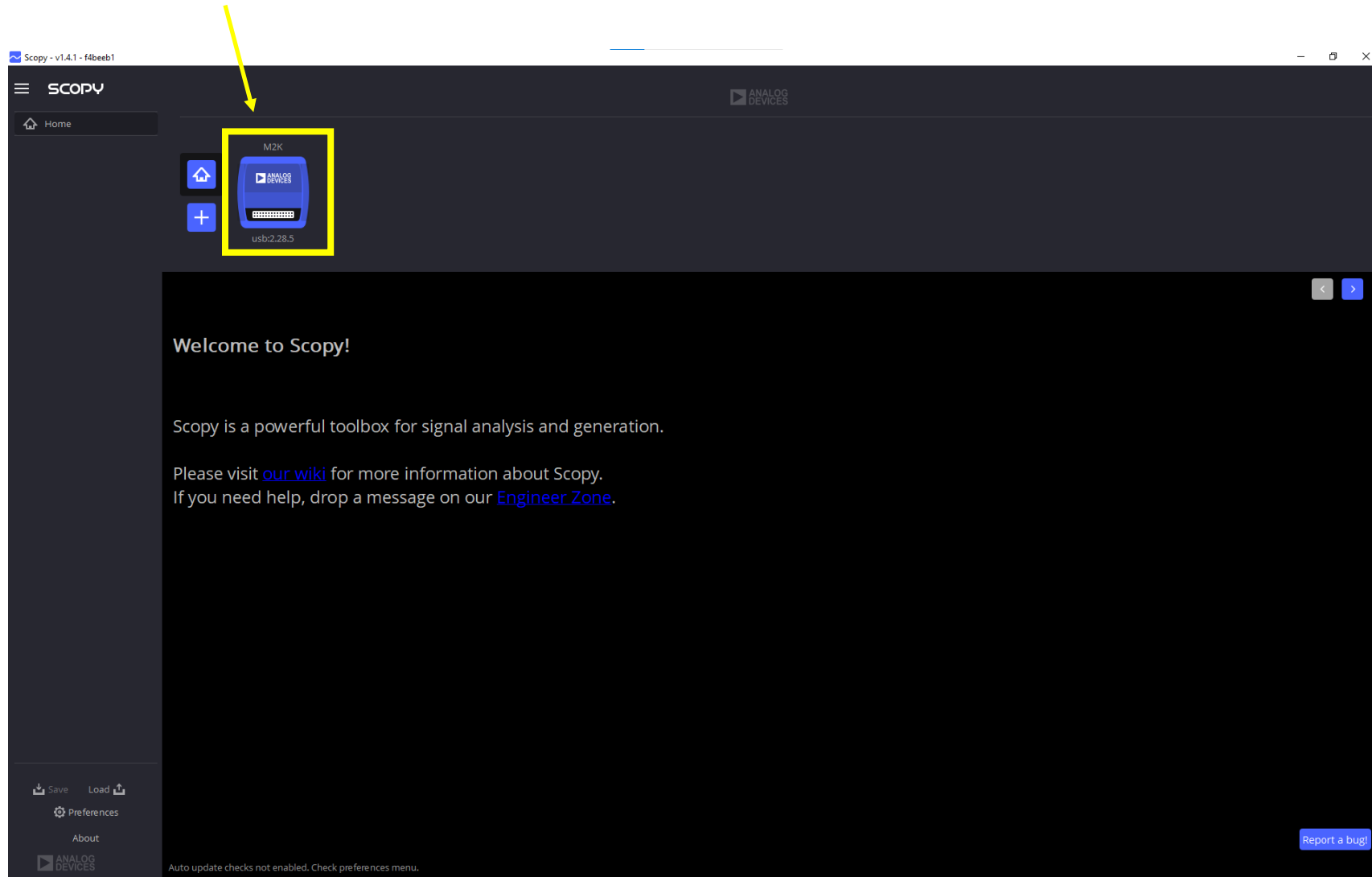
Launch the Scopy Software



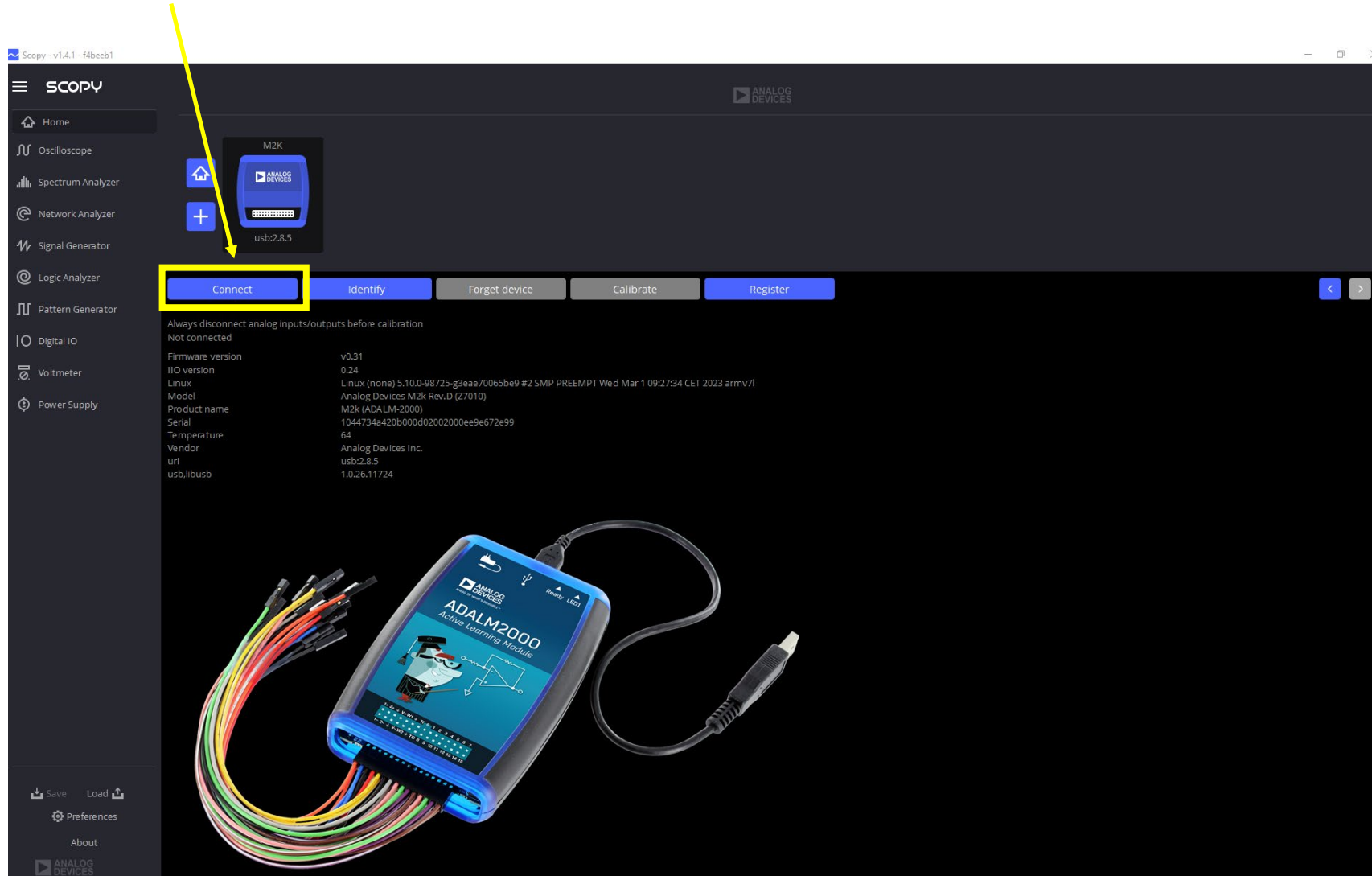
Physically Connect the ADALM2k to the Laptop



Click on the Icon



Click "Connect"




The screenshot shows the SCOPY software interface. A yellow arrow points to the 'Connect' button, which is highlighted with a yellow box. The interface displays the following information:

Always disconnect analog inputs/outputs before calibration
Not connected

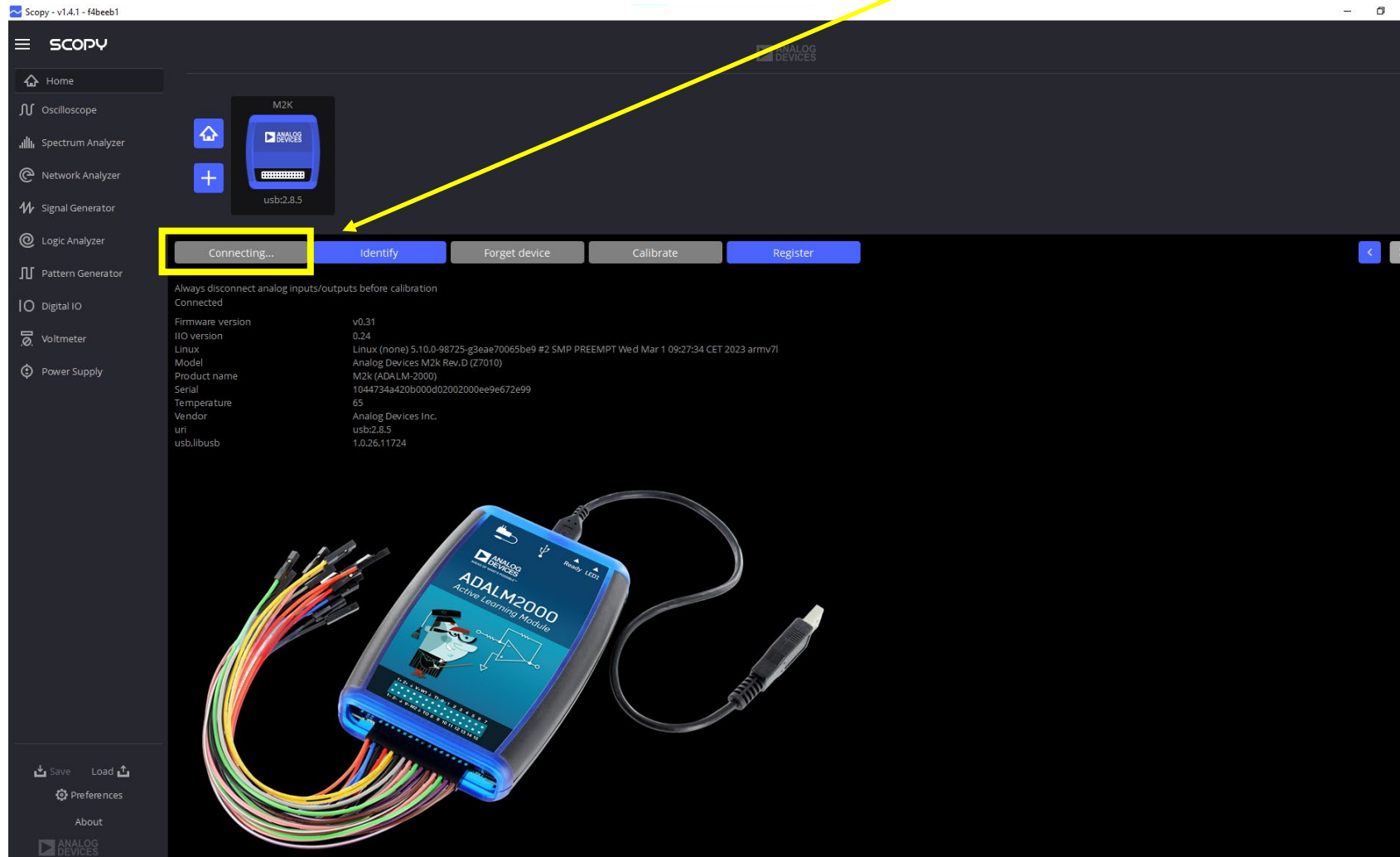
Firmware version	v0.31
I/O version	0.24
Linux	Linux (none) 5.10.0-98725-g3eae70065be9 #2 SMP PREEMPT Wed Mar 1 09:27:34 CET 2023 armv7l
Model	Analog Devices M2K Rev.D (Z7010)
Product name	M2K (ADALM-2000)
Serial	1044734a420b000d02002000ee9e672e99
Temperature	64
Vendor	Analog Devices Inc.
uri	usb2.8.5
usb.linux	1.0.26.11724

The interface also shows a list of tools on the left: Home, Oscilloscope, Spectrum Analyzer, Network Analyzer, Signal Generator, Logic Analyzer, Pattern Generator, Digital I/O, Voltmeter, and Power Supply. At the bottom, there are buttons for Save, Load, Preferences, and About.

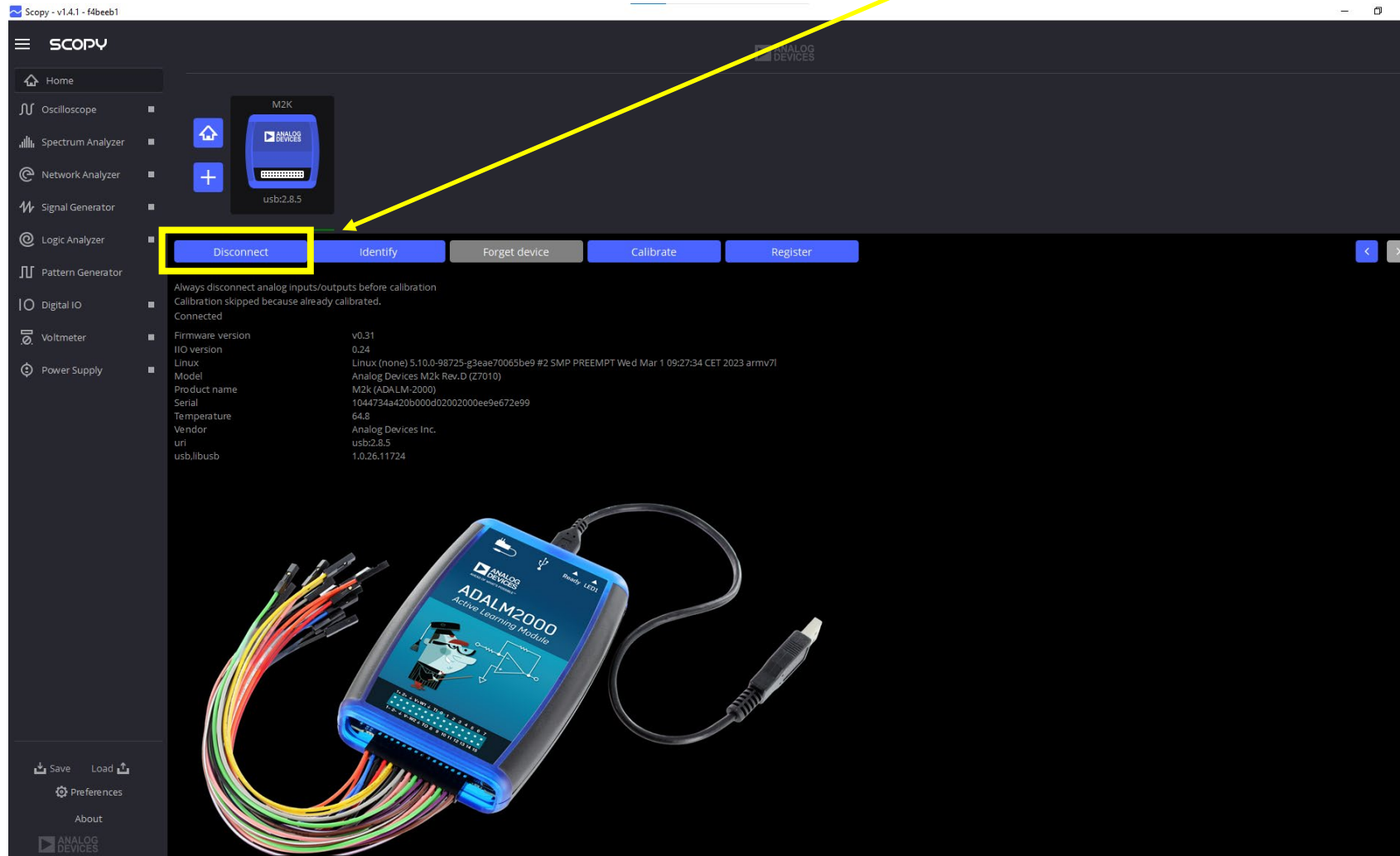


The image shows the ADALM2000 Active Learning Module, a blue USB device with a USB cable and a bundle of multi-colored cables connected to its front panel. The device has a screen displaying the Analog Devices logo and the text 'ADALM2000 Active Learning Module'.

The ADALM2k will Begin the Connection Process



Successful Connection Looks Like This



The screenshot shows the SCOPY software interface with the following elements:

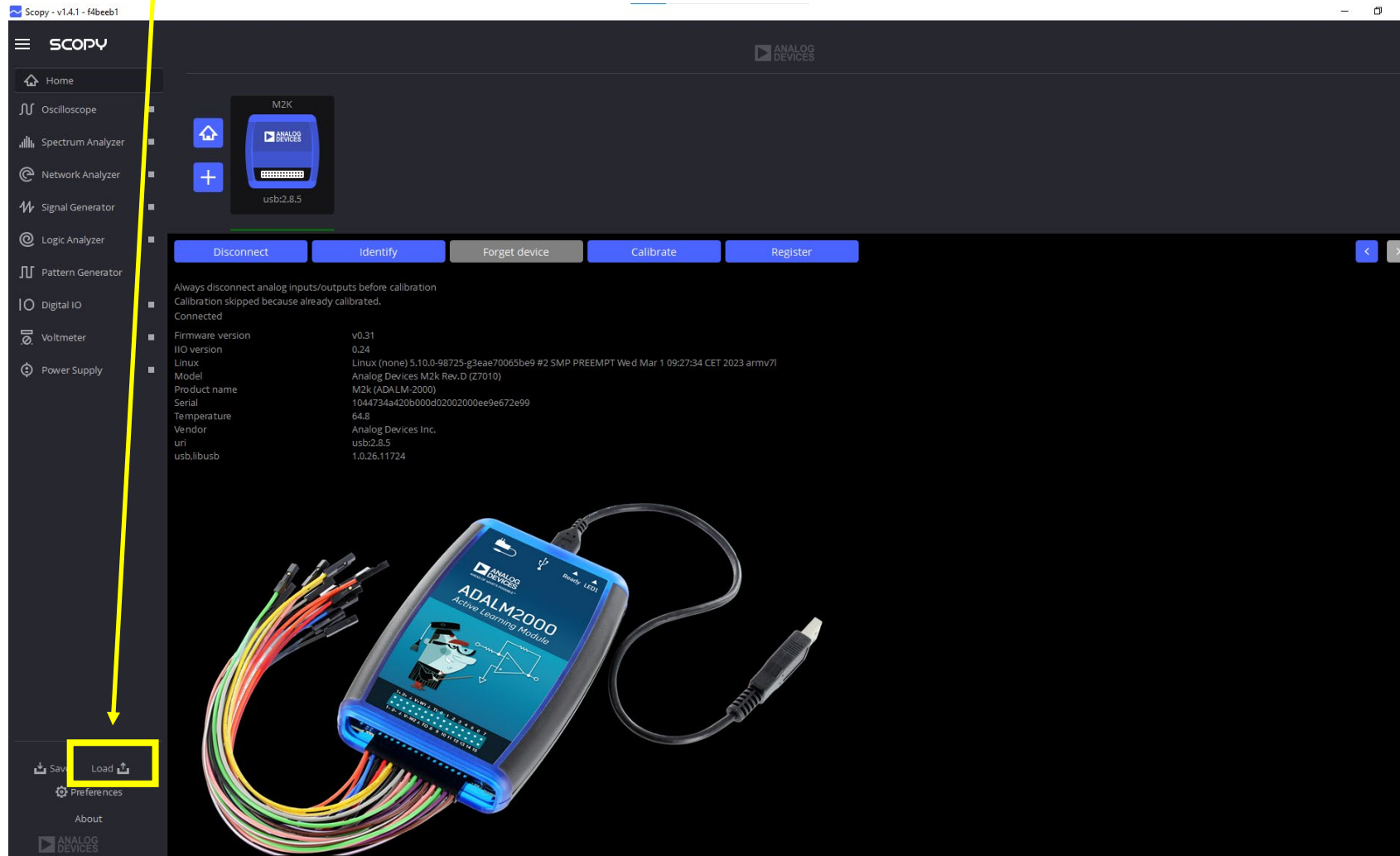
- Left sidebar: Home, Oscilloscope, Spectrum Analyzer, Network Analyzer, Signal Generator, Logic Analyzer, Pattern Generator, Digital IO, Voltmeter, Power Supply.
- Top right: ANALOG DEVICES logo.
- Device card: M2K, usb:2.8.5.
- Buttons: Disconnect (highlighted with a yellow box), Identify, Forget device, Calibrate, Register.
- Information panel:

Always disconnect analog inputs/outputs before calibration.
Calibration skipped because already calibrated.
Connected

Firmware version	v0.31
IIO version	0.24
Linux	Linux (none) 5.10.0-98725-g3eae70065be9 #2 SMP PREEMPT Wed Mar 1 09:27:34 CET 2023 armv7l
Model	Analog Devices M2K Rev.D (Z7010)
Product name	M2k (ADALM-2000)
Serial	T044734a420b000d02002000ee9e672e99
Temperature	64.8
Vendor	Analog Devices Inc.
uri	usb:2.8.5
usb.libusb	1.0.26.11724
- Bottom left: Save, Load, Preferences, About.

Below the screenshot is a photograph of the ADALM2000 Active Learning Module, a blue device with a screen and various ports. It is connected to a bundle of multi-colored cables and a power cable.

Load the Config Files



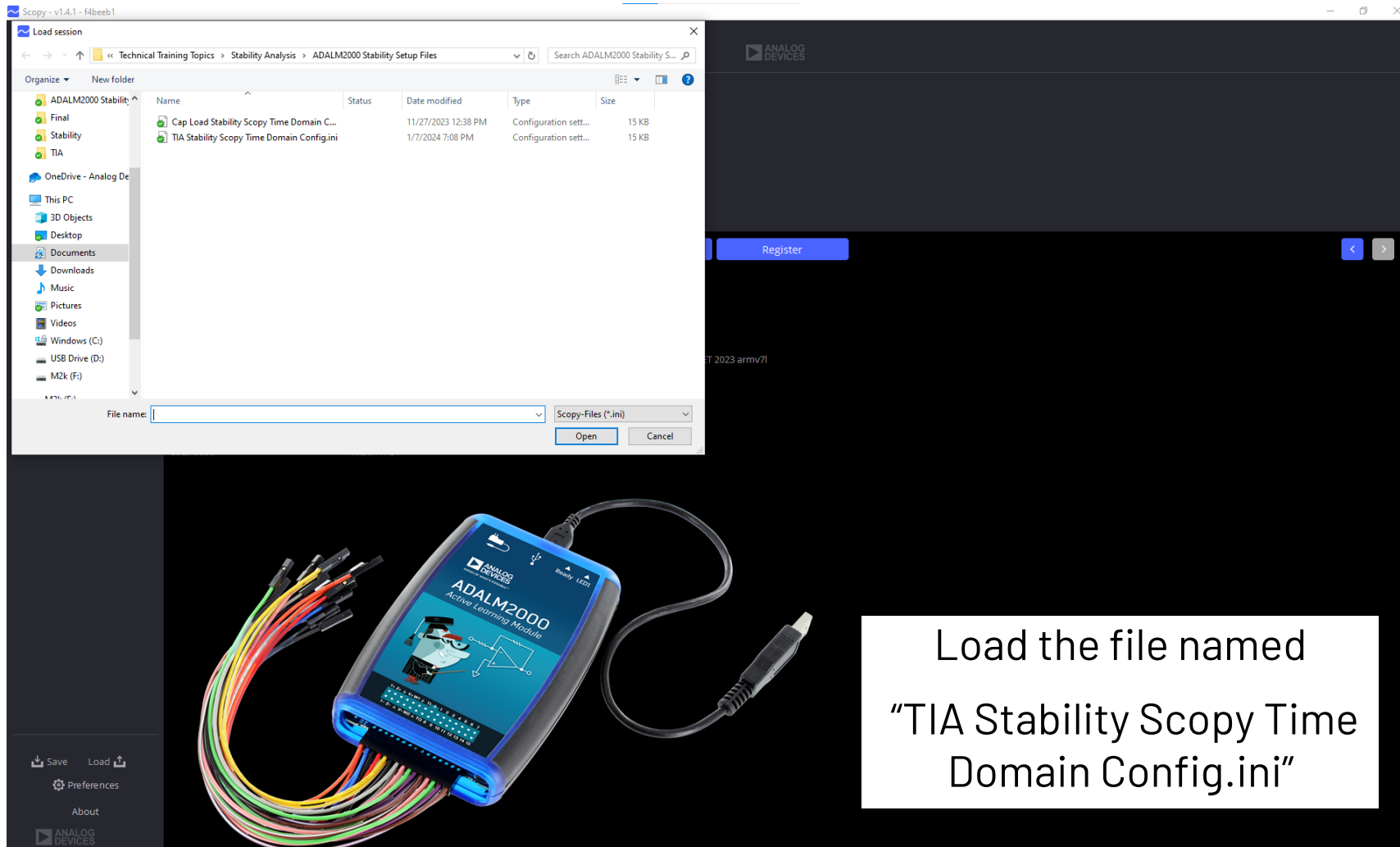
The screenshot shows the SCOPY software interface. On the left sidebar, the 'Load' button is highlighted with a yellow box and a yellow arrow. The main window displays the following information:

Device Information:

- Device: M2K
- usb:2.8.5
- Buttons: Disconnect, Identify, Forget device, Calibrate, Register
- Always disconnect analog inputs/outputs before calibration.
- Calibration skipped because already calibrated.
- Connected
- Firmware version: v0.31
- IIO version: 0.24
- Linux: Linux (none) 5.10.0-98725-g3eae70065be9 #2 SMP PREEMPT Wed Mar 1 09:27:34 CET 2023 armv7l
- Model: Analog Devices M2K Rev.D (Z7010)
- Product name: M2k (ADALM-2000)
- Serial: T044734a420b000d02002000ee9e672e99
- Temperature: 64.8
- Vendor: Analog Devices Inc.
- uri: usb:2.8.5
- usb.libus: 1.0.26.11724

Hardware: ADALM2000 Active Learning Module (Analog Devices logo, USB symbol, Round LED)

Navigate to the Config File Location



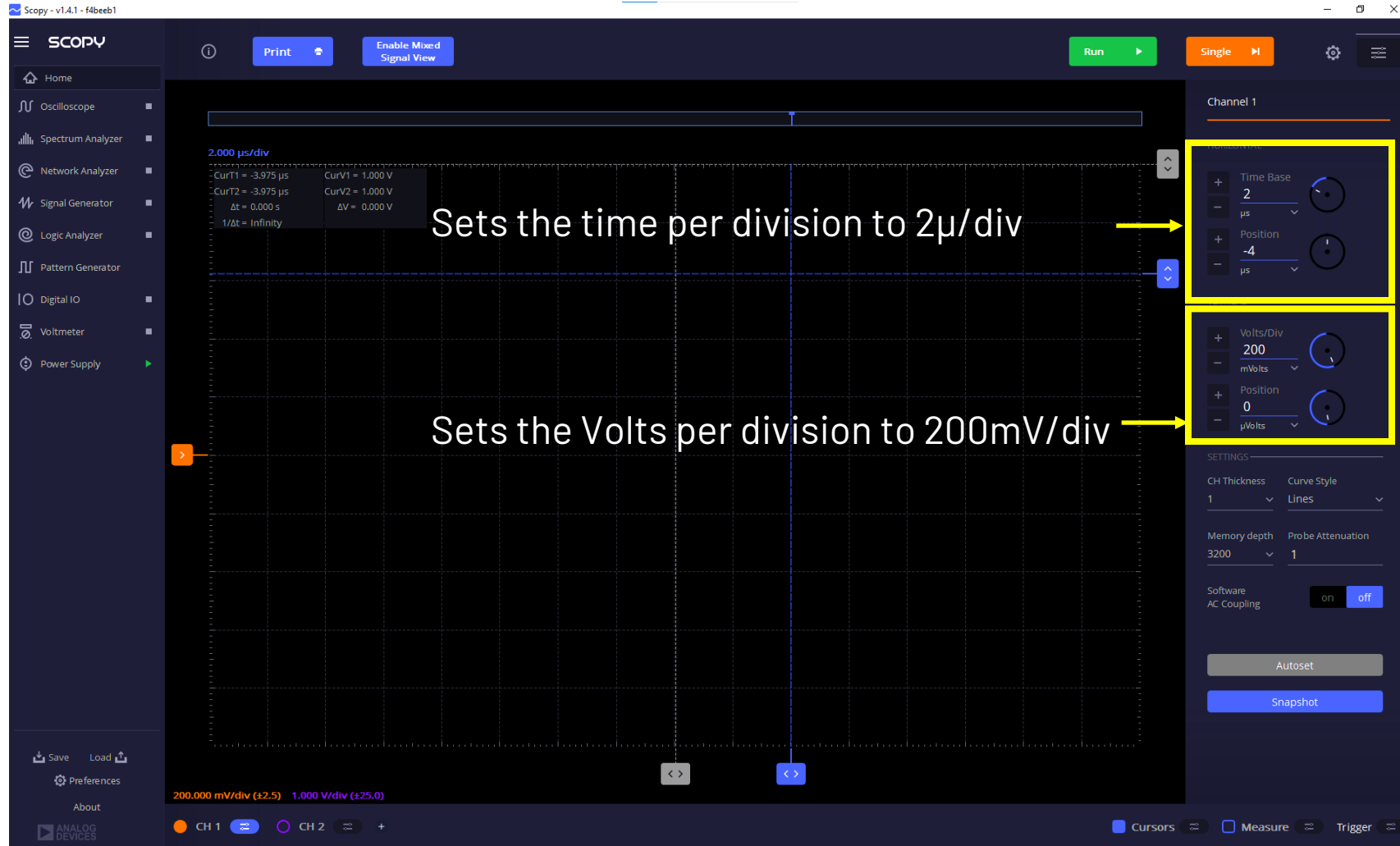
The image shows a Windows File Explorer window titled "Scopy - v1.4.1 - f4beeb1" with the address bar set to "Technical Training Topics > Stability Analysis > ADALM2000 Stability Setup Files". The file list contains two files:

Name	Status	Date modified	Type	Size
Cap Load Stability Scopy Time Domain C...		11/27/2023 12:38 PM	Configuration sett...	15 KB
TIA Stability Scopy Time Domain Config.ini		1/7/2024 7:08 PM	Configuration sett...	15 KB

The software interface in the background features a "Register" button and a hardware device, the ADALM2000 Active Learning Module, which is a blue and black device with a screen and multiple colored cables connected to its ports.

Load the file named
"TIA Stability Scopy Time
Domain Config.ini"

The O-Scope Will be Configured as Shown



SCOPE - v1.4.1 - f4beeb1

Print Enable Mixed Signal View Run Single

Channel 1

2.000 $\mu\text{s}/\text{div}$

CurT1 = -3.975 μs CurV1 = 1.000 V
CurT2 = -3.975 μs CurV2 = 1.000 V
 $\Delta t = 0.000$ s $\Delta V = 0.000$ V
1/ $\Delta t = \text{Infinity}$

Sets the time per division to $2\mu/\text{div}$

Sets the Volts per division to 200mV/div

Channel 1 Settings:

- Time Base: 2 μs
- Position: -4 μs
- Volts/Div: 200 mVolts
- Position: 0 μVolts

SETTINGS

- CH Thickness: 1
- Curve Style: Lines
- Memory depth: 3200
- Probe Attenuation: 1
- Software AC Coupling: on/off

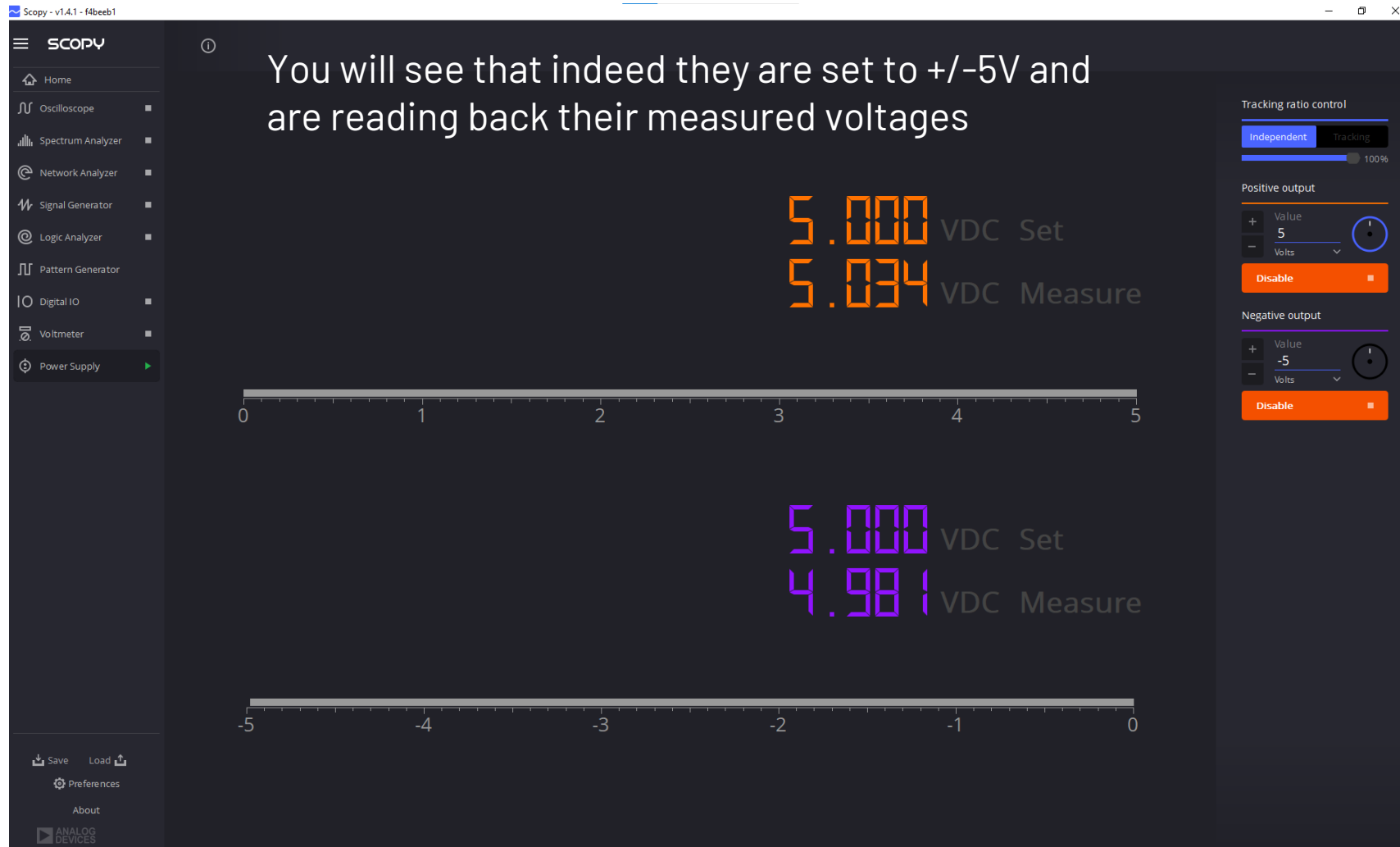
Autoset Snapshot

200.000 mV/div (± 2.5) 1.000 V/div (± 25.0)

CH 1 CH 2

Cursors Measure Trigger

If You Click on the Power Supply Label



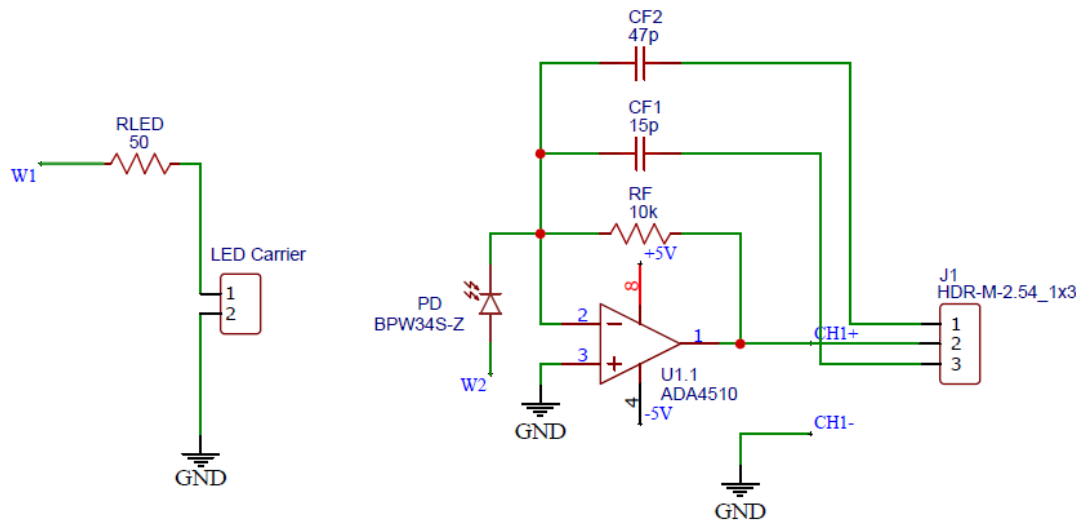
The screenshot displays the SCOPY software interface for a power supply. The main display area shows two voltage readings: a setpoint of 5.000 VDC and a measured value of 5.034 VDC. Below this, a second setpoint of 5.000 VDC and a measured value of 4.981 VDC are shown. The interface includes a sidebar with navigation options like Home, Oscilloscope, Spectrum Analyzer, Network Analyzer, Signal Generator, Logic Analyzer, Pattern Generator, Digital IO, Voltmeter, and Power Supply. On the right, there are controls for Tracking ratio control (Independent/Tracking), Positive output (set to 5 Volts), and Negative output (set to -5 Volts). A horizontal scale at the bottom ranges from -5 to 0.

You will see that indeed they are set to +/-5V and are reading back their measured voltages

5.000 VDC Set
5.034 VDC Measure

5.000 VDC Set
4.981 VDC Measure

TIA Schematic



$$f_{COMP} = \sqrt{f_Z f_U}$$

f_Z = zero frequency as a result of the photodiode capacitance reacting with the feedback resistor

$$f_Z = \frac{1}{2\pi R_F C_{IN}}$$

f_U = unity gain frequency of the amplifier

$$C_F = \frac{1}{2\pi f_{COMP} R_F}$$

Assume no jumpers are installed

What is f_U ?

What is f_Z ?

What is f_{COMP} ?

What is the ROC?

Is the Circuit Stable or Unstable?

Now assume the parasitic $C_F = 1.5\text{pf}$

What changed?

Can you draw any conclusions?

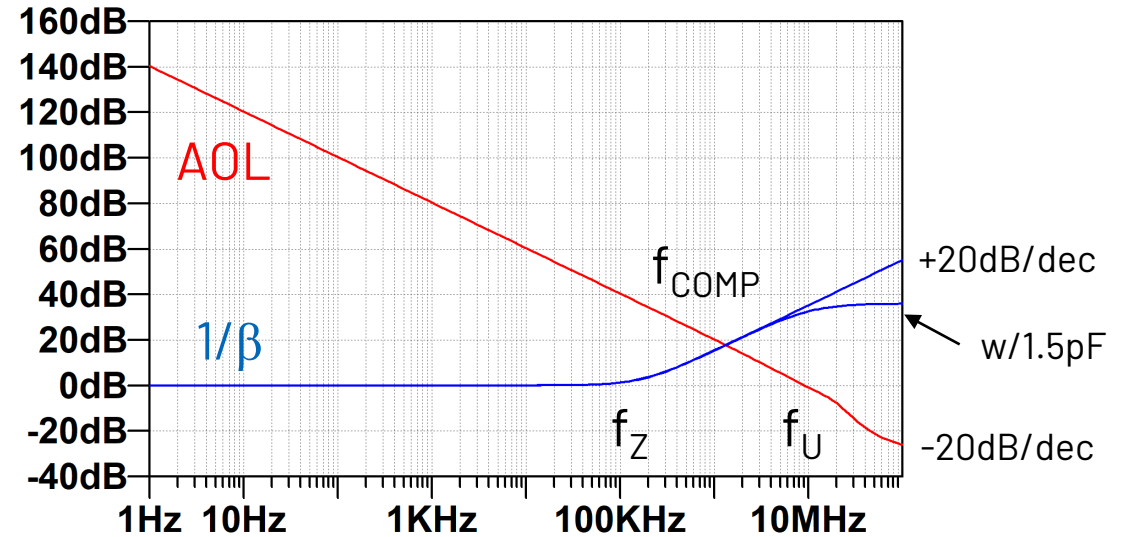
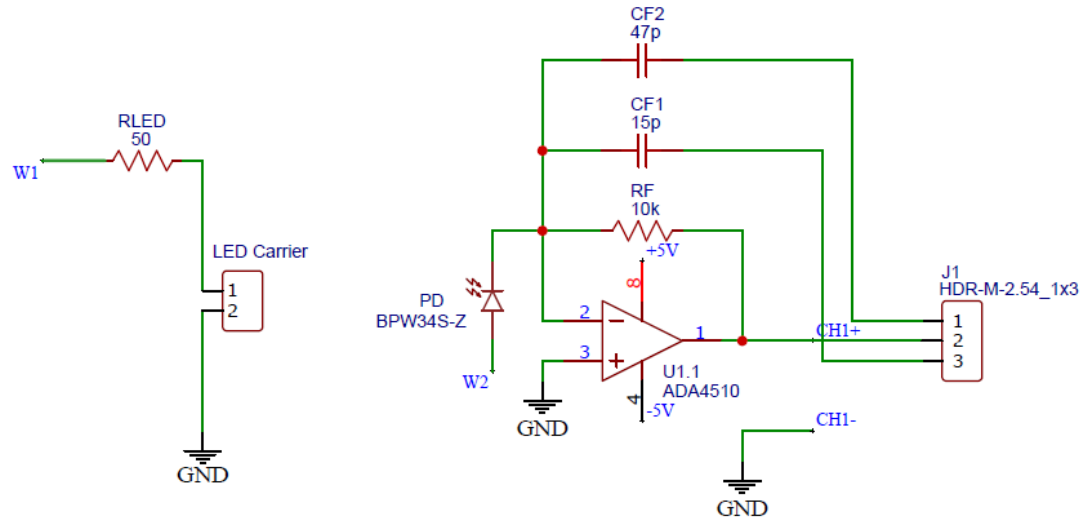
Precision, Low-Noise, 10MHz Opamp: ADA4510

Input Bias Current	Noise Spectral Density	Unity Gain Frequency	Input Capacitance
10 pA (max)	5nV/ $\sqrt{\text{Hz}}$	10.4 MHz	Differential: 20 pF Common-mode: 2pF

Large Area Photodiode: BPW34

Active Area	Spectral Range	Capacitance @ $V_R=0V$	Dark Current @ $V_R=0V$
2.65 x 2.65 mm ²	420 - 1120 nM	72 pF	200pA

TIA Schematic

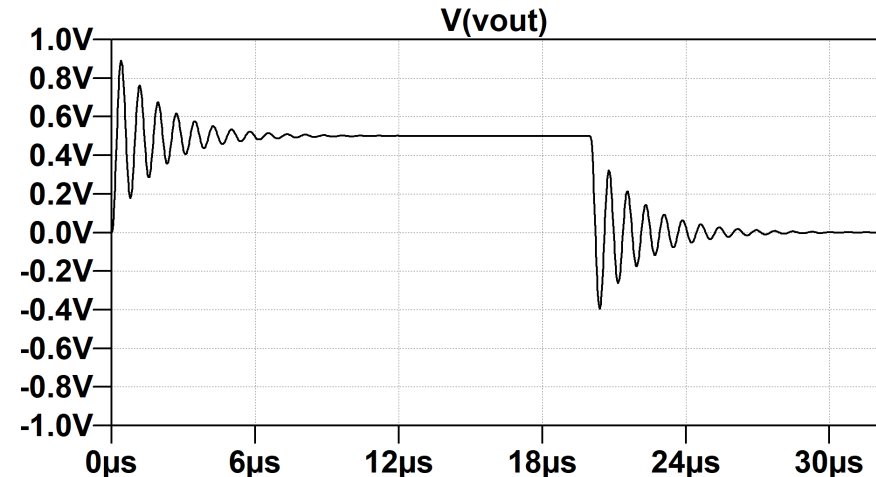


Precision, Low-Noise, 10MHz Opamp: ADA4510

Input Bias Current	Noise Spectral Density	Unity Gain Frequency	Input Capacitance
10 pA (max)	5nV/ $\sqrt{\text{Hz}}$	10.4 MHz	Differential: 20 pF Common-mode: 2pF

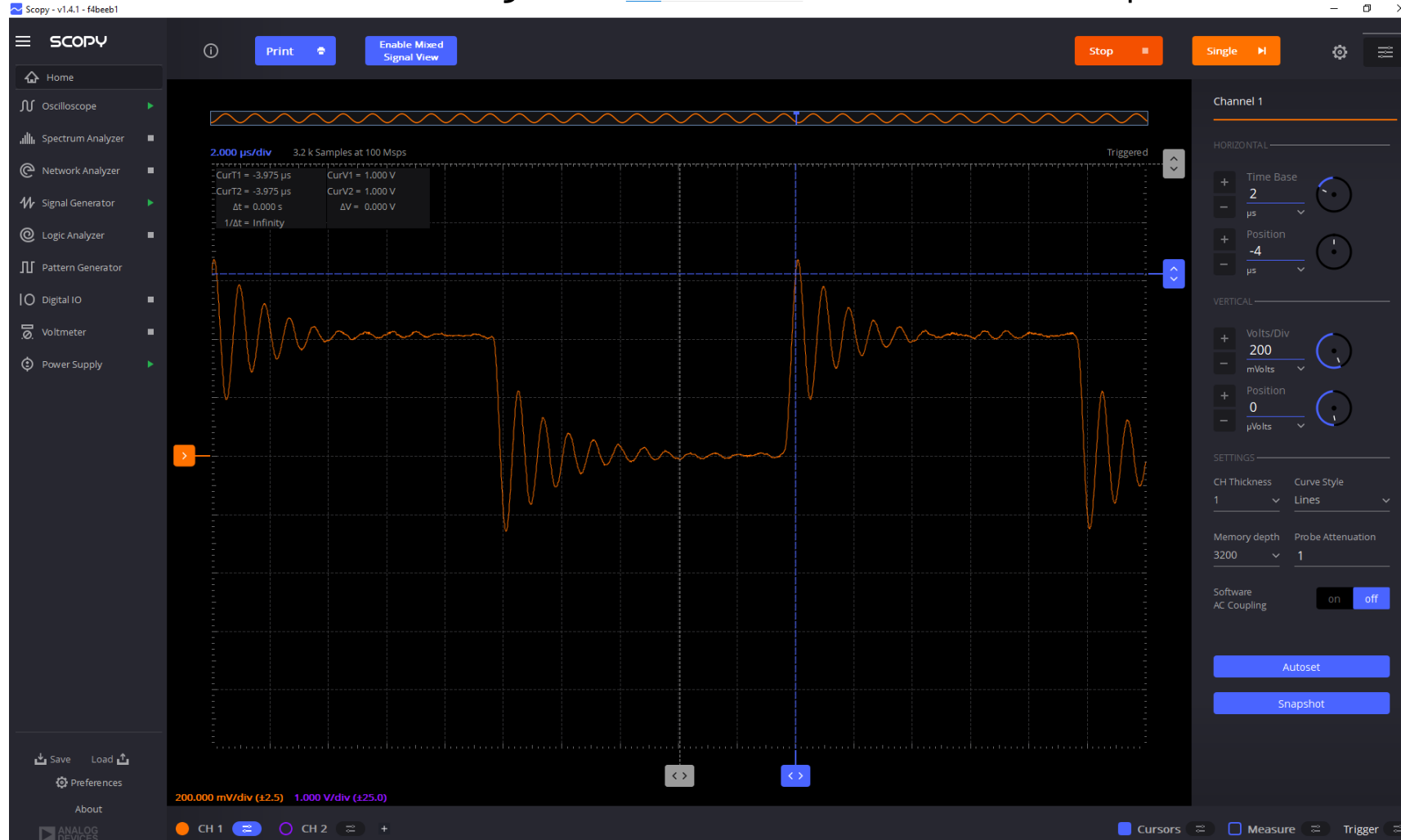
Large Area Photodiode: BPW34

Active Area	Spectral Range	Capacitance @ $V_R=0V$	Dark Current @ $V_R=0V$
2.65 x 2.65 mm ²	420 - 1120 nM	72 pF	200pA

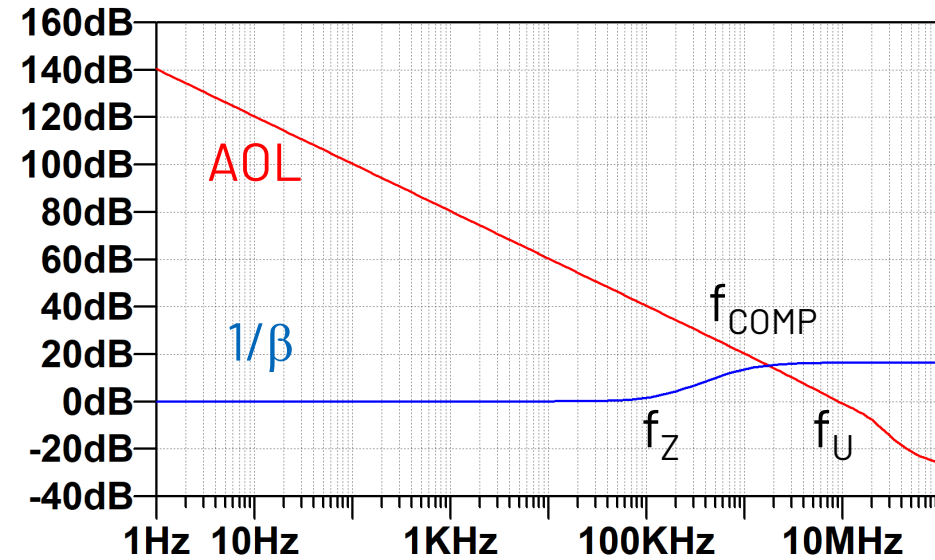
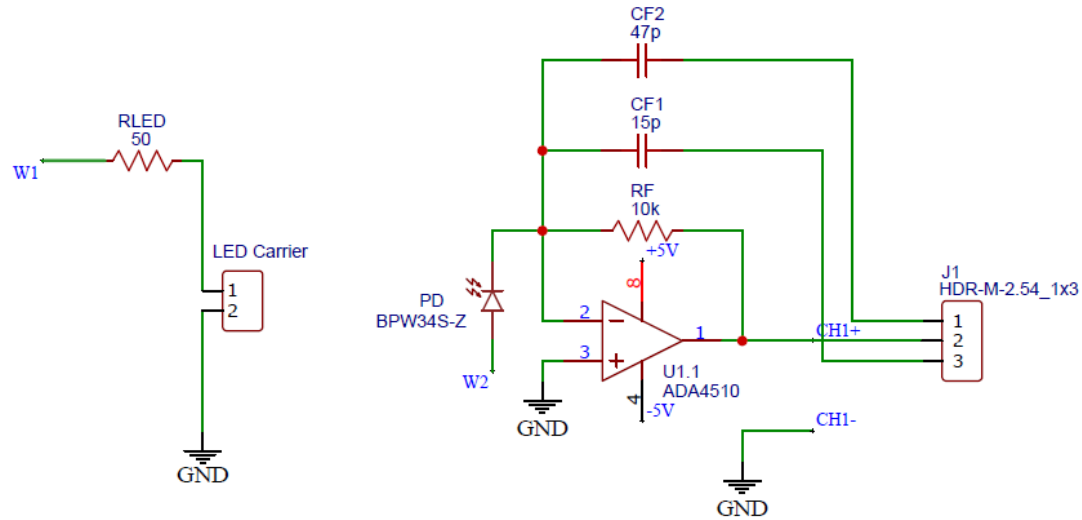


Remove the Jumper

Enable the Signal Generator and the Oscilloscope



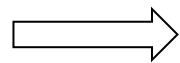
Let's Compensate for 45° of Phase Margin



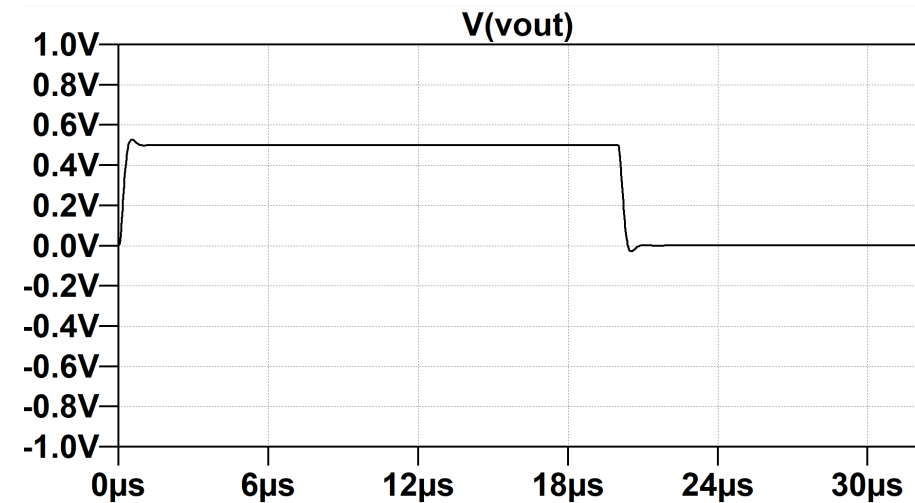
$$f_U \approx 10\text{MHz}$$

$$f_Z \approx 150\text{ kHz}$$

$$f_{\text{COMP}} = 1.2\text{ MHz}$$



$$C_F \approx 15\text{pF}$$

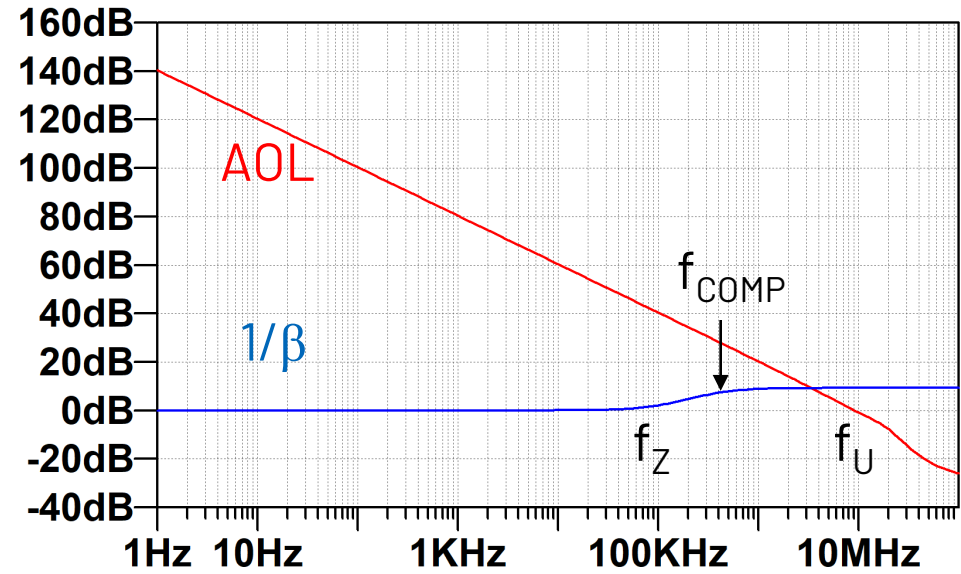
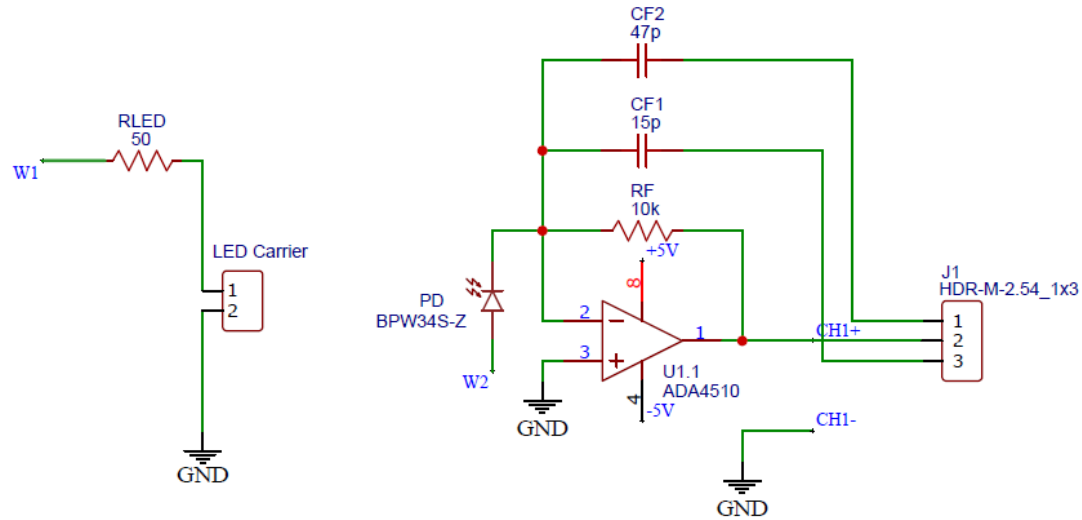


Place the Jumper for 45°

Adjust the trigger level as needed



Let's Overcompensate the Circuit

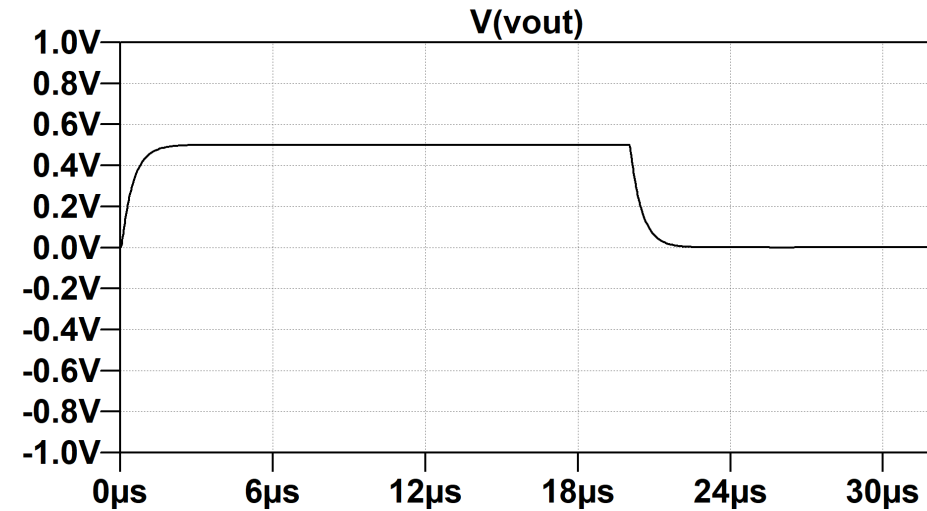


$$f_U \approx 10\text{MHz}$$

$$f_Z \approx 150\text{kHz}$$

$$C_F = 47\text{pF}$$

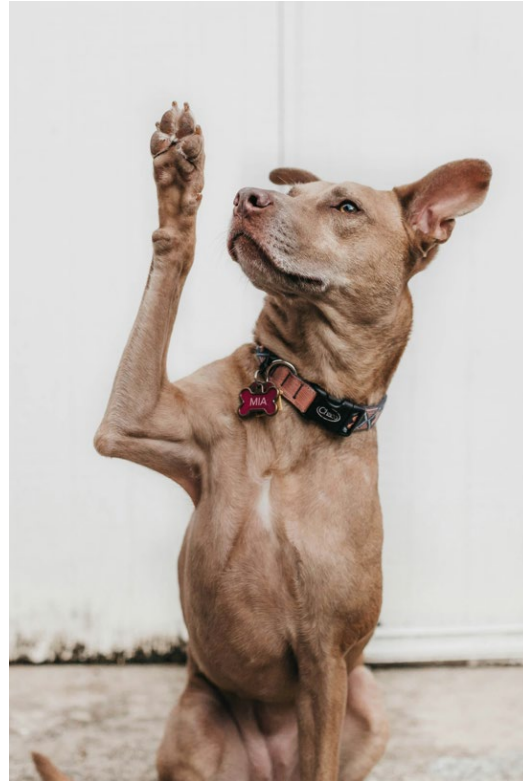
$$\longrightarrow f_{\text{COMP}} \approx 350\text{kHz}$$



Place the Jumper for $>70^{\circ}$



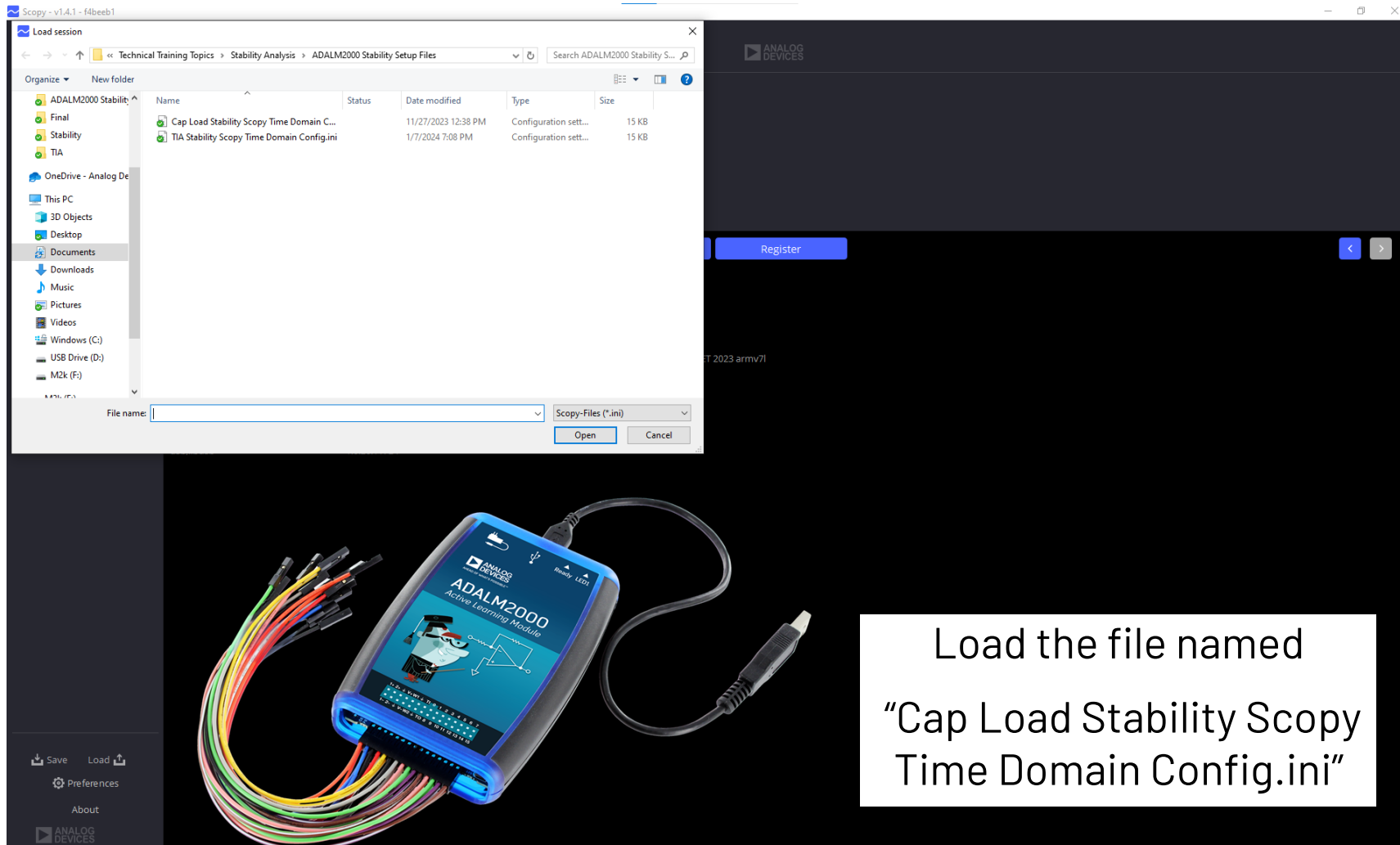
Questions?



Driving Capacitive Loads



Demo Time - Navigate to the Config File Location



The screenshot shows a Windows File Explorer window titled "Scopy - v1.4.1 - f4beeb1" with the address bar set to "Technical Training Topics > Stability Analysis > ADALM2000 Stability Setup Files". The file list contains two files:

Name	Status	Date modified	Type	Size
Cap Load Stability Scopy Time Domain C...		11/27/2023 12:38 PM	Configuration sett...	15 KB
TIA Stability Scopy Time Domain Config.ini		1/7/2024 7:08 PM	Configuration sett...	15 KB

The background image shows the ADALM2000 Active Learning Module, a blue device with a screen and various ports, connected to a multi-colored cable and a USB cable. A white text box in the bottom right of the screenshot contains the instruction:

Load the file named
"Cap Load Stability Scopy
Time Domain Config.ini"

The 0-Scope Will be Configured as Shown

The screenshot displays the SCOPE software interface. The main window shows an oscilloscope with two channels. Channel 1 (orange) shows a sine wave, and Channel 2 (purple) shows a square wave. The time base is set to 1.000 $\mu\text{s}/\text{div}$ and the volts per division is set to 100 mV/div. The interface includes a sidebar with various analysis tools, a top bar with controls like 'Print', 'Enable Mixed Signal View', 'Stop', and 'Single', and a right-hand panel for channel settings. Two yellow boxes highlight the 'Time Base' and 'Volts/Div' settings in the Channel 2 configuration panel. Arrows point from text annotations to these settings.

1.000 $\mu\text{s}/\text{div}$ 1.6 k Samples at 100 Msps

Cur1 = 78.35 μs CurV1 = 1.000 V
Cur2 = -8.264 μs CurV2 = 1.000 V
 $\Delta t = 0.000 \text{ s}$ $\Delta V = 0.000 \text{ V}$
1/ $\Delta t = \text{Infinity}$

Sets the time per division to 1 $\mu\text{s}/\text{div}$

Sets the Volts per division to 100mV/div

Channel 2

HORIZONTAL

Time Base: 1 μs

Position: -4 μs

VOLTS/DIV

Volts/Div: 100 mVolts

Position: 0 μVolts

SETTINGS

CH Thickness: 1 Curve Style: Lines

Memory depth: 1600 Probe Attenuation: 1

Software AC Coupling: on off

Autoset

Snapshot

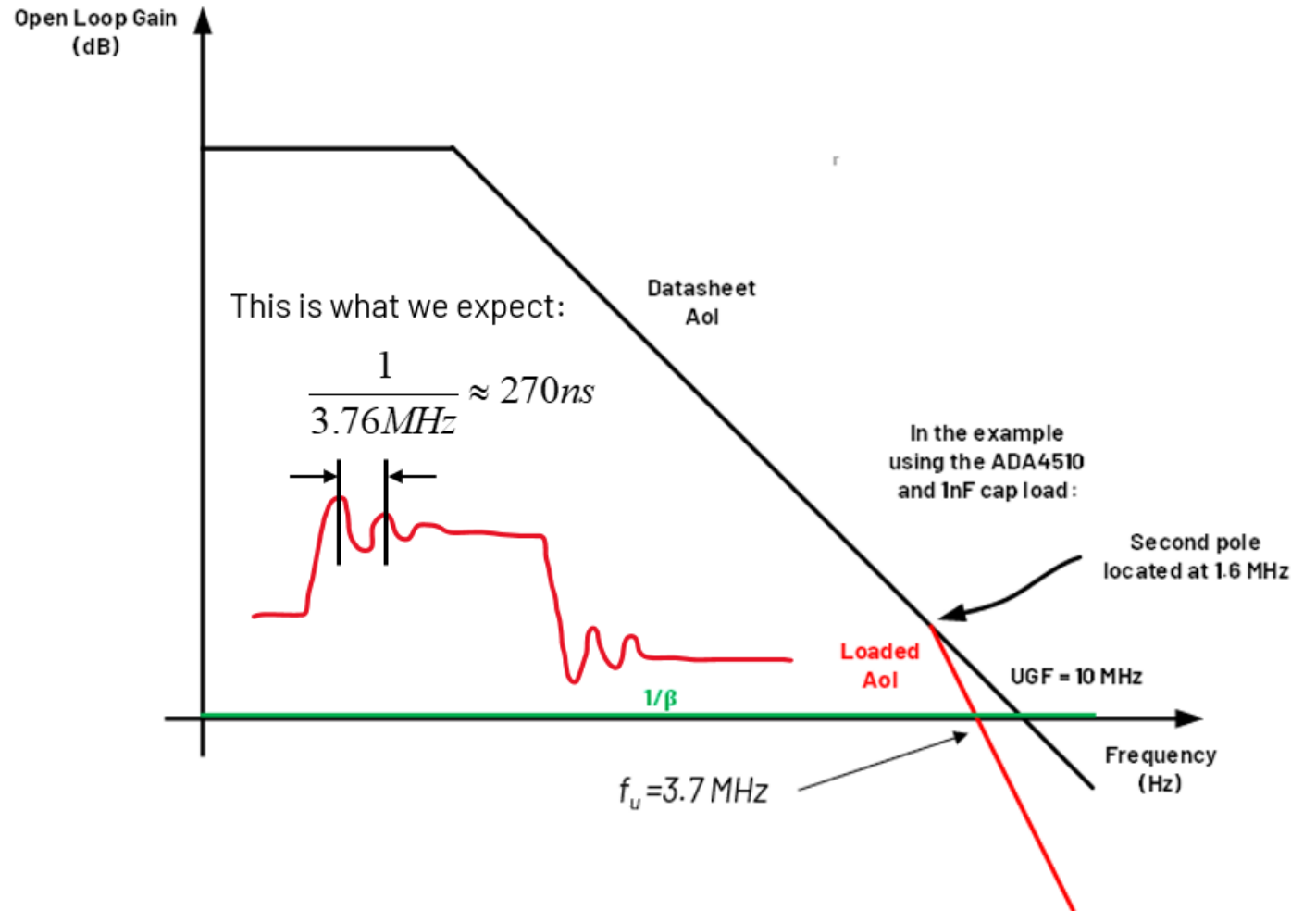
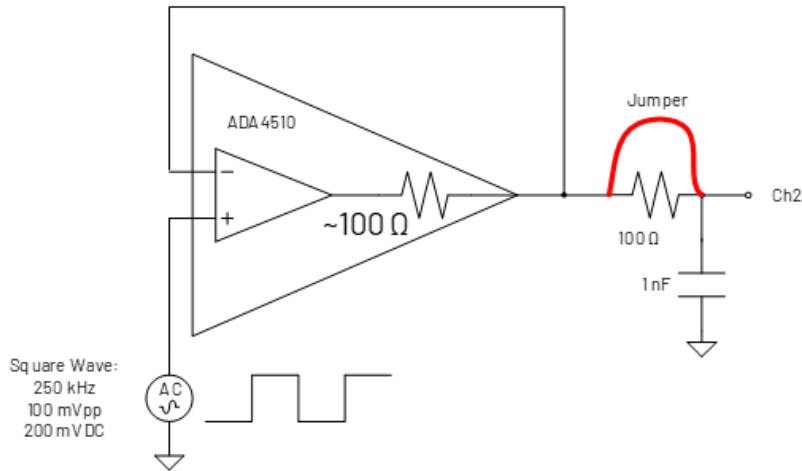
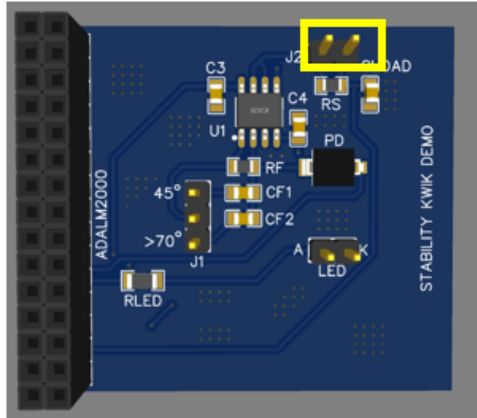
200 mV/div (± 2.5) 100 mV/div (± 2.5)

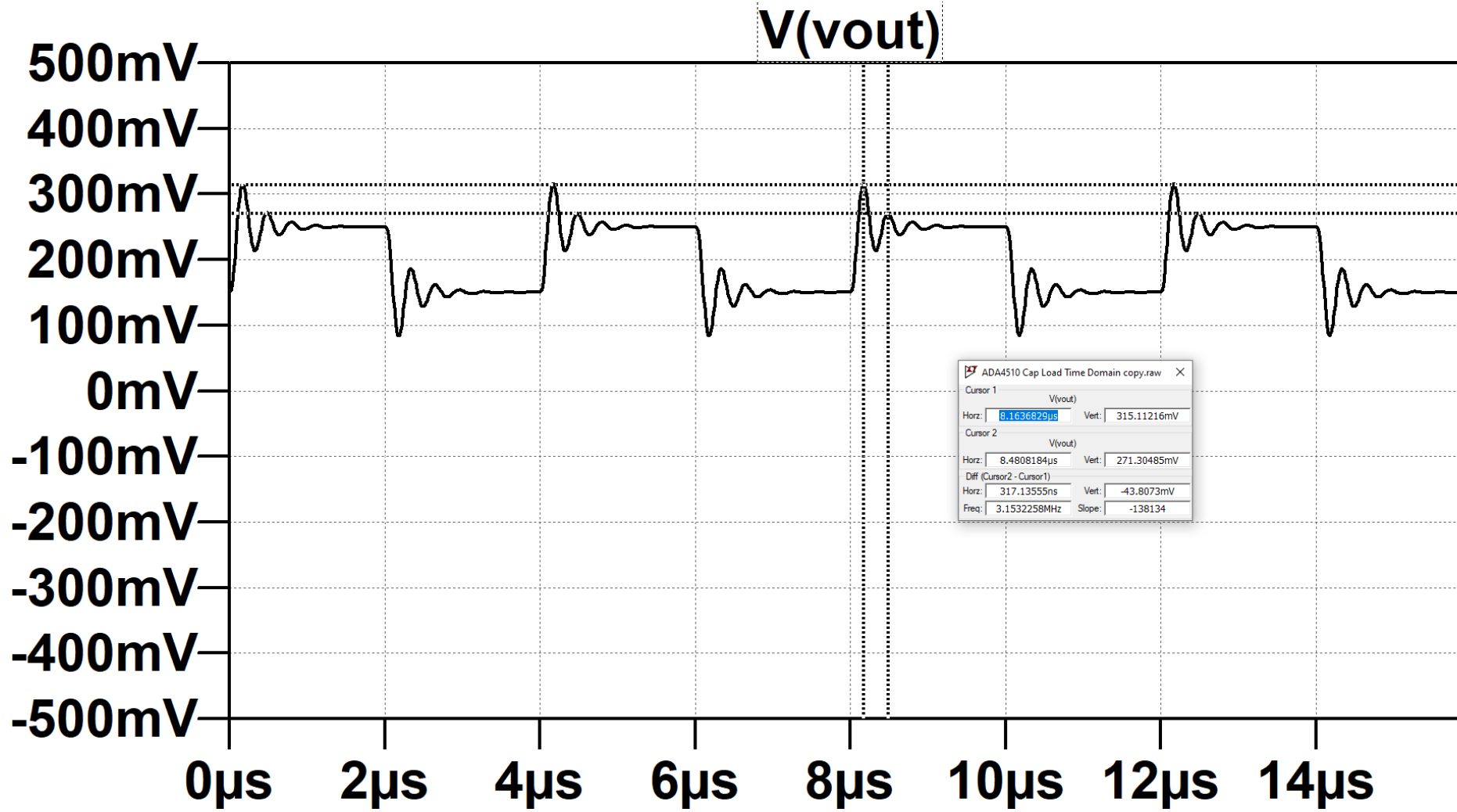
CH 1 CH 2

Cursors Measure Trigger

Let's Configure the Hardware

Place jumper at J2



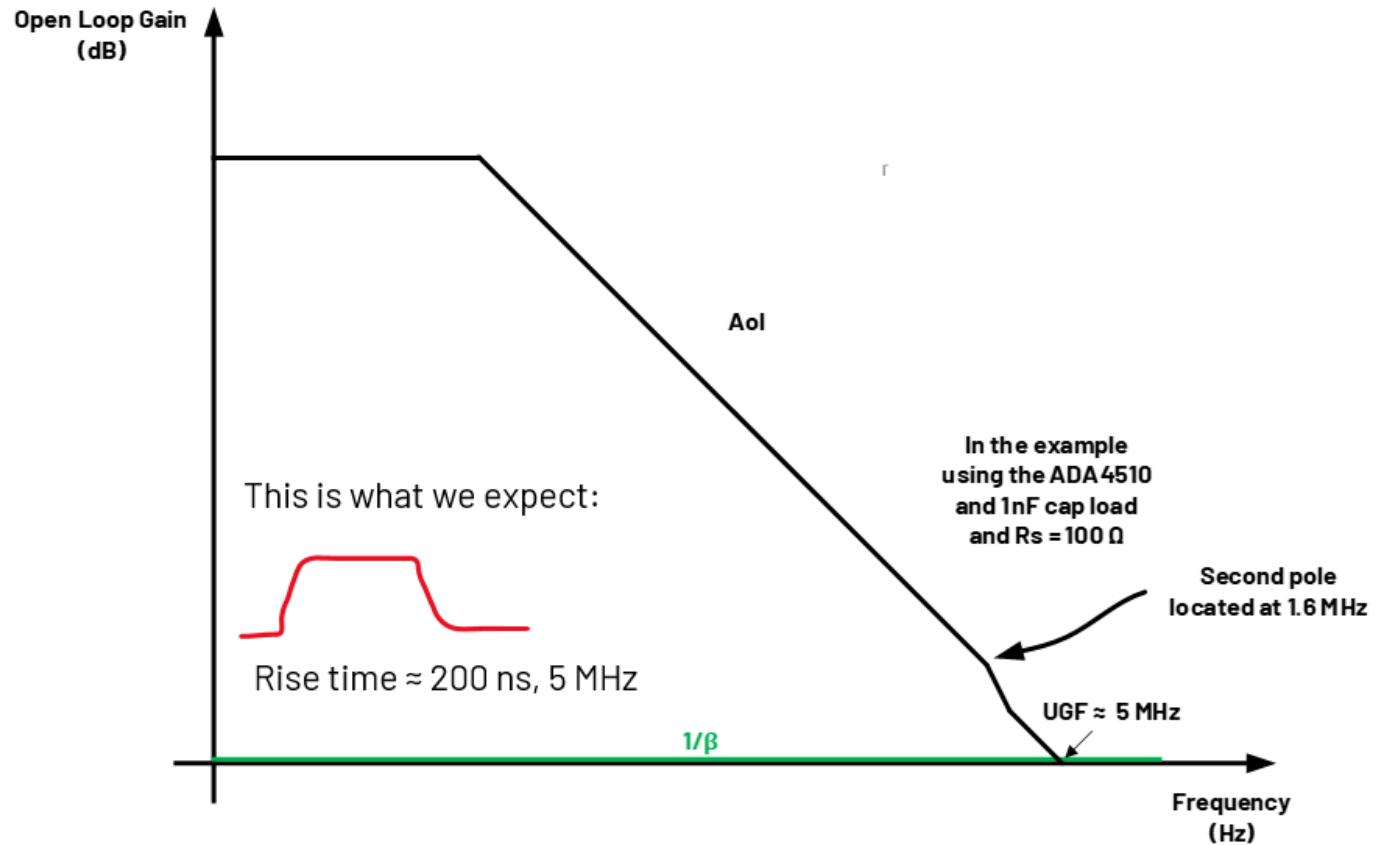
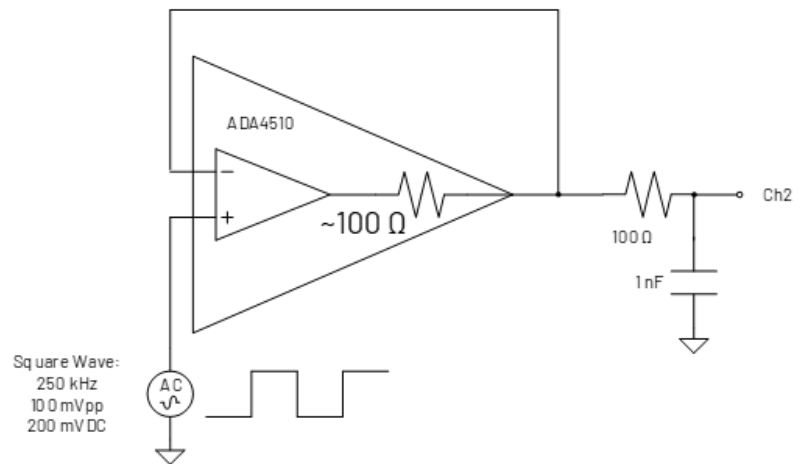
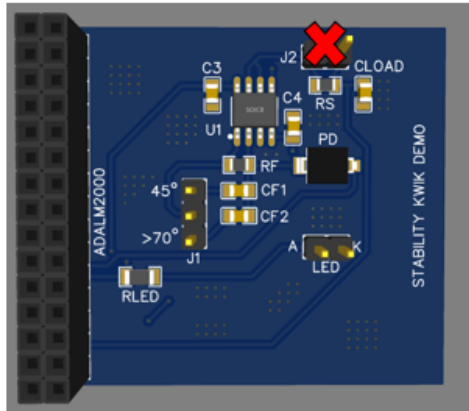


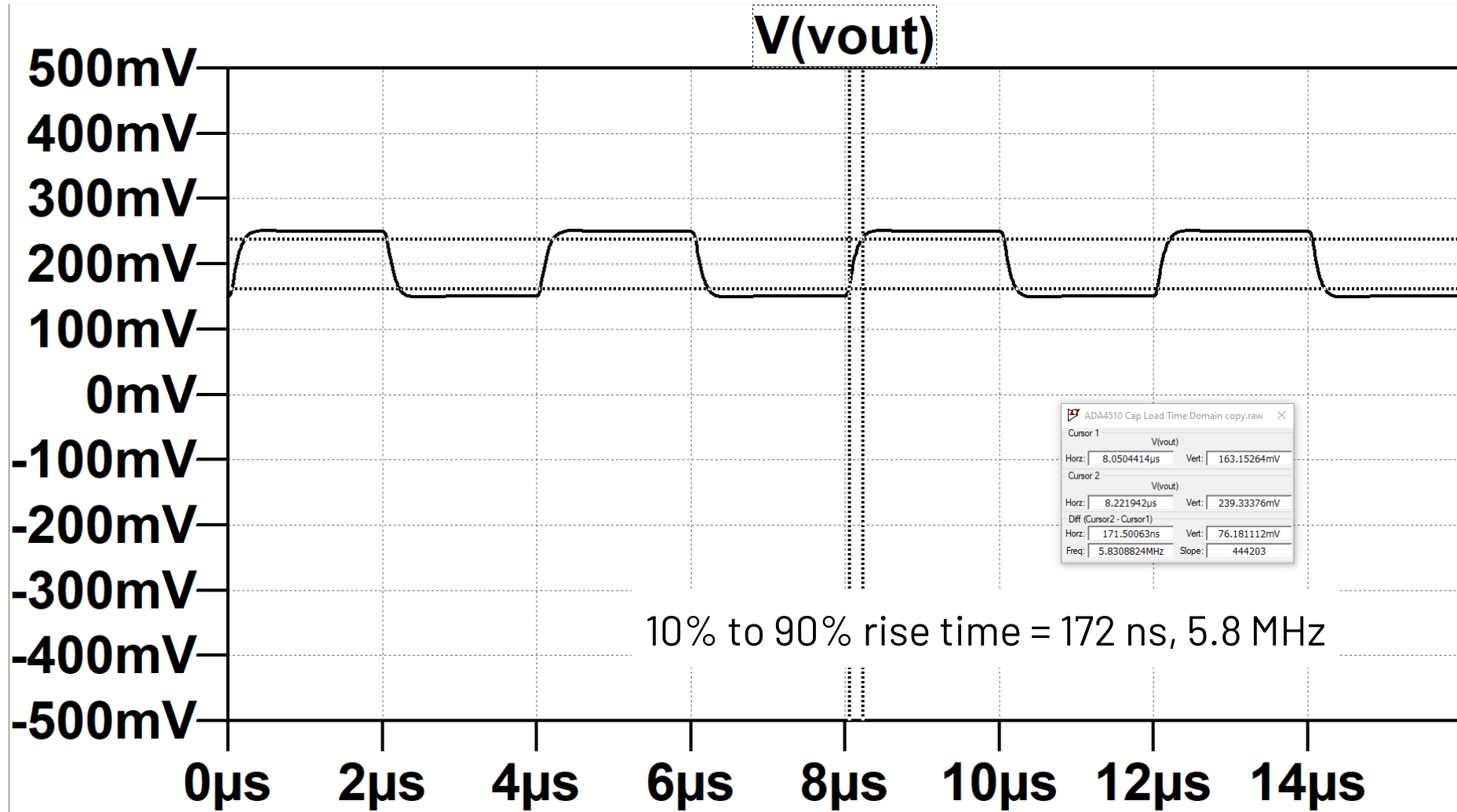
ADALM2k Results



Let's Configure the Hardware

Remove jumper at J2





ADALM2k Results



THANK YOU

