Quick Start Guide for testing the AD6673 Analog-to-Digital Converter (ADC) Customer Evaluation Board Using the FPGA based Capture Board HSC-ADC-EVALEZ

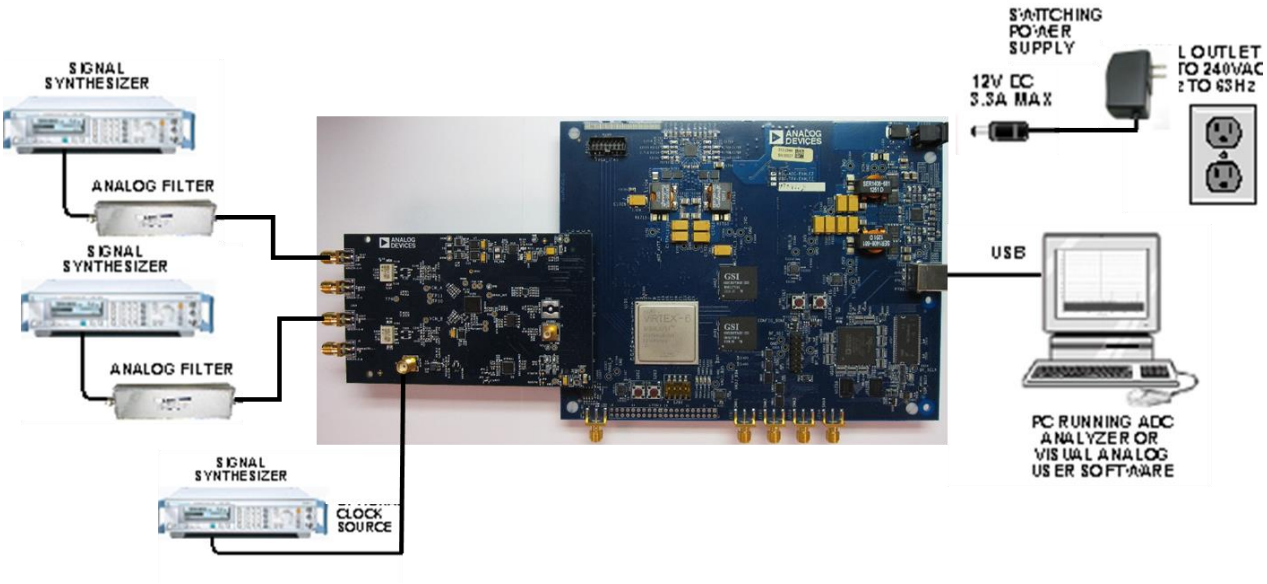


Figure 1: AD6673 Evaluation Board with HSC-ADC-EVALEZ Data Capture Board

Equipment Needed

- ► Analog signal source and anti-aliasing filter
- ► Analog Clock Source
- ► PC
- ► USB 2.0 port recommended (USB 1.1-compatible)
- ► AD6673 customer evaluation board (AD6673-EBZ)
- ► HSC-ADC-EVALEZ FPGA Based Data Capture Board

Documents Needed

- ► AD6673 Datasheet
- ► VisualAnalog Converter Evaluation Tool User Manual, AN-905
- ► High Speed ADC SPI Control Software User Manual, AN-878
- ► Interfacing to High Speed ADCs via SPI, AN-877

Software Needed

- ► VisualAnalog
- ► SPIController

All documents and software are available at http://www.analog.com/fifo.
For any questions please send an email to highspeed.converters@analog.com**.**

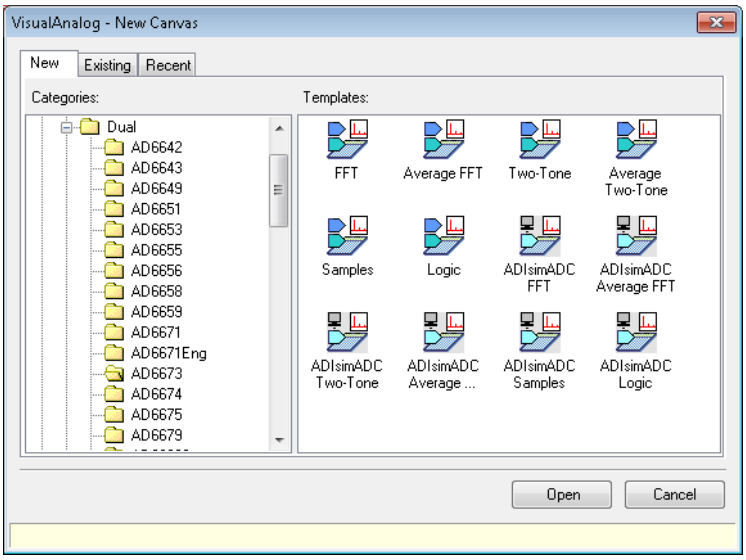
Install software from the ADI website

1. Download and install **VisualAnalog** software, Rev 1.9.46.9 or later.
2. Download and install **SPI Controller** software, Rev 4.0.11.4640 or later.

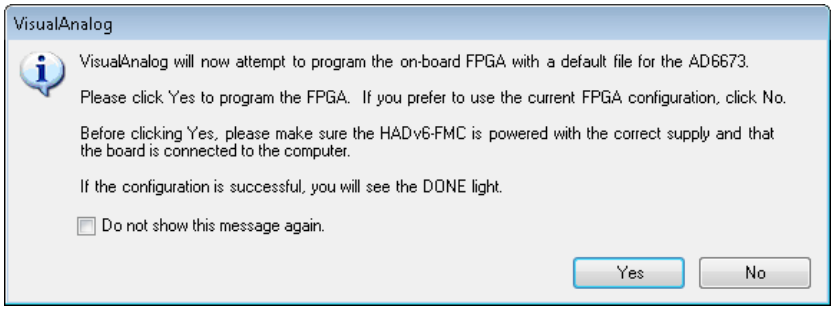
Setup hardware and software

1. Connect the AD6673 EVB and the HSC-ADC-EVALEZ board together as shown in Figure 1.
2. Connect one 12V, 3.3A switching power supply (such as the V-Infinity ETSA120330UDC-P5P-SZ supplied) to the HSC-ADC-EVALEZ board. Note: Make sure the 12V power supply is used.
3. Connect the HSC-ADC-EVALEZ board to the PC with a USB cable. (Connect to P702.)
4. On the AD6673 EVB, provide a clean, low jitter clock source to the connector labeled *CLKIN* at the desired ADC conversion rate with power level set between 10dBm and 14dBm.
5. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the analog input at connector J100 (Channel A) and/or J200 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (ADI uses TTE, Allen Avionics, and K&L band-pass filters.) In order for the input level to be near the ADC's full scale, the generator level should be set to 8dBm to 12dBm – this level depends on the input frequency and any losses in bandpass filters.

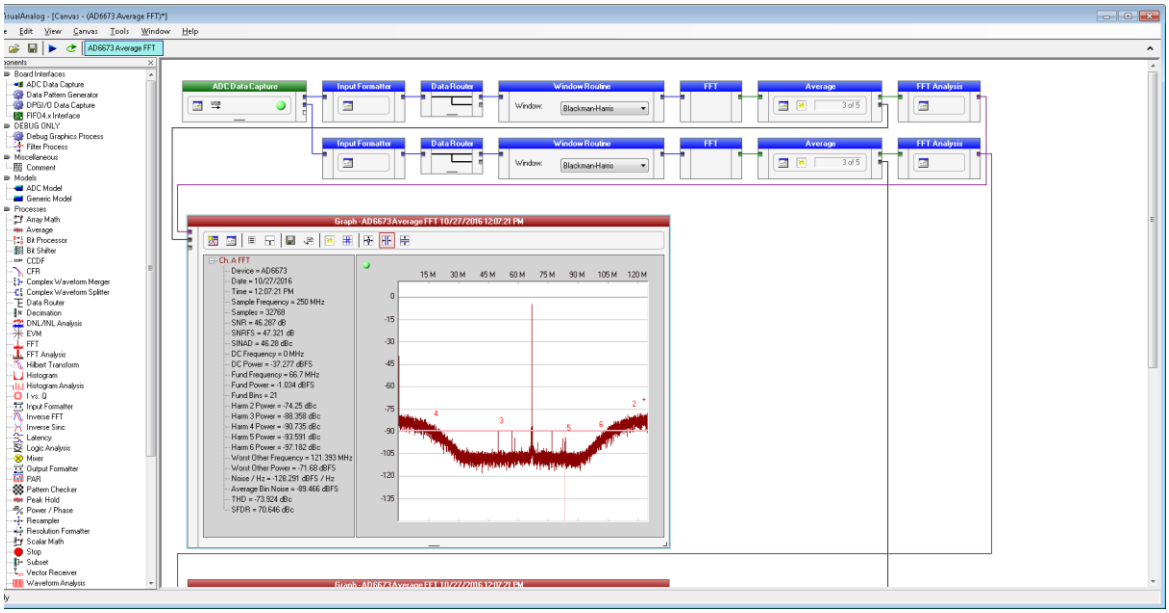
6. Open **Visual Analog** on the PC and select the *Average FFT* canvas in the AD6673 folder located in ADC/Dual/AD6673 directory. Note other templates could also be selected.



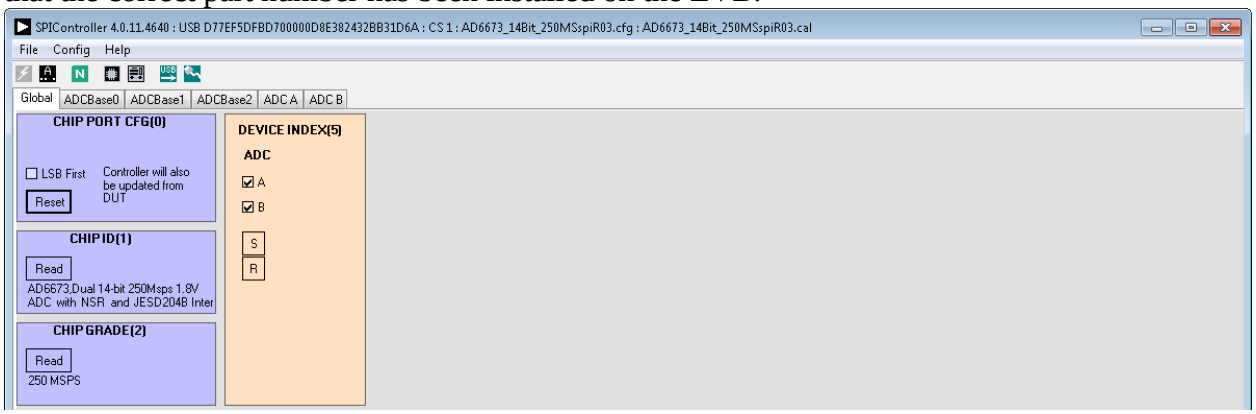
Click on **YES** to program the FPGA when he following message appears.



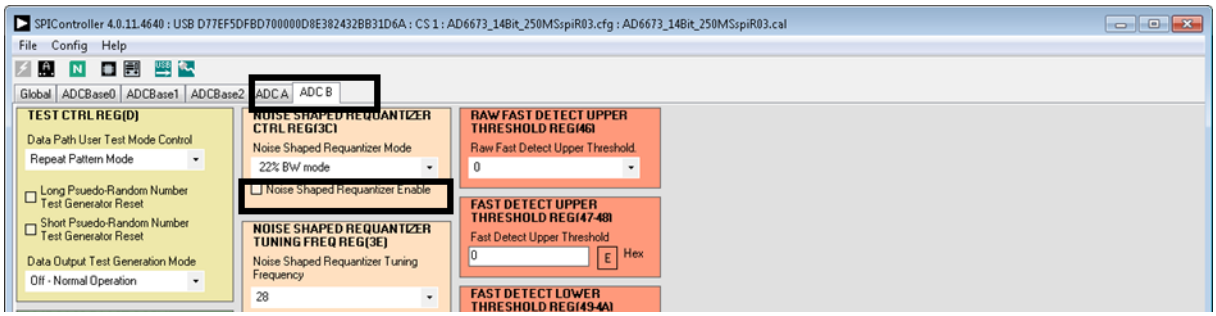
7. The following VA canvas below should appear below <u>after clicking</u> the Run button (▶) in VisualAnalog..



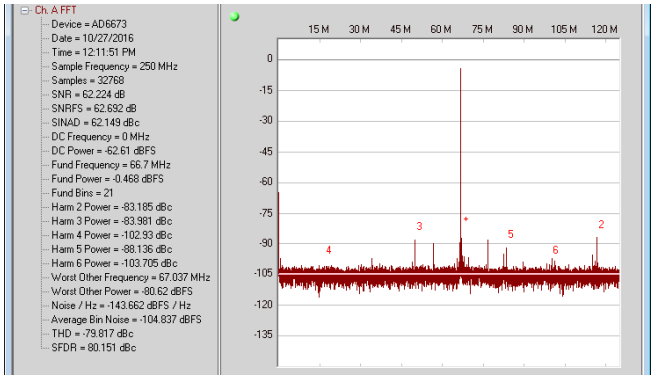
8. Open **SPI Controller** to re-configure any of the AD6673 registers. The following window should appear with the proper CHIP ID(1) and CHIP GRADE (2) being displayed to validate that the correct part number has been installed on the EVB.



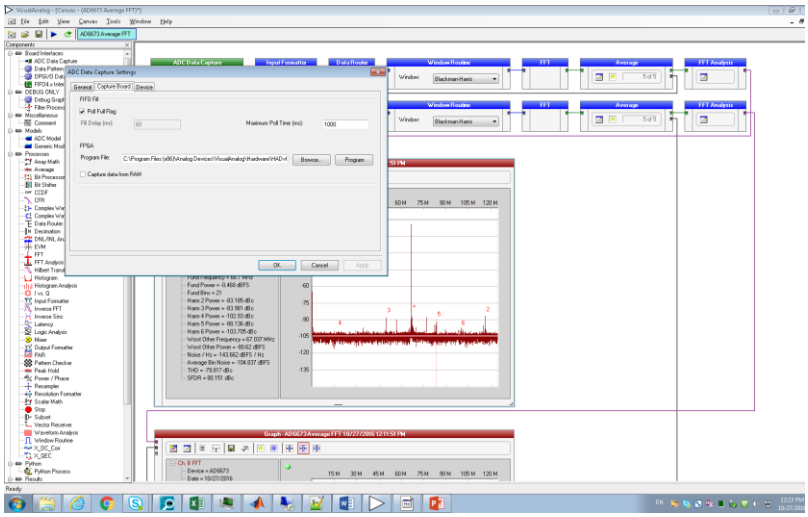
9. For additional validation of SPI control, one can disable the Noise Shaped Requantizer feature of ADC A and/or ADC B.



The FFT of the selected ADC(s) will appear like below with a flat noise spectral density..



10. (Optional): To re-program the FPGA, select the ADC Data Capture Settings window and click on the 'Capture Board' tab (see the box in the figure below). In the FPGA box select the program "AD9250_evalez.mcs" to configure the FPGA. After selecting the file, click the "Program" button to download the file to the FPGA. The 'CONFIG_DONE' LED should illuminate on the HSC-ADC-EVALEZ board indicating that the FPGA is now programmed.



Troubleshooting

► *The FFT plot appears abnormal...*

- ✓ If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce input level if necessary.
- ✓ In VisualAnalog, Click on the Settings button in the "Input Formatter" block. Check that "Number Format" is set to the correct encoding (2's compliment by default).

► *The FFT plot appears normal, but performance is poor.*

- ✓ Make sure you are using an appropriate filter on the analog input.
- ✓ Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- ✓ If you are using non-coherent sampling, change the analog input frequency slightly.
- ✓ Make sure the SPI config file matches the product being evaluated.

► *The FFT window remains blank after the Run button is clicked.*

- ✓ Make sure the evaluation board is securely connected to the HSC-ADC-EVALEZ board
- ✓ Disconnect power from both the ADC evaluation board and the HSC-ADC-EVALEZ board, disconnect the USB cable from the HSC-ADC-EVALEZ board and begin again at Step 1.
- ✓ Make sure the FPGA has been programmed by verifying that the 'CONFIG_DONE' LED is illuminated on the HSC-ADC-EVALEZ board.
- ✓ Make sure the correct FPGA program was installed.

► *VisualAnalog indicates that the "FIFO capture timed out."*

- ✓ Make sure all power and USB connections are secure.
- ✓ Double check that the encode clock source is present at the *CLKIN* connector.

Revision: 0 Oct 19, 2016