

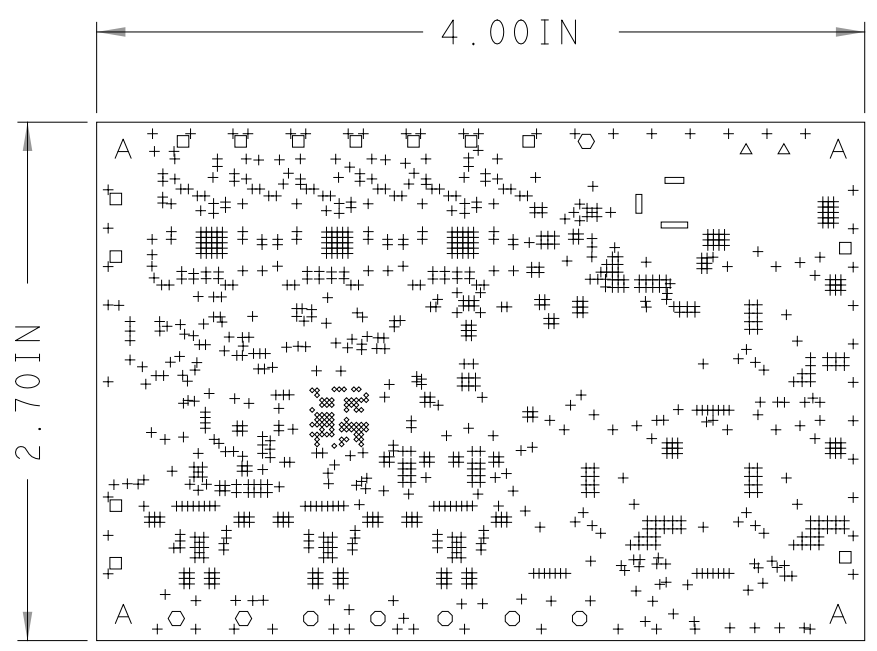
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	02AUG23	Z. ARCEO
B	ECR-116325	15AUG23	Z. ARCEO
C	ECR-117464	08NOV23	Z. ARCEO

HOLE TOLERANCE
 UNLESS SPECIFIED
 PLATED: +/- .003
 NON PLATED: +/- .002


FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
•	6.0	PLATED	71	DIA MAX
+	10.0	PLATED	1025	DIA MAX
□	40.0	PLATED	13	
△	50.0	PLATED	2	
○	63.0	PLATED	3	
○	100.0	PLATED	5	
A	125.0	NON-PLATED	4	
TOTAL HOLES: 1123				

TENTED VIA
 TENTED VIA

FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
▭	98.0x31.0	PLATED	1	
▭	98.0x31.0	PLATED	1	
▭	138.0x31.0	PLATED	1	
TOTAL HOLES: 3				



PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 --2 .XXX -.005 .XXXX -.0050	APPROVAL TEMPLATE ENGINEER BILLY PHILLIPS	DATE 07APR21	 GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887
	HARDWARE SERVICES BOB MACDONALD	DATE 07APR21	
MATERIAL	HARDWARE SYSTEMS DAVE WILLIAMS	DATE 07APR21	TITLE FABRICATION AD-PAARRAY3552R-SL
	TEST ENGINEER N/A	DATE N/A	
	COMPONENT ENGINEER ADGT LIBRARY	DATE 02AUG23	
FINISH	TEST PROCESS N/A	DATE N/A	SIZE FSCM NO DRAWING NUMBER REV C 24355 09-079905 C
	HARDWARE RELEASE C. PASIA	DATE 08NOV23	
	PCB DESIGNER C. PASIA	DATE 08NOV23	
DO NOT SCALE DWG	ENGINEER Z. ARCEO	DATE 08NOV23	SHEET 1 OF 2
	CHECKER N/A	DATE N/A	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	02AUG23	Z. ARCEO
B	ECR-116325	15AUG23	Z. ARCEO
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ASSEMBLY NOTES:

- BOARD ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00119 (LATEST REVISION).
- REPAIRS PER IPC-7711/21(LATEST REVISION) ARE ALLOWED.
- REPAIRS ARE NOT ALLOWED IN SOLDERMASK FREE AREAS ON EITHER SIDE OF THE BOARD.
- RoHS COMPLIANCE: ASSEMBLY VENDOR SHOULD ASSURE COMPLIANCE WITH LEAD-FREE AND RoHS PCB ASSEMBLY STANDARDS (EU RoHS DIRECTIVE 2002/95/EC).
- SOLDER SHORT PINS BELOW:

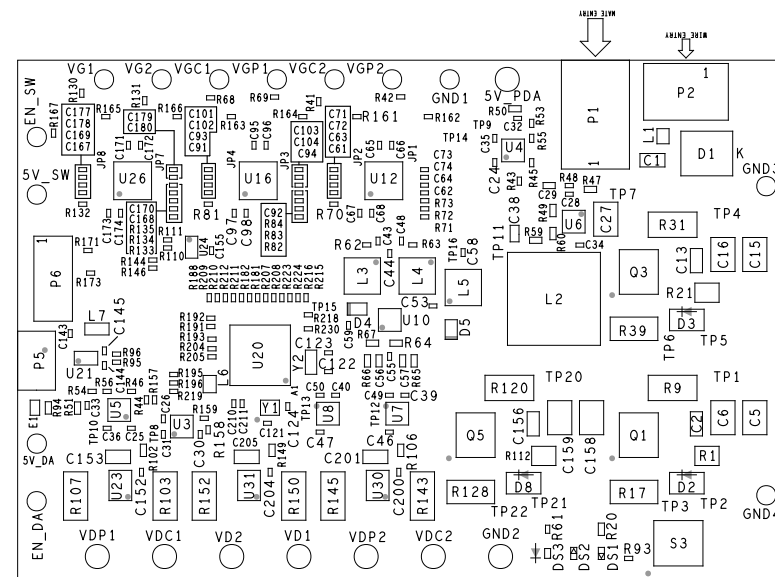
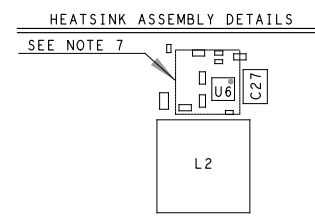
JP9 (PIN 1 & 2)
 JP10 (PIN 1 & 2)
 JP11 (PIN 2 & 3)
 JP12 (PIN 2 & 3)

P3
 P4
 P7
 P8
 P9
 P10
 P11


- THESE FOLLOWING PARTS ARE DNI:

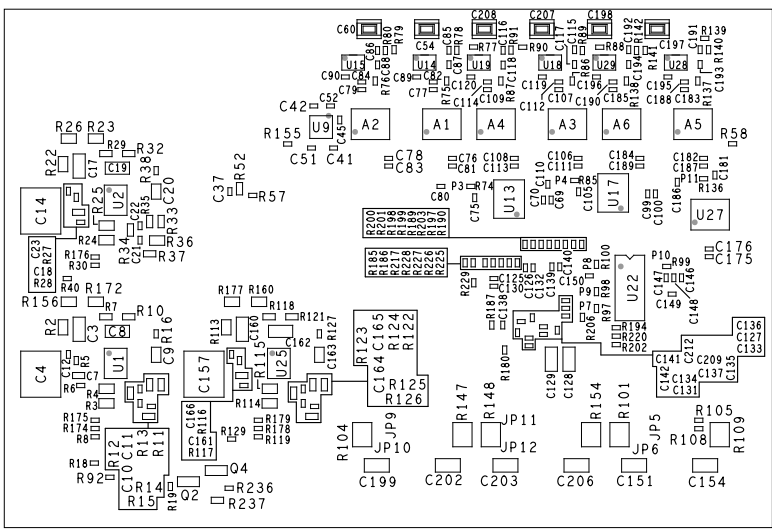
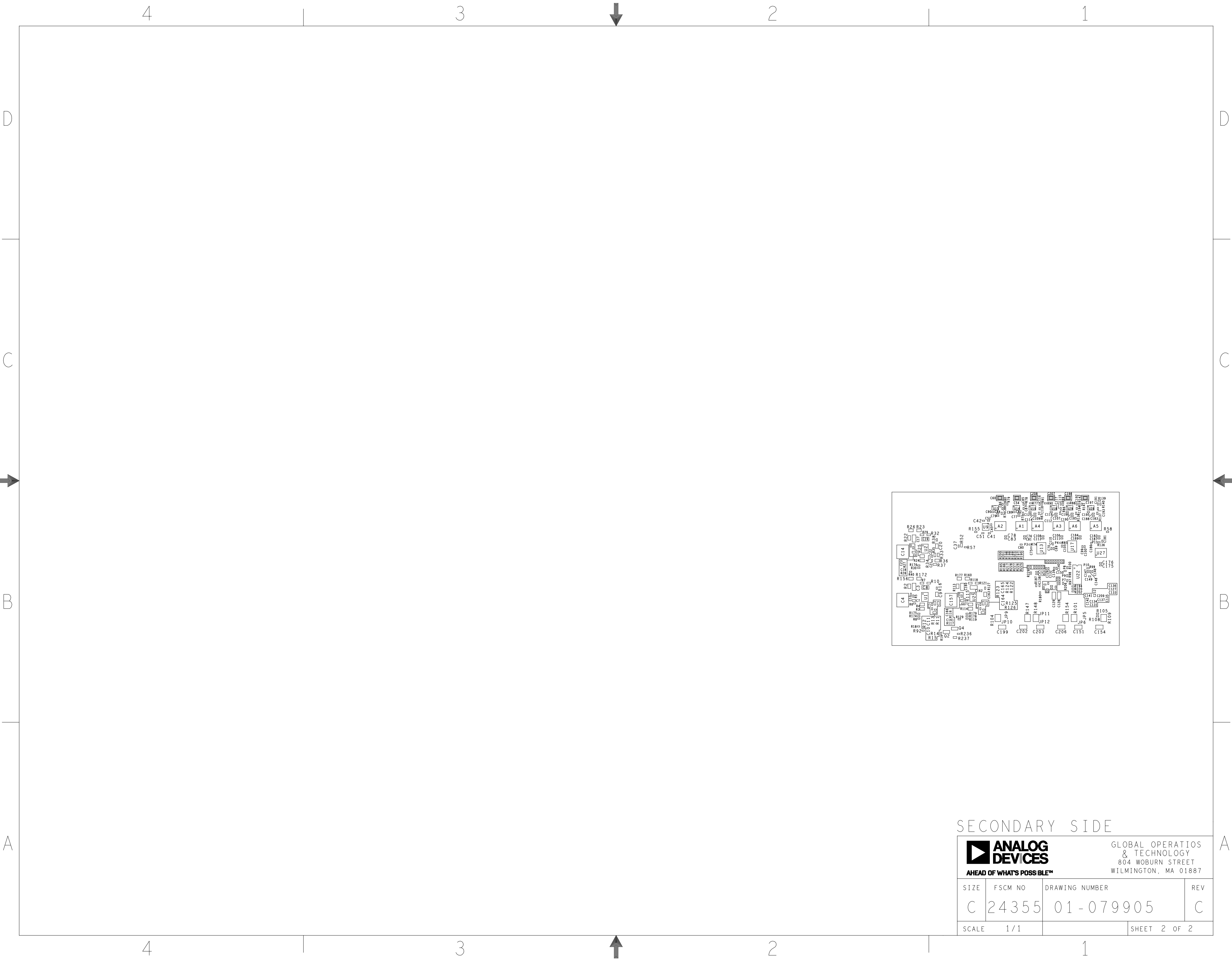
C10, C21, C164
 C11, C22, C165
 C85, C86, C115, C116, C191, C192
 C122, C123
 C54, C60, C197, C198, C207, C208
 R5, R14, R16, R27, R38, R116, R125, R127, R144
 R6, R28, R117
 R174, R175, R176, R178, R179
 R36

- INSTALL (N063458) V2016B HEATSINK ON TOP OF U6 (MAX17643ATC+) USING 468MP ADHESIVE TRANSFER TAPE
 1 QTY OF (MFG PN = 1-5-468MP)TAPE CAN MAKE UP TO 1075 PCS OF 0.335"X0.335"(8.5mmx8.5mm) TAPE FOR V2016B HEATSINK




PRIMARY SIDE

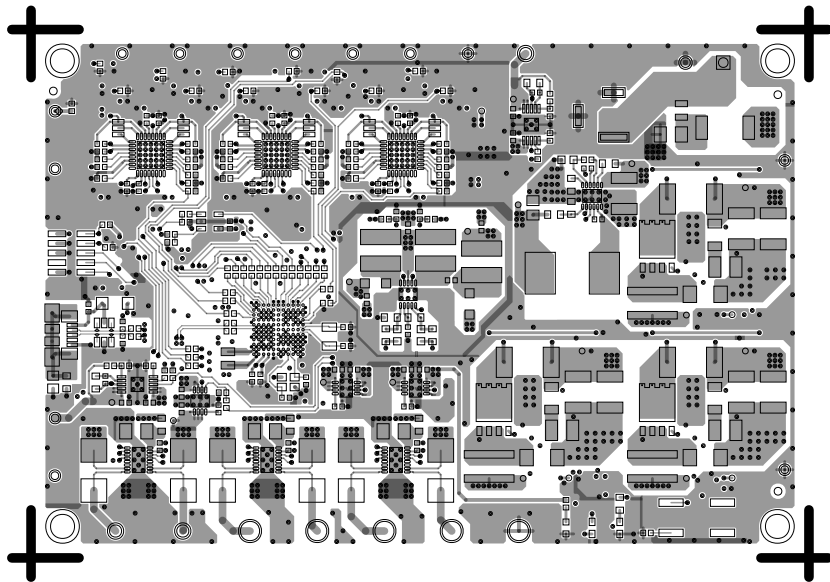
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 --2 .XXX -.005 .XXXX -.0050	APPROVAL BILLY PHILLIPS	DATE 07APR21	 GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887			
	HARDWARE SERVICES BOB MACDONALD	DATE 07APR21				
MATERIAL	HARDWARE SYSTEMS DAVE WILLIAMS	DATE 07APR21	TITLE ASSEMBLY AD-PAARRAY3552R-SL			
	TEST ENGINEER N/A	DATE N/A				
	COMPONENT ENGINEER ADGT LIBRARY	DATE 02AUG23				
	TEST PROCESS N/A	DATE N/A				
FINISH	HARDWARE RELEASE C. PASIA	DATE 08NOV23	SIZE C	FSCM NO 24355	DRAWING NUMBER 01-079905	REV C
	PCB DESIGNER C. PASIA	DATE 08NOV23	SCALE 1/1		SHEET 1 OF 2	
	ENGINEER Z. ARCEO	DATE 08NOV23				
DO NOT SCALE DWG	CHECKER N/A	DATE N/A				



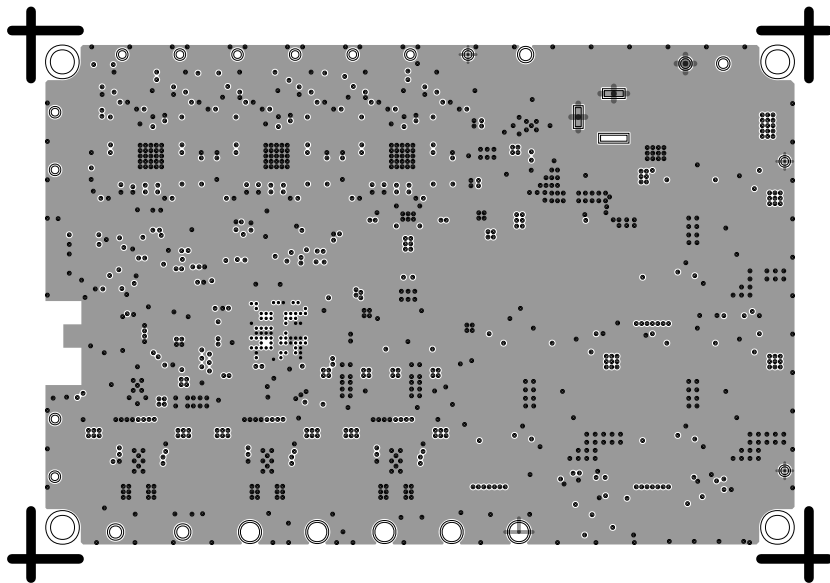
SECONDARY SIDE

		GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887	
SIZE	FSCM NO	DRAWING NUMBER	REV
C	24355	01-079905	C
SCALE	1/1	SHEET 2 OF 2	

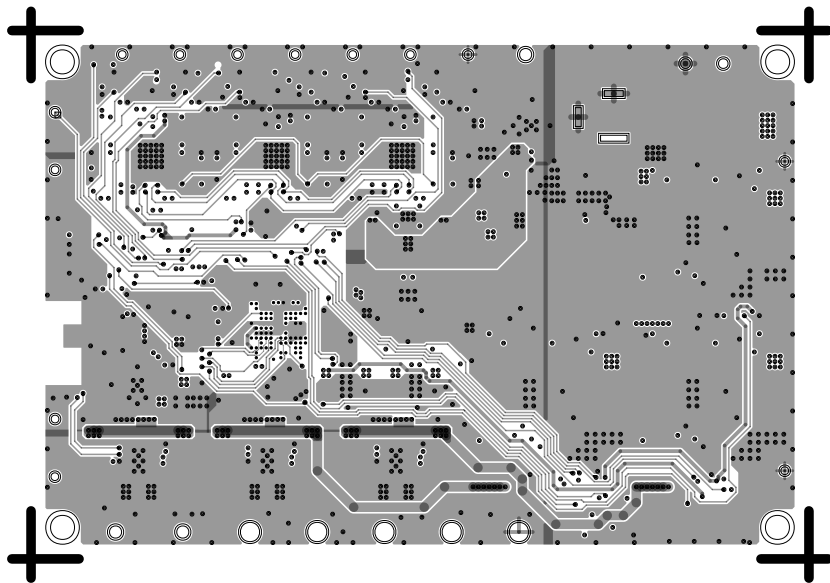
L1 PRIMARY
08-079905-01
REV C



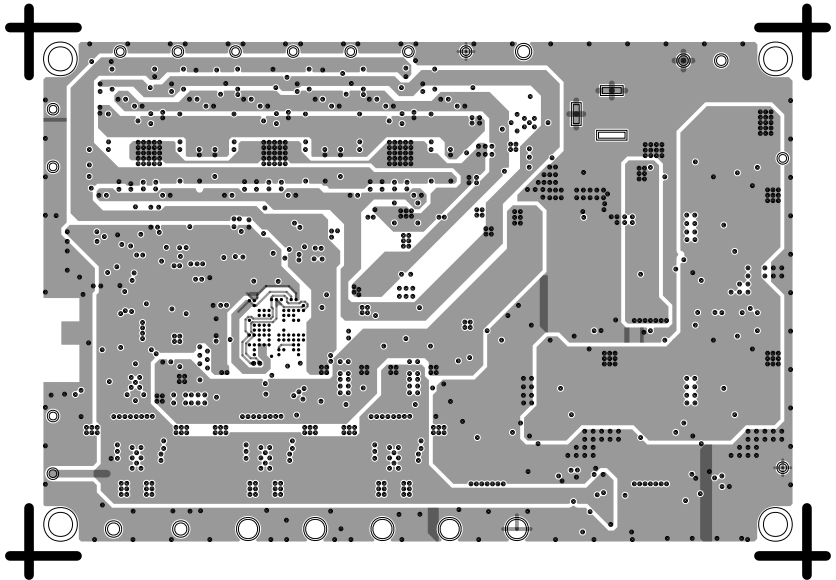
L2 GND
08-079905-07
REV C



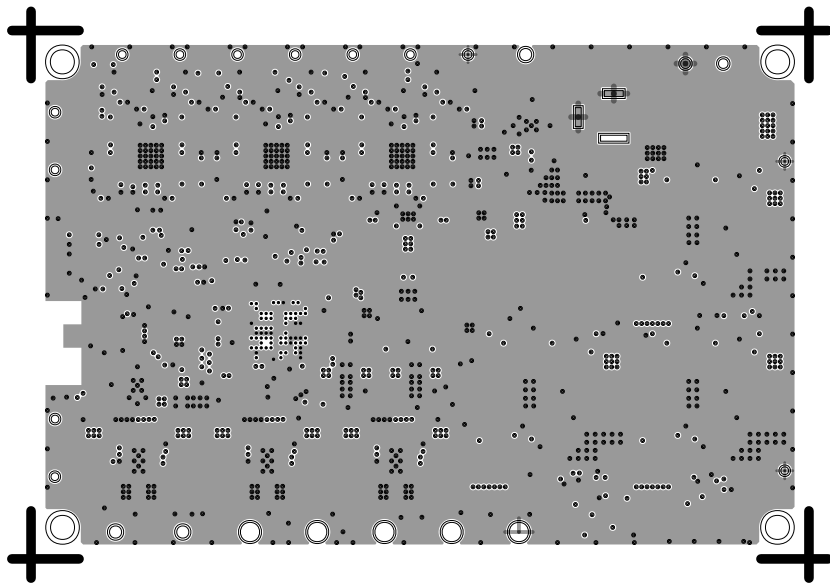
L3 SIG
08-079905-08
REV C



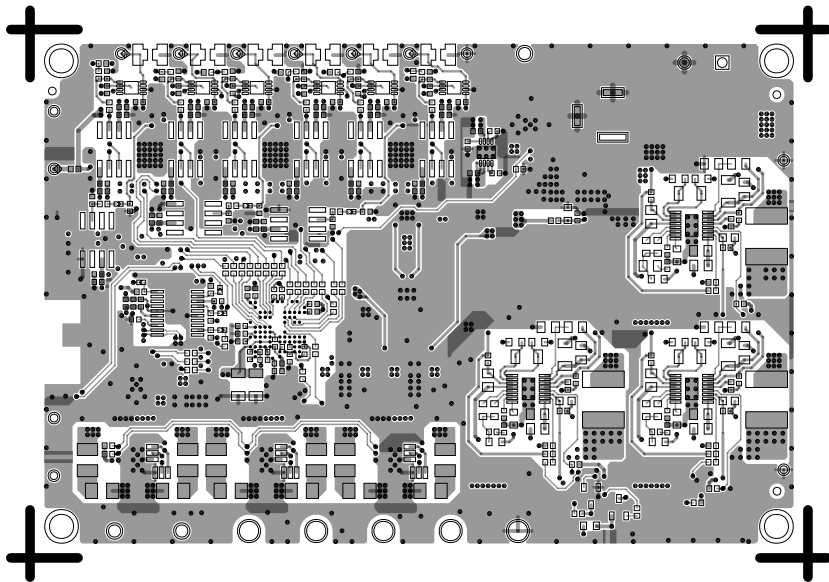
L4 PWR
08-079905-09
REV C



L5 GND
08-079905-10
REV C



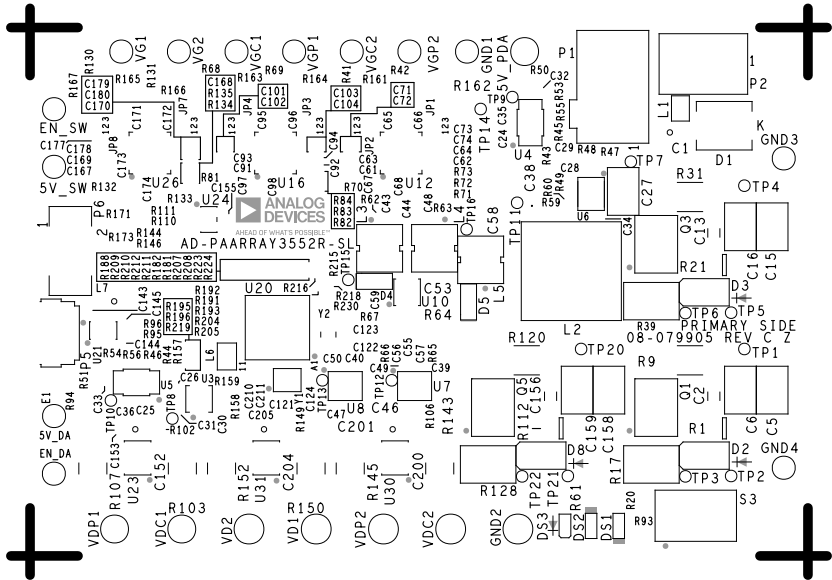
L6 SECONDARY
08-079905-02
REV C



SILKSCREEN PRIMARY

08-079905-03

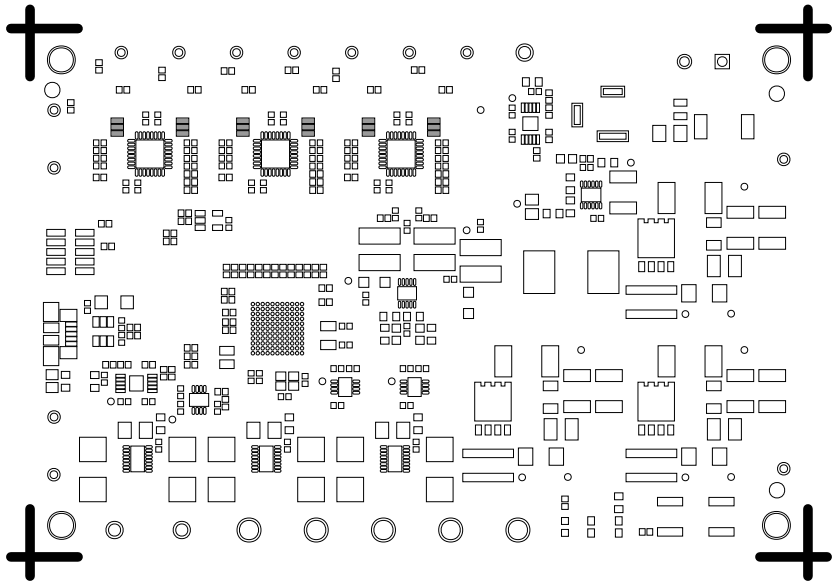
REV C



SOLDERMASK PRIMARY

08-079905-04

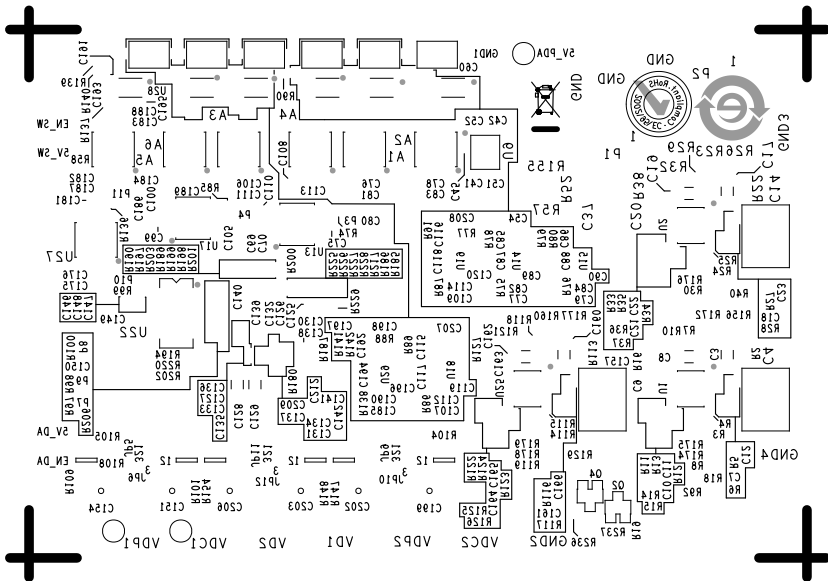
REV C



SILKSCREEN SECONDARY

08-079905-05

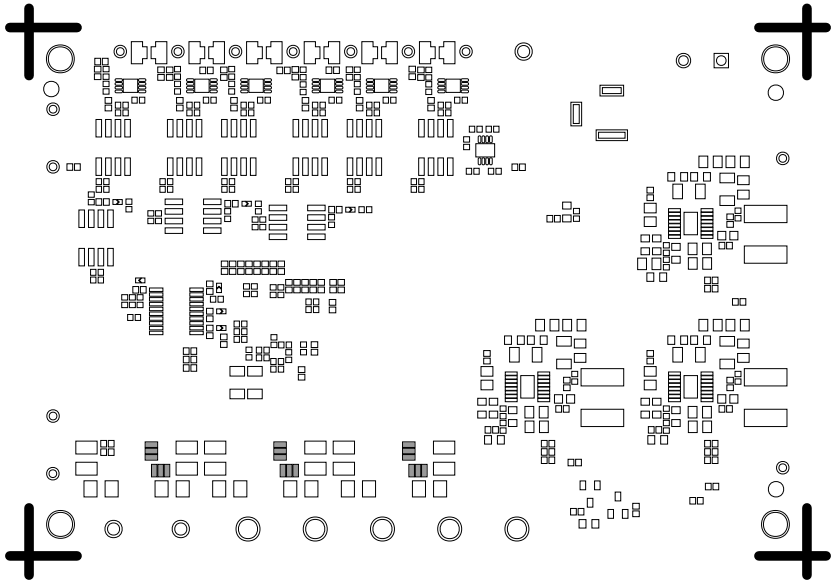
REV C



SOLDERMASK SECONDARY

08-079905-06

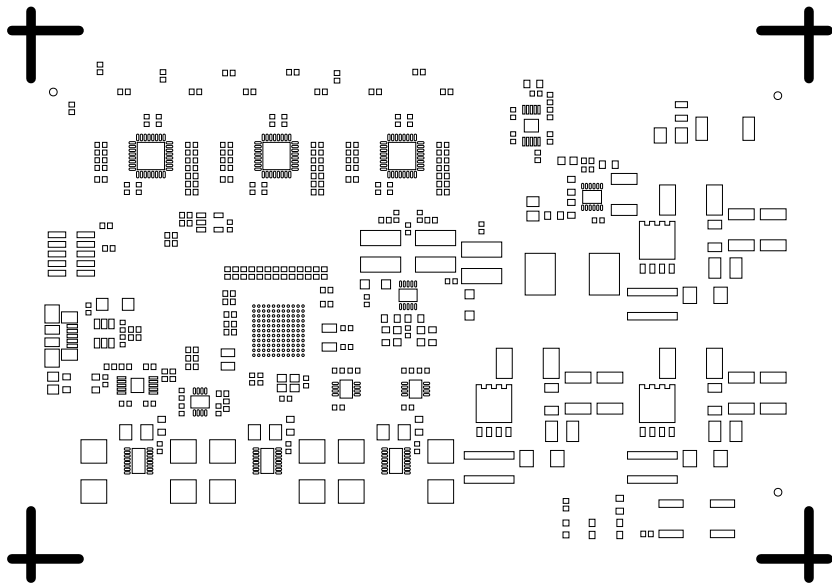
REV C



PASTEMASK PRIMARY

08-079905-11

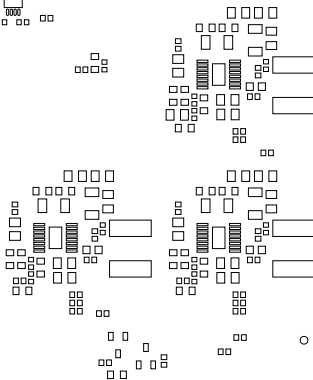
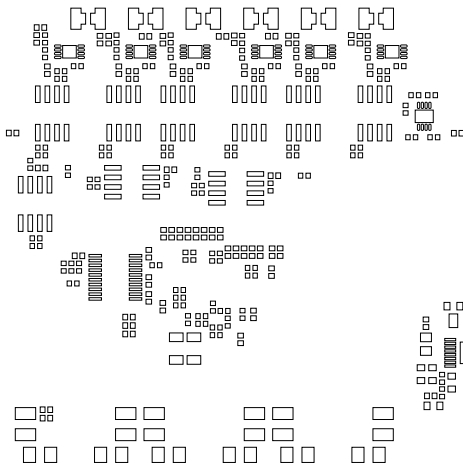
REV C



PASTEMASK SECONDARY

08-079905-12

REV C



NOTES: UNLESS OTHERWISE SPECIFIED

- DIMENSIONS ARE IN INCHES (EXCEPT WHERE NOTED). ALL DOCUMENTS & SPECIFICATIONS REFERRED TO BELOW SHOULD BE THE LATEST REVISIONS.

MATERIAL: HOMOGENOUS MATERIALS IN THIS BOARD SHALL BE COMPLAINT WITH THE EU DIRECTIVE 2002/95/EC

- BOARD MATERIAL:(USE CHECKED ITEMS)
 - ISOLA 370HR OR EQUIVALENT
 - ISOLA-FR408HR OR EQUIVALENT
 - ISOLA 15410
 - MEGTRON 6
 - NELCO-4000-13
 - ROGERS 4350B
 - ROGERS 3003
 - ARLON 85N
 - EM370D
 - OTHER _____
- ALL LAMINATES & BONDING MATERIALS SHOULD BE SELECTED FROM IPC-4101 OR IPC-4103.(TG>170 DEGC TD>300 DEGC) UL FLAMMABILITY RATING 94V-0. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796/UL796F.
- REFER TO IPC-6010 SERIES, CLASS 2 FOR FABRICATION. WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2.
- REFER TO LAMINATION DIAGRAM FOR OVERALL BOARD THICKNESS. TOLERANCE APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES. FINISHED THICKNESS MEASURED FROM TOP COPPER TO BOTTOM COPPER.
- BOW & TWIST NOT TO EXCEED 0.0075 INCHES (0.75%) PER LINEAR INCH AND SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.
- ACCEPTABILITY PER ADI SPECIFICATION TST00115.

TOOLING:

- IMPEDANCE REQUIREMENTS: IF NO STACKUP IS DEFINED, THE VENDOR IS ALLOWED TO ADJUST THE DIELECTRIC THICKNESS & TRACE WIDTHS TO MEET THE IMPEDANCE REQUIREMENT. IF SPECIFIED, THE VENDOR MUST MEET THE REQUIREMENTS LISTED IN THE IMPEDANCE TABLE. ANY ADJUSTMENT MADE TO THE DEFINED STACKUP, TRACE WIDTH & SPACING THAT IMPACT THE REQUIREMENTS MUST HAVE WRITTEN APPROVAL FROM ADI.
- FILLET OPTIONS TO ENHANCE RELIABILITY AT PAD JUNCTIONS WHERE SPACING PERMITS.
 - FILLETS ALLOWED
 - FILLETS NOT ALLOWED
- THIEVING:
 - VENDOR MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS MAINTAINING A MINIMUM 0.100 INCH CLEARANCE FROM ALL COPPER FEATURES.
 - VENDOR MAY NOT ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS.
- LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003 INCHES.

FINISH:

- DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN 0.005 INCHES DTP,UNLESS SPECIFIED. MINIMUM BARREL PLATING OF 0.001 INCHES. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO HINDER PROPER SOLDER WICKING. BARREL RELIEF ON SOLDERMASK ALLOWED IN UNFILLED VIA IN PAD HOLES.
- PLATING SPECIFICATION:
 - REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIRMENTS
 - THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE.
- SURFACE FINISH:
 - IMMERSION GOLD (ENIG) 1.58-3.94 MICRO INCHES OVER 118-236 MICRO INCHES MIN. OF ELECTROLESS NICKEL PER IPC-4552
 - OSP (ORGANIC SOLDERABILITY PRESERVATIVE)
 - IMMERSION SILVER
 - SOFT WIRE BONDABLE GOLD 30-50 MICRO INCHES OF SOFT WIRE
 - BONDABLE GOLD OVER 100-150 MICRO INCHES OF NICKEL
 - EDGE CONNECTOR FINGERS ARE TO BE PLATED WITH 100 MICRO-INCHES (.0001") OF LOW STRESS NICKEL UNDER 30 MICRO-INCHES (.0003") OF GOLD
 - OTHER:
- SOLDERMASK:
 - SOLDERMASK OVER BARE COPPER OR BARE GOLD (BOTH SIDES) TO MEET IPC-SM-840.
 - IF PRESENT,DO NOT MODIFY SOLDERMASK DEFINED PADS (MASK OPENINGS LESS THAN COPPER PAD) WITHOUT APPROVAL.
 - LPI
 - OTHER _____
 - COLOR
 - GREEN
 - OTHER BLUE
- APPLY SILKSCREEN TO BOTH SIDES USING A NON-CONDUCTIVE, EPOXY BASED INK PER ARTWORK.
 - WHITE
 - OTHER

NOTES: UNITS IN INCH
DP = DIFFERENTIAL PAIR

IMPEDANCE TABLE					
IMPEDANCE TOLERANCE: +/-10%					
LAYER	- OHM TRACE WIDTH	- OHM TRACE WIDTH	- OHM TRACE WIDTH/SPACE	90 OHM DP TRACE WIDTH/SPACE	REFERENCE LAYER
TOP	-	-	-	0.00590/0.00910	L2
BOTTOM	-	-	-	0.00590/0.00910	L5

NOTE: DO NOT EDIT THIS TABLE MANUALLY,USE IMPEDANCE TABLE GENERATOR FROM ADI Tools.

TESTING:

- FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE. THE PCB SHALL HAVE A VERIFICATION STAMP.
- A TIME DOMAIN REFLECTOMETER REPORT (TDR) FOR EACH IMPEDANCE CONTROLLED LAYER & A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE, ALL OTHER INSTANCES MUST BE REPORTED.

MISCELLANEOUS:


- IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO <1:1 TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE FILLED WITH NON-CONDUCTIVE EPOXY.
- FOR VIA FILL INFORMATION REFER TO DRILL CHART:
 - NON-CONDUCTIVE EPOXY FILL ALL 0.0050 INCHES AND 0.XXXX INCHES DRILLED VIAS
 - COPPER FILL ALL 0.XXXX INCHES DRILLED VIAS
- INTENTIONAL SHORTS:
 - IF AN INTENTIONAL SHORT REPORT IS SUPPLIED AND DOES NOT MATCH THE FAB DATA THEN ADI APPROVAL IS REQUIRED.
- PEMNUTS:
 - PEMNUTS TO BE INSTALLED BY FABRICATOR
 - PEMNUTS NOT TO BE INSTALLED BY FABRICATOR
 - NOT APPLICABLE
- MANUFACTURER TO ETCH/STAMP WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE UNLESS OTHERWISE SPECIFIED:
 - A. UL CODE-FLAMMABILITY RATING FOR THOSE APPROVED MATERIALS(IF APPLICABLE)
 - B. DATE CODE
 - C. LOT NUMBER
 - D. MANUFACTURER LOGO
- MINIMUM DESIGN LINE WIDTH IS .004 INCH.
- MINIMUM DESIGN LINE SPACING IS .004 INCH.
- BOARDS TO BE SHIPPED SINGULATED AFTER FABRICATION PROCESS SMOOTHEN EDGES AND FREE FROM BURRS AFTER DEPANELIZATION PROCESS

FAB NOTES REVISION: 2ND NOVEMBER 2022

LAMINATION DIAGRAM				
LAYER NUMBER	LAYER NAME	FINISHED CU WEIGHT (OZ)	DIELECTRIC THICKNESS (INCH)	MATERIALS
1	TOP	1		FINAL CU(THICKNESS AFTER PLATING)
			0.0039	ISOLA 370HR/EQUIVALENT
2	L2_GND	1		CU CLAD
			0.008	ISOLA 370HR/EQUIVALENT
3	L3_SIG	1		CU CLAD
			0.03	ISOLA 370HR/EQUIVALENT
4	L4_PWR	1		CU CLAD
			0.008	ISOLA 370HR/EQUIVALENT
5	L5_GND	1		CU CLAD
			0.0039	ISOLA 370HR/EQUIVALENT
6	BOTTOM	1		FINAL CU(THICKNESS AFTER PLATING)

THE FINISHED PCB THICKNESS TO BE: 0.062" +/-0.006"

PRIMARY SIDE

		GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887	
SIZE	FSCM NO	DRAWING NUMBER	REV
C	24355	09-079905	C
SCALE	1/1	SHEET 2 OF 2	