Zynq Bank	Zynq Pin #	PicoZed SDR 1X1 Net	JX1 Pin #	JX1 Pin #	PicoZed SDR 1X1 Net	Zynq Pin #	Zynq Bank
0	F9	JTAG_TCK	1	2	JTAG_TMS	J6	0
0	F6	JTAG_TDO	3	4	JTAG_TDI	G6	0
n/a	n/a	PWR_ENABLE(1)	5	6	CARRIER_RESET(2)	B10	501
0	F11	FPGA_VBATT	7	8	FPGA_DONE	R11	0
		open	9	10	open		
		open	11	12	open		
		open	13	14	open		
		GND	15	16	**GND**		
		open	17	18	open		
		open	19	20	open		
		GND	21	22	**GND**		
		open	23	24	open		
		open	25	26	open		
		GND	27	28	**GND**		
		open	29	30	open		
		open	31	32	open		
		GND	33	34	**GND**		
		open	35	36	open		
		open	37	38	open		
		GND	39	40	**GND**		
		open	41	42	open		
		open	43	44	open		
		GND	45	46	**GND**		
		open	47	48	open		
		open	49	50	open		
		GND	51	52	**GND**		
		open	53	54	open		
		open	55	56	open		
n/a		**JX_VIN**	57	58	**JX_VIN**		n/a
n/a		**JX_VIN**	59	60	**JX_VIN**		n/a
		open	61	62	open		
		open	63	64	open		
		GND	65	66	**GND**		
		open	67	68	open		
		open	69	70	open		
		GND	71	72	**GND**		
		open	73	74	open		
		open	75	76	open		
		GND	77	78	open		
		open	79	80	open		
		open	81	82	open		
		open	83	84	open		
		GND	85	86	**GND**		
		open	87	88	open		
		open	89	90	open		
		open	91	92	open		
		open	93	94	open		
		GND	95	96	**GND**		
		open	97	98	DX_0_P	M9	0
		open	99	100	DX_0_N	M10	0

Zynq Bank	Zynq Pin #	PicoZed SDR 1X1 Net	JX2 Pin #	JX2 Pin #	PicoZed SDR 1X1 Net	Zynq Pin #	Zynq Bank
		open	1	2	open		
		open	3	4	open		
		open	5	6	open		
		open	7	8	open		
0		INIT_B_0_JX2_09	9	10	PG_1P8V	n/a	n/a
n/a	n/a	PG_MODULE(1)	11	12	**JX_VIN**		n/a
		open	13	14	open		
		GND	15	16	**GND**		
13	W6	SCL	17	18	IO_L06_13_JX2_P	V5	13
13	V6	SDA	19	20	open		
		GND	21	22	**GND**		
		open	23	24	open		
		open	25	26	open		
		GND	27	28	**GND**		
		open	29	30	open		
		open	31	32	open		
		GND	33	34	**GND**		
13	U7	IO_L11_SRCC_13_JX2_P	35	36	IO_L12_MRCC_13_JX2_P	T9	13
13	V7	IO_L11_SRCC_13_JX2_N	37	38	IO_L12_MRCC_13_JX2_N	U10	13
		GND	39	40	**GND**		
13	Y7	IO_L13_MRCC_13_JX2_P	41	42	IO_L14_SRCC_13_JX2_P	Y9	13
13	Y6	IO_L13_MRCC_13_JX2_N	43	44	IO_L14_SRCC_13_JX2_N	Y8	13
		GND	45	46	**GND**		
13	V8	IO_L15_13_JX2_P	47	48	IO_L16_13_JX2_P	W10	13
13	W8	IO_L15_13_JX2_N	49	50	IO_L16_13_JX2_N	W9	13
		GND	51	52	**GND**		
13	U9	IO_L17_13_JX2_P	53	54	IO_L18_13_JX2_P	W11	13
13	U8	IO_L17_13_JX2_N	55	56	IO_L18_13_JX2_N	Y11	13
n/a		**JX_VIN**	57	58	**JX_VIN**		n/a
n/a		**JX_VIN**	59	60	**JX_VIN**		n/a
13	T5	IO_L19_13_JX2_P	61	62	IO_L20_13_JX2_P	Y12	13
13	U5	IO_L19_13_JX2_N	63	64	IO_L20_13_JX2_N	Y13	13
		GND	65	66	**GND**		
13	V11	IO_L21_13_JX2_P	67	68	open		
13	V10	IO_L21_13_JX2_N	69	70	open		
		GND	71	72	**GND**		
		open	73	74	open		
		open	75	76	open		
		GND	77	78	**JX_VCCO_34**		n/a
n/a		**JX_VCCO_34**	79	80	**JX_VCCO_34**		n/a
		open	81	82	open		
		open	83	84	open		
		GND	85	86	**GND**		
		open	87	88	open		
		open	89	90	open		
		GND	91	92	**GND**		
		open	93	94	open		
		open	95	96	open		
		open	97	98	**JX_VCCO_13**		n/a
		open	99	100	open		

Zynq Bank	Zynq Pin #	PicoZed SDR 1X1 Net	JX3 Pin #	JX3 Pin #	PicoZed SDR 1X1 Net	Zynq Pin #	Zynq Bank
0	L10	V_0_P	1	2	open		
0	K9	V_0_N	3	4	open		
		open	5	6	**GND**		
		open	7	8	open		
		open	9	10	open		
		open	11	12	**GND**		
		open	13	14	open		
		open	15	16	open		
		GND	17	18	**GND**		
		open	19	20	open		
		open	21	22	open		
		GND	23	24	**GND**		
		open	25	26	open		
		open	27	28	open		
		GND	29	30	open		
		open	31	32	open		
		open	33	34	SDIO_CMDB1	n/a	n/a
		GND	35	36	SDIO_DAT1B1	n/a	n/a
n/a	n/a	SDIO_DAT0B1	37	38	SDIO_DAT3B1	n/a	n/a
n/a	n/a	SDIO_DAT2B1	39	40	**GND**		
n/a	n/a	JX3_SD1_CDN	41	42	open		
n/a	n/a	SDIO_CLKB1	43	44	open		
n/a		**JX_VCCO_13**	45	46	**JX_VCCO_13**		n/a
n/a	n/a	ETH_PHY_LED0	47	48	ETH_PHY_LED1	n/a	n/a
		GND	49	50	**GND**		
n/a	n/a	ETH_MD1_P	51	52	ETH_MD2_P	n/a	n/a
n/a	n/a	ETH_MD1_N	53	54	ETH_MD2_N	n/a	n/a
		GND	55	56	**GND**		
n/a	n/a	ETH_MD3_P	57	58	ETH_MD4_P	n/a	n/a
n/a	n/a	ETH_MD3_N	59	60	ETH_MD4_N	n/a	n/a
		GND	61	62	**GND**		
n/a	n/a	USB_ID	63	64	open		
		GND	65	66	open		
n/a	n/a	USB_OTG_P	67	68	USB_VBUS_OTG	n/a	n/a
n/a	n/a	USB_OTG_N	69	70	USB_OTG_CPEN	n/a	n/a
		GND	71	72	**GND**		
		open	73	74	open		
		open	75	76	open		
		GND	77	78	**GND**		
		open	79	80	open		
		open	81	82	open		
		GND	83	84	**GND**		
		open	85	86	open		
		open	87	88	open		
		GND	89	90	**GND**		
		open	91	92	open		
		open	93	94	open		
		GND	95	96	**GND**		
		open	97	98	open		
		open	99	100	open		

Zynq Bank	Zynq Pin #	PicoZed SDR 1X1 Net	JX4 Pin #	JX4 Pin #	PicoZed SDR 1X1 Net	Zynq Pin #	Zynq Bank
n/a	n/a	GPO_0	1	2	GPO_1	n/a	n/a
n/a	n/a	GPO_2	3	4	GPO_3	n/a	n/a
		GND	5	6	**GND**		
n/a	n/a	AUXADC	7	8	AUXDAC1	n/a	n/a
n/a	n/a	VDDA_GPO_PWR	9	10	AUXDAC2	n/a	n/a
		GND	11	12	**GND**		
		open	13	14	open		
		open	15	16	open		
		GND	17	18	**GND**		
34	T11	IO_L01_34_JX4_P	19	20	IO_L02_34_JX4_P	T12	34
34	T10	IO_L01_34_JX4_N	21	22	IO_L02_34_JX4_N	U12	34
		GND	23	24	**GND**		
34	U13	IO_L03_34_JX4_P	25	26	IO_L04_34_JX4_P	V12	34
34	V13	IO_L03_34_JX4_N	27	28	IO_L04_34_JX4_N	W13	34
		GND	29	30	**GND**		
34	T14	IO_L05_34_JX4_P	31	32	IO_L06_34_JX4_P	P14	34
34	T15	IO_L05_34_JX4_N	33	34	IO_L06_34_JX4_N	R14	34
34	Y16	IO_L07_34_JX4_P	35	36	IO_L08_34_JX4_P	W14	34
34	Y17	IO_L07_34_JX4_N	37	38	IO_L08_34_JX4_N	Y14	34
		GND	39	40	**GND**		
34	T16	IO_L09_34_JX4_P	41	42	IO_L10_34_JX4_P	V15	34
34	U17	IO_L09_34_JX4_N	43	44	IO_L10_34_JX4_N	W15	34
34	U14	IO_L11_SRCC_34_JX4_P	45	46	IO_L12_MRCC_34_JX4_P	U18	34
34	U15	IO_L11_SRCC_34_JX4_N	47	48	IO_L12_MRCC_34_JX4_N	U19	34
		GND	49	50	**GND**		
34	N18	IO_L13_MRCC_34_JX4_P	51	52	IO_L14_SRCC_34_JX4_P	N20	34
34	P19	IO_L13_MRCC_34_JX4_N	53	54	IO_L14_SRCC_34_JX4_N	P20	34
		GND	55	56	**GND**		
34	T20	IO_L15_34_JX4_P	57	58	IO_L16_34_JX4_P	V20	34
34	U20	IO_L15_34_JX4_N	59	60	IO_L16_34_JX4_N	W20	34
		GND	61	62	**GND**		
n/a		AD9364_CLK	63	64	IO_25_34_JX4	T19	34
		GND	65	66	**GND**		
34	Y18	IO_L17_34_JX4_P	67	68	IO_L18_34_JX4_P	V16	34
34	Y19	IO_L17_34_JX4_N	69	70	IO_L18_34_JX4_N	W16	34
		GND	71	72	**GND**		
34	R16	IO_L19_34_JX4_P	73	74	IO_L20_34_JX4_P	T17	34
34	R17	IO_L19_34_JX4_N	75	76	IO_L20_34_JX4_N	R18	34
34	V17	IO_L21_34_JX4_P	77	78	IO_L22_34_JX4_P	W18	34
34	V18	IO_L21_34_JX4_N	79	80	IO_L22_34_JX4_N	W19	34
		open	81	82	open		
		GND	83	84	**GND**		
500	C8	PS_MIO15_500_JX4	85	86	PS_MIO12_500_JX4	D9	500
500	E9	PS_MIO10_500_JX4	87	88	PS_MIO11_500_JX4	C6	500
		GND	89	90	**GND**		
500	E8	PS_MIO13_500_JX4	91	92	PS_MIO46_501_JX4	D16	501
500	C5	PS_MIO14_500_JX4	93	94	PS_MIO47_501_JX4	B14	501
		GND	95	96	**GND**		
500	E6	PS_MIO00_500_JX4	97	98	PS_MIO49_501_JX4	C12	501
501	B12	PS_MIO48_501_JX4	99	100	PS_MIO51_501_JX4	B9	501