Zynq Bank	Zynq Pin #	PicoZed SDR 2X2 Net	JX1 Pin #	JX1 Pin #	PicoZed SDR 2X2 Net	Zynq Pin #	Zynq Bank
0	W12	JTAG_TCK	1	2	JTAG_TMS	W11	0
0	W10	JTAG_TDO	3	4	JTAG_TDI	V11	0
n/a	n/a	PWR_ENABLE	5	6	CARRIER_RESET	A22	501
0	V15	FPGA_VBATT	7	8	FPGA_DONE	W9	0
33	L9	IO_00_33_JX1	9	10	IO_25_33_JX1	N8	33
33	M2	IO_L16_33_JX1_P	11	12	IO_L17_33_JX1_P	N4	33
33	L2	IO_L16_33_JX1_N	13	14	IO_L17_33_JX1_N	M4	33
		GND	15	16	**GND**		
33	N1	IO_L18_33_JX1_P	17	18	IO_L19_33_JX1_P	M7	33
33	M1	IO_L18_33_JX1_N	19	20	IO_L19_33_JX1_N	L7	33
		GND	21	22	**GND**		
33	K5	IO_L20_33_JX1_P	23	24	IO_L21_33_JX1_P	M8	33
33	J5	IO_L20_33_JX1_N	25	26	IO_L21_33_JX1_N	L8	33
		GND	27	28	**GND**		
33	K6	IO_L22_33_JX1_P	29	30	IO_L23_33_JX1_P	N7	33
33	J6	IO_L22_33_JX1_N	31	32	IO_L23_33_JX1_N	N6	33
		GND	33	34	**GND**		
33	G4	IO_L01_33_JX1_P	35	36	IO_L24_33_JX1_P	K8	33
33	F4	IO_L01_33_JX1_N	37	38	IO_L24_33_JX1_N	K7	33
		GND	39	40	**GND**		
33	D4	IO_L02_33_JX1_P	41	42	IO_L03_33_JX1_P	G2	33
33	D3	IO_L02_33_JX1_N	43	44	IO_L03_33_JX1_N	F2	33
		GND	45	46	**GND**		
33	D1	IO_L04_33_JX1_P	47	48	IO_L14_SRCC_33_JX1_P	L5	33
33	C1	IO_L04_33_JX1_N	49	50	IO_L14_SRCC_33_JX1_N	L4	33
		GND	51	52	**GND**		
33	N3	IO_L15_33_JX1_P	53	54	IO_L05_33_JX1_P	E2	33
33	N2	IO_L15_33_JX1_N	55	56	IO_L05_33_JX1_N	E1	33
n/a		**JX_VIN**	57	58	**JX_VIN**		n/a
n/a		**JX_VIN**	59	60	**JX_VIN**		n/a
33	F3	IO_L06_33_JX1_P	61	62	IO_L07_33_JX1_P	J1	33
33	E3	IO_L06_33_JX1_N	63	64	IO_L07_33_JX1_N	H1	33
		GND	65	66	**GND**		
33	H4	IO_L08_33_JX1_P	67	68	IO_L09_33_JX1_P	K2	33
33	H3	IO_L08_33_JX1_N	69	70	IO_L09_33_JX1_N	K1	33
		GND	71	72	**GND**		
33	H2	IO_L10_33_JX1_P	73	74	IO_L11_SRCC_33_JX1_P	L3	33
33	G1	IO_L10_33_JX1_N	75	76	IO_L11_SRCC_33_JX1_N	K3	33
		GND	77	78	**JX_VCCO_12**		n/a
n/a		**JX_VCCO_12**	79	80	**JX_VCCO_12**		n/a
33	J4	IO_L12_MRCC_33_JX1_P	81	82	IO_L13_MRCC_33_JX1_P	M6	33
33	J3	IO_L12_MRCC_33_JX1_N	83	84	IO_L13_MRCC_33_JX1_N	M5	33
		GND	85	86	**GND**		
111	W6	MGTREFCLK0_111_JX1_P	87	88	MGTXRX0_111_JX1_P	AD8	111
111	W5	MGTREFCLK0_111_JX1_N	89	90	MGTXRX0_111_JX1_N	AD7	111
111	AE6	MGTXRX1_111_JX1_P	91	92	MGTXRX2_111_JX1_P	AC6	111
111	AE5	MGTXRX1_111_JX1_N	93	94	MGTXRX2_111_JX1_N	AC5	111
		GND	95	96	**GND**		
111	AD4	MGTXRX3_111_JX1_P	97	98	DX_0_P	R14	0
111	AD3	MGTXRX3_111_JX1_N	99	100	DX_0_N	R13	0

Zynq Bank	Zynq Pin #	PicoZed SDR 2X2 Net	JX2 Pin #	JX2 Pin #	PicoZed SDR 2X2 Net	Zynq Pin #	Zynq Bank
13	AA25	IO_L01_13_JX2_P	1	2	IO_L02_13_JX2_P	AB26	13
13	AB25	IO_L01_13_JX2_N	3	4	IO_L02_13_JX2_N	AC26	13
13	AE25	IO_L03_13_JX2_P	5	6	IO_L04_13_JX2_P	AD25	13
13	AE26	IO_L03_13_JX2_N	7	8	IO_L04_13_JX2_N	AD26	13
0		INIT_B_0_JX2_09	9	10	PG_1P8V	n/a	n/a
n/a	n/a	PG_MODULE	11	12	**JX_VIN**		n/a
13	V19	IO_00_13_JX2	13	14	IO_25_13_JX2	V18	13
		GND	15	16	**GND**		
13	AF24	SCL	17	18	IO_L06_13_JX2_P	AA24	13
13	AF25	SDA	19	20	IO_L06_13_JX2_N	AB24	13
		GND	21	22	**GND**		
13	AE22	IO_L07_13_JX2_P	23	24	IO_L08_13_JX2_P	AE23	13
13	AF22	IO_L07_13_JX2_N	25	26	IO_L08_13_JX2_N	AF23	13
		GND	27	28	**GND**		
13	AB21	IO_L09_13_JX2_P	29	30	IO_L10_13_JX2_P	AA22	13
13	AB22	IO_L09_13_JX2_N	31	32	IO_L10_13_JX2_N	AA23	13
		GND	33	34	**GND**		
13	AD23	IO_L11_SRCC_13_JX2_P	35	36	IO_L12_MRCC_13_JX2_P	AC23	13
13	AD24	IO_L11_SRCC_13_JX2_N	37	38	IO_L12_MRCC_13_JX2_N	AC24	13
		GND	39	40	**GND**		
13	AD20	IO_L13_MRCC_13_JX2_P	41	42	IO_L14_SRCC_13_JX2_P	AC21	13
13	AD21	IO_L13_MRCC_13_JX2_N	43	44	IO_L14_SRCC_13_JX2_N	AC22	13
		GND	45	46	**GND**		
13	AF19	IO_L15_13_JX2_P	47	48	IO_L16_13_JX2_P	AE20	13
13	AF20	IO_L15_13_JX2_N	49	50	IO_L16_13_JX2_N	AE21	13
		GND	51	52	**GND**		
13	AD18	IO_L17_13_JX2_P	53	54	IO_L18_13_JX2_P	AE8	13
13	AD19	IO_L17_13_JX2_N	55	56	IO_L18_13_JX2_N	AF18	13
n/a		**JX_VIN**	57	58	**JX_VIN**		n/a
n/a		**JX_VIN**	59	60	**JX_VIN**		n/a
13	W20	IO_L19_13_JX2_P	61	62	IO_L20_13_JX2_P	AA20	13
13	Y20	IO_L19_13_JX2_N	63	64	IO_L20_13_JX2_N	AB20	13
		GND	65	66	**GND**		
13	AC18	IO_L21_13_JX2_P	67	68	IO_L22_13_JX2_P	AA19	13
13	AC19	IO_L21_13_JX2_N	69	70	IO_L22_13_JX2_N	AB19	13
		GND	71	72	**GND**		
13	W18	IO_L23_13_JX2_P	73	74	IO_L24_13_JX2_P	Y18	13
13	W19	IO_L23_13_JX2_N	75	76	IO_L24_13_JX2_N	AA18	13
		GND	77	78	**JX_VCCO_33_34**		n/a
n/a		**JX_VCCO_33_34**	79	80	**JX_VCCO_33_34**		n/a
12	AE17	IO_L18_12_JX2_P	81	82	IO_L17_12_JX2_P	AE16	12
12	AF17	IO_L18_12_JX2_N	83	84	IO_L17_12_JX2_N	AE15	12
		GND	85	86	**GND**		
12	AB17	IO_L20_12_JX2_P	87	88	IO_L19_12_JX2_P	Y17	12
12	AB16	IO_L20_12_JX2_N	89	90	IO_L19_12_JX2_N	AA17	12
		GND	91	92	**GND**		
12	AC17	IO_L21_12_JX2_P	93	94	IO_L22_12_JX2_P	AA15	12
12	AC16	IO_L21_12_JX2_N	95	96	IO_L22_12_JX2_N	AA14	12
12	Y16	IO_L23_12_JX2_P	97	98	**JX_VCCO_13**		n/a
12	Y15	IO_L23_12_JX2_N	99	100	open		

Zynq Bank	Zynq Pin #	PicoZed SDR 2X2 Net	JX3 Pin #	JX3 Pin #	PicoZed SDR 2X2 Net	Zynq Pin #	Zynq Bank
0	N14	V_0_P	1	2	MGTREFCLK1_111_JX3_P	AA6	111
0	P13	V_0_N	3	4	MGTREFCLK1_111_JX3_N	AA5	111
n/a		**JX_MGTAVCC**	5	6	**GND**		
n/a		**JX_MGTAVCC**	7	8	MGTXTX0_111_JX3_P	AF8	111
n/a		**JX_MGTAVCC**	9	10	MGTXTX0_111_JX3_N	AF7	111
n/a		**JX_MGTAVCC**	11	12	**GND**		
111	AF4	MGTXTX1_111_JX3_P	13	14	MGTXTX2_111_JX3_P	AE2	111
111	AF3	MGTXTX1_111_JX3_N	15	16	MGTXTX2_111_JX3_N	AE1	111
		GND	17	18	**GND**		
111	AC2	MGTXTX3_111_JX3_P	19	20	IO_L01_12_JX3_P	Y12	12
111	AC1	MGTXTX3_111_JX3_N	21	22	IO_L01_12_JX3_N	Y11	12
		GND	23	24	**GND**		
12	AB12	IO_L02_12_JX3_P	25	26	IO_L03_12_JX3_P	Y10	12
12	AC11	IO_L02_12_JX3_N	27	28	IO_L03_12_JX3_N	AA10	12
		GND	29	30	**JX_MGTAVTT**		n/a
12	AB11	IO_L04_12_JX3_P	31	32	**JX_MGTAVTT**		n/a
12	AB10	IO_L04_12_JX3_N	33	34	SDIO_CMDB1	n/a	n/a
		GND	35	36	SDIO_DATB1	n/a	n/a
n/a	n/a	SDIO_DATB1	37	38	SDIO_DATB1	n/a	n/a
n/a	n/a	SDIO_DATB1	39	40	**GND**		
n/a	n/a	JX3_SD1_CDN	41	42	IO_L05_12_JX3_P	W13	12
n/a	n/a	SDIO_CLKB1	43	44	IO_L05_12_JX3_N	Y13	12
n/a		**JX_VCCO_13**	45	46	**JX_VCCO_13**		n/a
n/a	n/a	ETH_PHY_LED0	47	48	ETH_PHY_LED1	n/a	n/a
		GND	49	50	**GND**		
n/a	n/a	ETH_MD1_P	51	52	ETH_MD2_P	n/a	n/a
n/a	n/a	ETH_MD1_N	53	54	ETH_MD2_N	n/a	n/a
		GND	55	56	**GND**		
n/a	n/a	ETH_MD3_P	57	58	ETH_MD4_P	n/a	n/a
n/a	n/a	ETH_MD3_N	59	60	ETH_MD4_N	n/a	n/a
		GND	61	62	**GND**		
n/a	n/a	USB_ID	63	64	IO_L06_12_JX3_P	AA13	12
		GND	65	66	IO_L06_12_JX3_N	AA12	12
n/a	n/a	USB_OTG_P	67	68	USB_VBUS_OTG	n/a	n/a
n/a	n/a	USB_OTG_N	69	70	USB_OTG_CPEN	n/a	n/a
		GND	71	72	**GND**		
12	AE10	IO_L07_12_JX3_P	73	74	IO_L08_12_JX3_P	AE12	12
12	AD10	IO_L07_12_JX3_N	75	76	IO_L08_12_JX3_N	AF12	12
		GND	77	78	**GND**		
12	AE11	IO_L09_12_JX3_P	79	80	IO_L10_12_JX3_P	AE13	12
12	AF10	IO_L09_12_JX3_N	81	82	IO_L10_12_JX3_N	AF13	12
		GND	83	84	**GND**		
12	AC12	IO_L11_SRCC_12_JX3_P	85	86	IO_L12_MRCC_12_JX3_P	AC13	12
12	AD12	IO_L11_SRCC_12_JX3_N	87	88	IO_L12_MRCC_12_JX3_N	AD13	12
		GND	89	90	**GND**		
12	AC14	IO_L13_MRCC_12_JX3_P	91	92	IO_L14_SRCC_12_JX3_P	AB15	12
12	AD14	IO_L13_MRCC_12_JX3_N	93	94	IO_L14_SRCC_12_JX3_N	AB14	12
		GND	95	96	**GND**		
12	AD16	IO_L15_12_JX3_P	97	98	IO_L16_12_JX3_P	AF15	12
12	AD15	IO_L15_12_JX3_N	99	100	IO_L16_12_JX3_N	AF14	12

Zynq Bank	Zynq Pin #	PicoZed SDR 2X2 Net	JX4 Pin #	JX4 Pin #	PicoZed SDR 2X2 Net	Zynq Pin #	Zynq Bank
n/a	n/a	GPO_0	1	2	GPO_1	n/a	n/a
n/a	n/a	GPO_2	3	4	GPO_3	n/a	n/a
		GND	5	6	**GND**		
n/a	n/a	AUXADC	7	8	AUXDAC1	n/a	n/a
n/a	n/a	VDDA_GPO_PWR	9	10	AUXDAC2	n/a	n/a
		GND	11	12	**GND**		
12	W16	IO_L24_12_JX4_P	13	14	IO_00_12_JX4	W14	12
12	W15	IO_L24_12_JX4_N	15	16	IO_25_12_JX4	W17	12
		GND	17	18	**GND**		
34	J11	IO_L01_34_JX4_P	19	20	IO_L02_34_JX4_P	G6	34
34	H11	IO_L01_34_JX4_N	21	22	IO_L02_34_JX4_N	G5	34
		GND	23	24	**GND**		
34	H9	IO_L03_34_JX4_P	25	26	IO_L04_34_JX4_P	H7	34
34	G9	IO_L03_34_JX4_N	27	28	IO_L04_34_JX4_N	H6	34
		GND	29	30	**GND**		
34	J10	IO_L05_34_JX4_P	31	32	IO_L06_34_JX4_P	J8	34
34	J9	IO_L05_34_JX4_N	33	34	IO_L06_34_JX4_N	H8	34
34	F5	IO_L07_34_JX4_P	35	36	IO_L08_34_JX4_P	D9	34
34	E5	IO_L07_34_JX4_N	37	38	IO_L08_34_JX4_N	D8	34
		GND	39	40	**GND**		
34	F9	IO_L09_34_JX4_P	41	42	IO_L10_34_JX4_P	E6	34
34	E8	IO_L09_34_JX4_N	43	44	IO_L10_34_JX4_N	D5	34
34	F8	IO_L11_SRCC_34_JX4_P	45	46	IO_L12_MRCC_34_JX4_P	G7	34
34	E7	IO_L11_SRCC_34_JX4_N	47	48	IO_L12_MRCC_34_JX4_N	F7	34
		GND	49	50	**GND**		
34	C8	IO_L13_MRCC_34_JX4_P	51	52	IO_L14_SRCC_34_JX4_P	D6	34
34	C7	IO_L13_MRCC_34_JX4_N	53	54	IO_L14_SRCC_34_JX4_N	C6	34
		GND	55	56	**GND**		
34	C9	IO_L15_34_JX4_P	57	58	IO_L16_34_JX4_P	B10	34
34	B9	IO_L15_34_JX4_N	59	60	IO_L16_34_JX4_N	A10	34
		GND	61	62	**GND**		
n/a	n/a	AD9361_CLK	63	64	IO_25_34_JX4	K10	34
		GND	65	66	**GND**		
34	A9	IO_L17_34_JX4_P	67	68	IO_L18_34_JX4_P	B7	34
34	A8	IO_L17_34_JX4_N	69	70	IO_L18_34_JX4_N	A7	34
		GND	71	72	**GND**		
34	C4	IO_L19_34_JX4_P	73	74	IO_L20_34_JX4_P	B5	34
34	C3	IO_L19_34_JX4_N	75	76	IO_L20_34_JX4_N	B4	34
34	B6	IO_L21_34_JX4_P	77	78	IO_L22_34_JX4_P	A4	34
34	A5	IO_L21_34_JX4_N	79	80	IO_L22_34_JX4_N	A3	34
n/a	n/a	**3V3_I2C**	81	82	*open*		
		GND	83	84	**GND**		
500	C24	PS_MIO15_500_JX4	85	86	PS_MIO12_500_JX4	A23	500
500	A25	PS_MIO10_500_JX4	87	88	PS_MIO11_500_JX4	B26	500
		GND	89	90	**GND**		
500	B25	PS_MIO13_500_JX4	91	92	PS_MIO46_501_JX4	E17	501
500	D23	PS_MIO14_500_JX4	93	94	PS_MIO47_501_JX4	B19	501
		GND	95	96	**GND**		
500	E26	PS_MIO00_500_JX4	97	98	PS_MIO49_501_JX4	A18	501
501	B21	PS_MIO48_501_JX4	99	100	PS_MIO51_501_JX4	B20	501