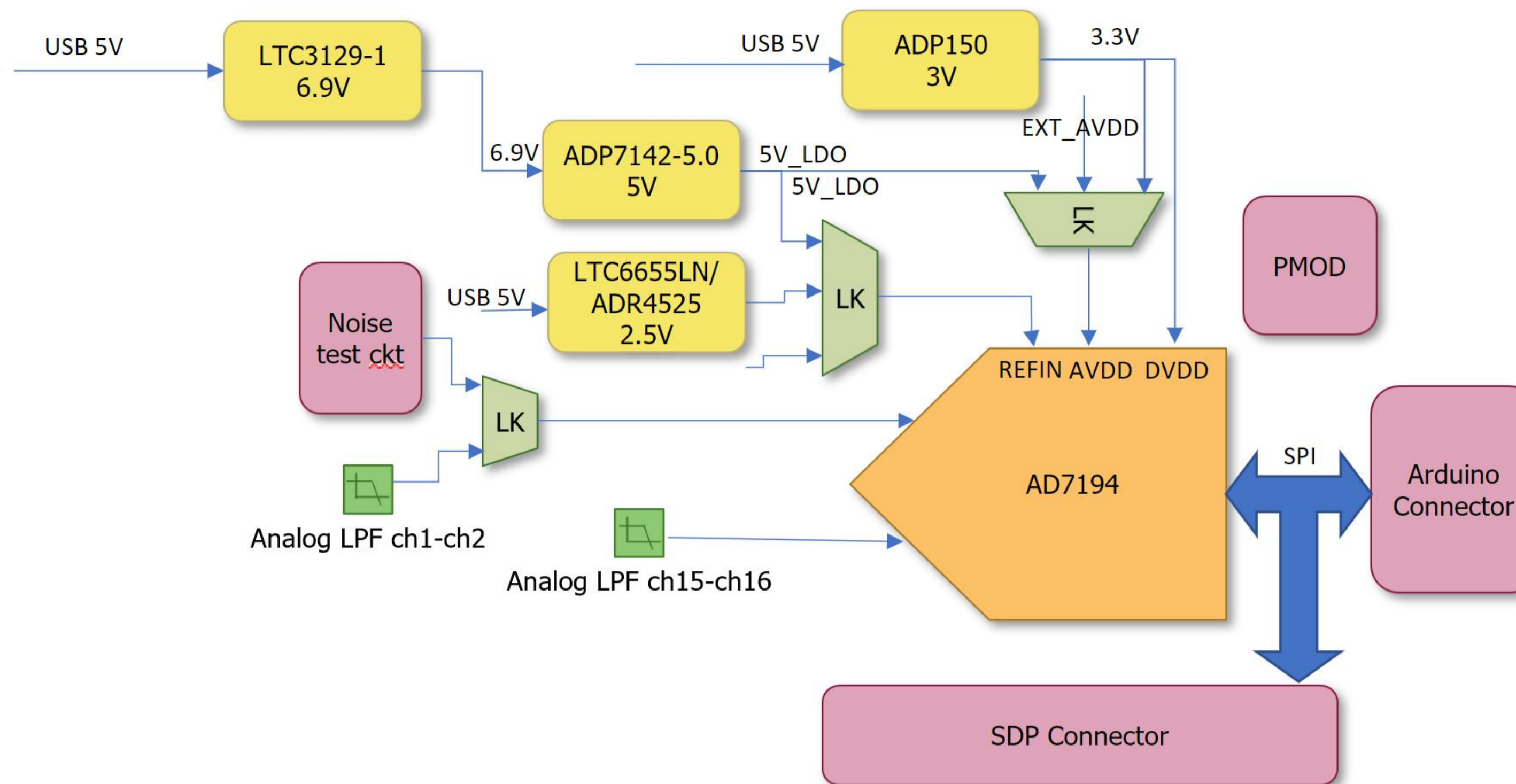


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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	18OCT22	P. AGRAWAL
A1	CHANGES AS PER ECR-111134	24OCT22	P. AGRAWAL



# EVAL-AD7194-ARDZ SCHEMATIC REV (C)

PAGE 2 - POWER CIRCUITRY

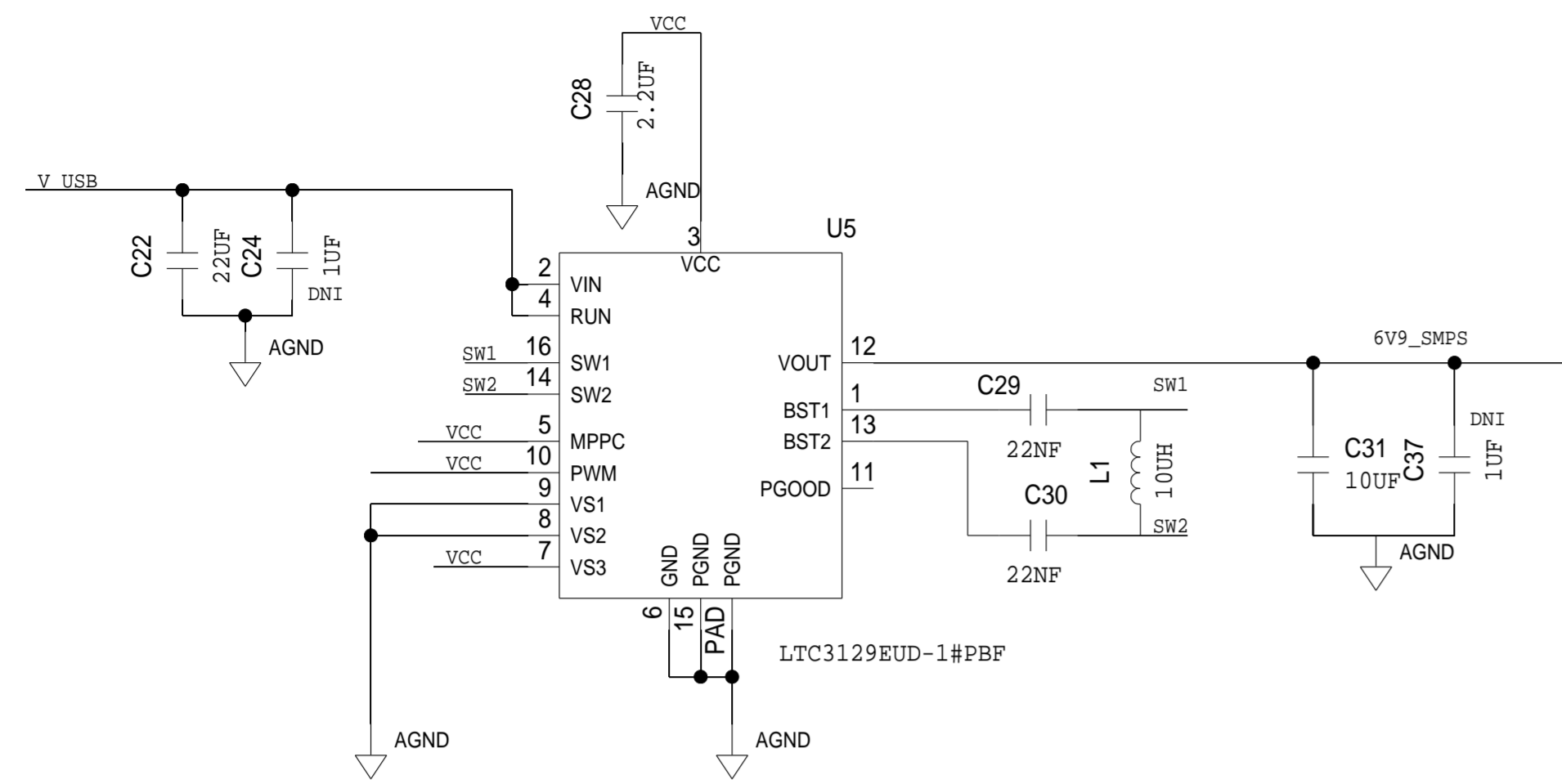
PAGE 3 - AD7194 CIRCUITRY

PAGE 4 - ARDUINO HEADER, PMOD & SDP CONNECTOR

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

TRIP		SCHEMATIC		ANALOG DEVICES	
TEMPLATE ENGINEER	DATE	HW TYPE : Customer Evaluation Z		Product(s): AD7194	
HARDWARE SERVICES	18OCT22	: NA		PACKAGE : LeadCount-lead BodySize PackageType-family	
HARDWARE SYSTEMS		: NA		: Pitch-pitch StyleVendor Style	
TEST ENGINEER		<User Define>		<User Define>	
COMPONENT ENGINEER	18OCT22	<User Define>		<User Define>	
D. TAMISEN		MASTER PROJECT TEMPLATE		TESTER TEMPLATE	
TEST PROCESS		TBD		064489_c	
HARDWARE RELEASE	18OCT22	DRAWING NO.		REV.	
K. JABATAN		02_072728		A	
DESIGNER	18OCT22	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		TOLERANCES	
G. GARCIA		DECIMALS		FRACTIONS	
PTD ENGINEER	18OCT22	X.XX +0.010		+1/32	
P. AGRAWAL		X.XXX +0.005		ANGLES	
CHECKER		+2		SIZE	
		D		SCALE	
		1:1		CODE ID NO.	
		CodeID		SHEET 1 OF 4	

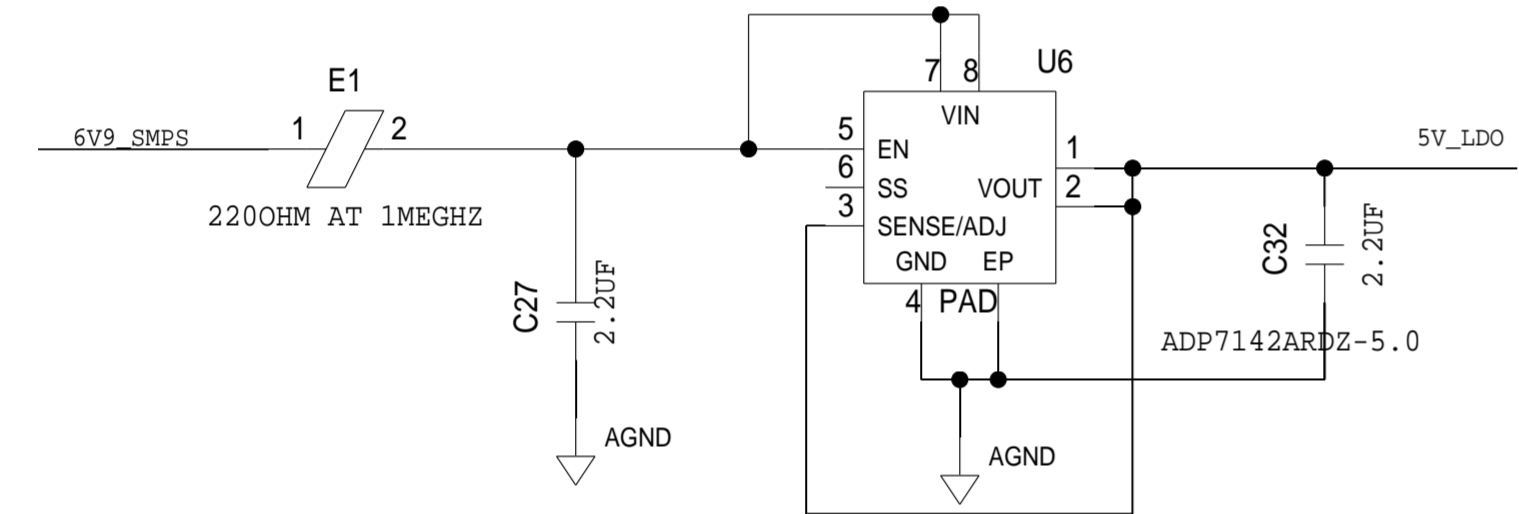
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



6.9V SMPS REGULATOR  
PLACE CAPS C24, C25 AND C31 CLOSE TO IN AND OUT PINS

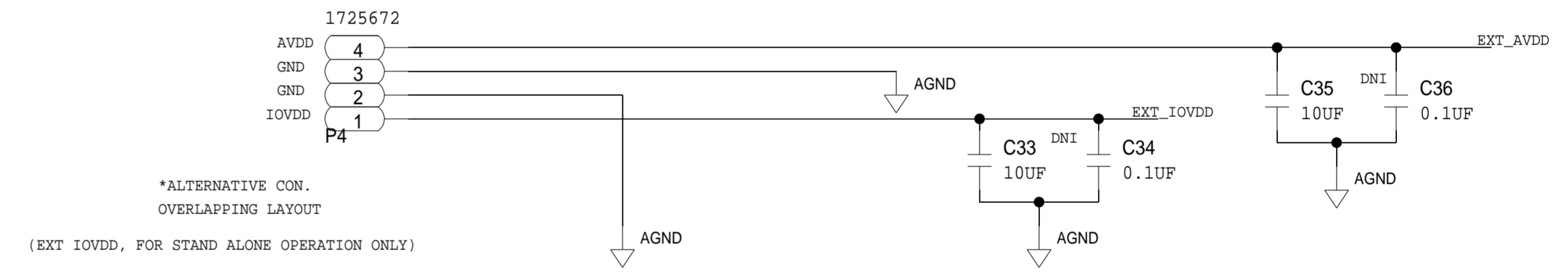
written place caps close to in and out pins

EXTERNAL VOLTAGE CONNECTOR FOR SCP BOARDS

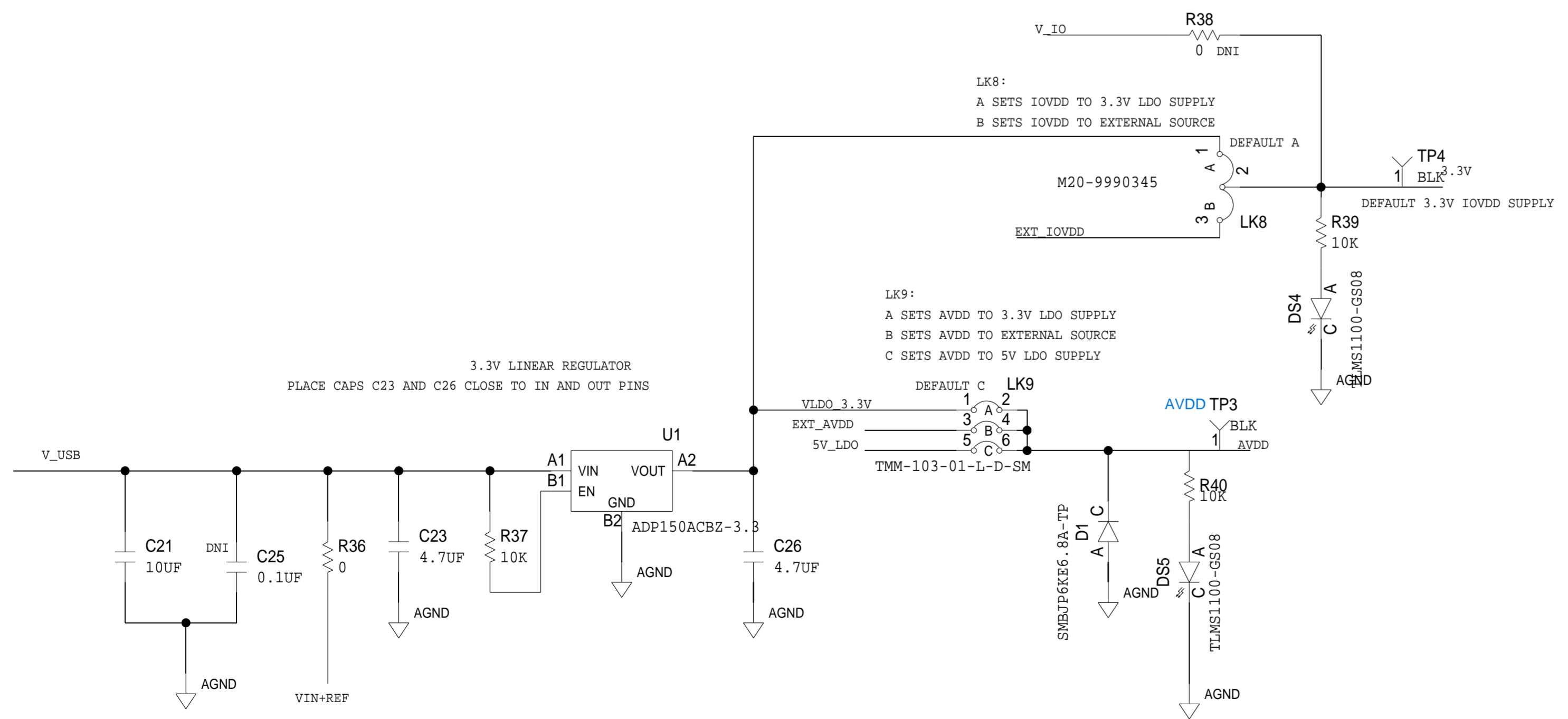


5V LDO REGULATOR  
PLACE CAPS C38, C39 AND C40 CLOSE TO IN AND OUT PINS

written place caps close to in and out pins



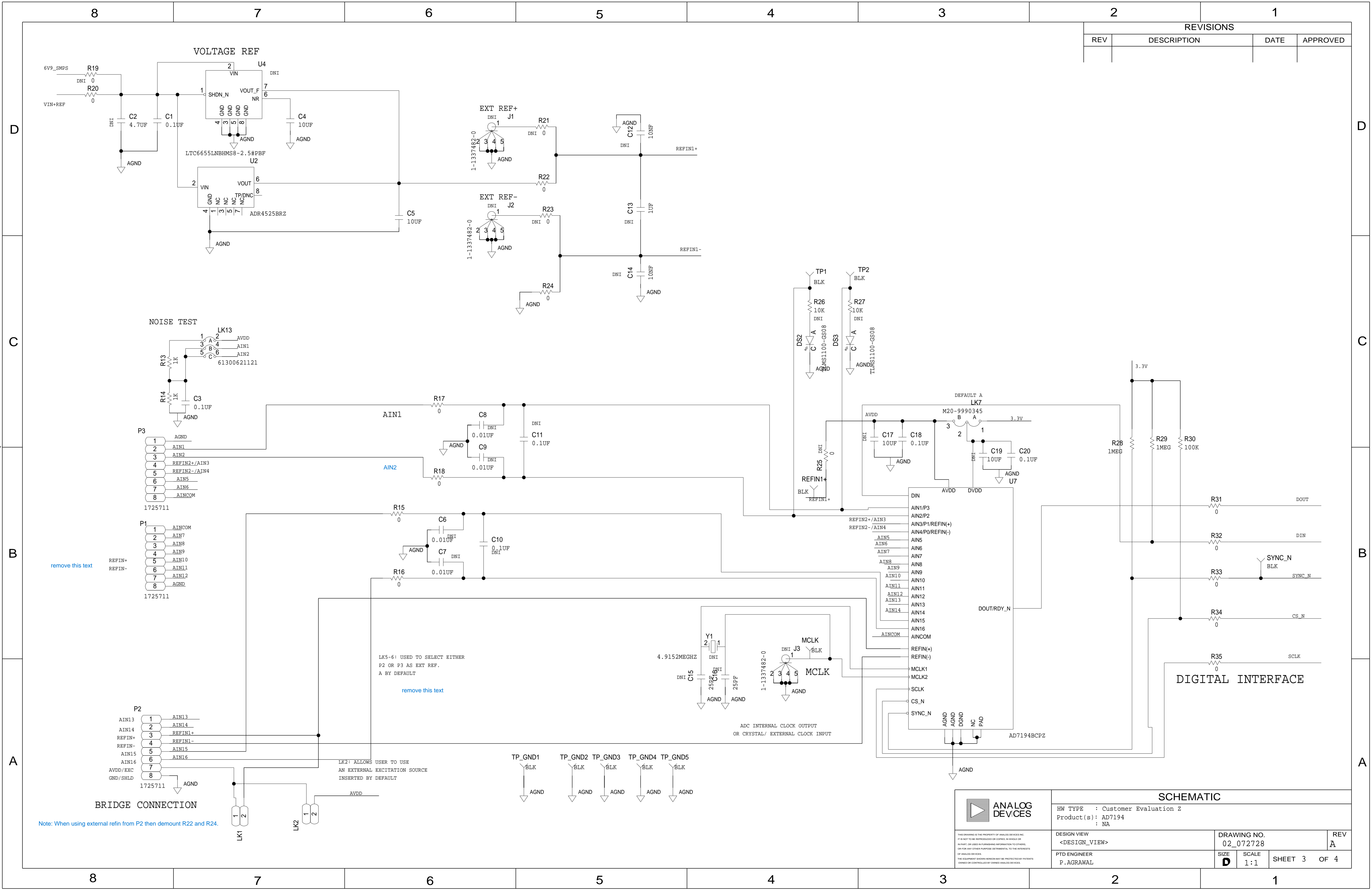
\*ALTERNATIVE CON. OVERLAPPING LAYOUT  
(EXT IOVDD, FOR STAND ALONE OPERATION ONLY)



3.3V LINEAR REGULATOR  
PLACE CAPS C23 AND C26 CLOSE TO IN AND OUT PINS

SCHEMATIC			
		HW TYPE : Customer Evaluation Z Product(s): AD7194 : NA	
DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_072728	
PTD ENGINEER P. AGRAWAL		SIZE <b>D</b>	SCALE 1:1
		SHEET 2 OF 4	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



LK5-6: USED TO SELECT EITHER P2 OR P3 AS EXT REF. A BY DEFAULT

remove this text

LK2: ALLOWS USER TO USE AN EXTERNAL EXCITATION SOURCE INSERTED BY DEFAULT

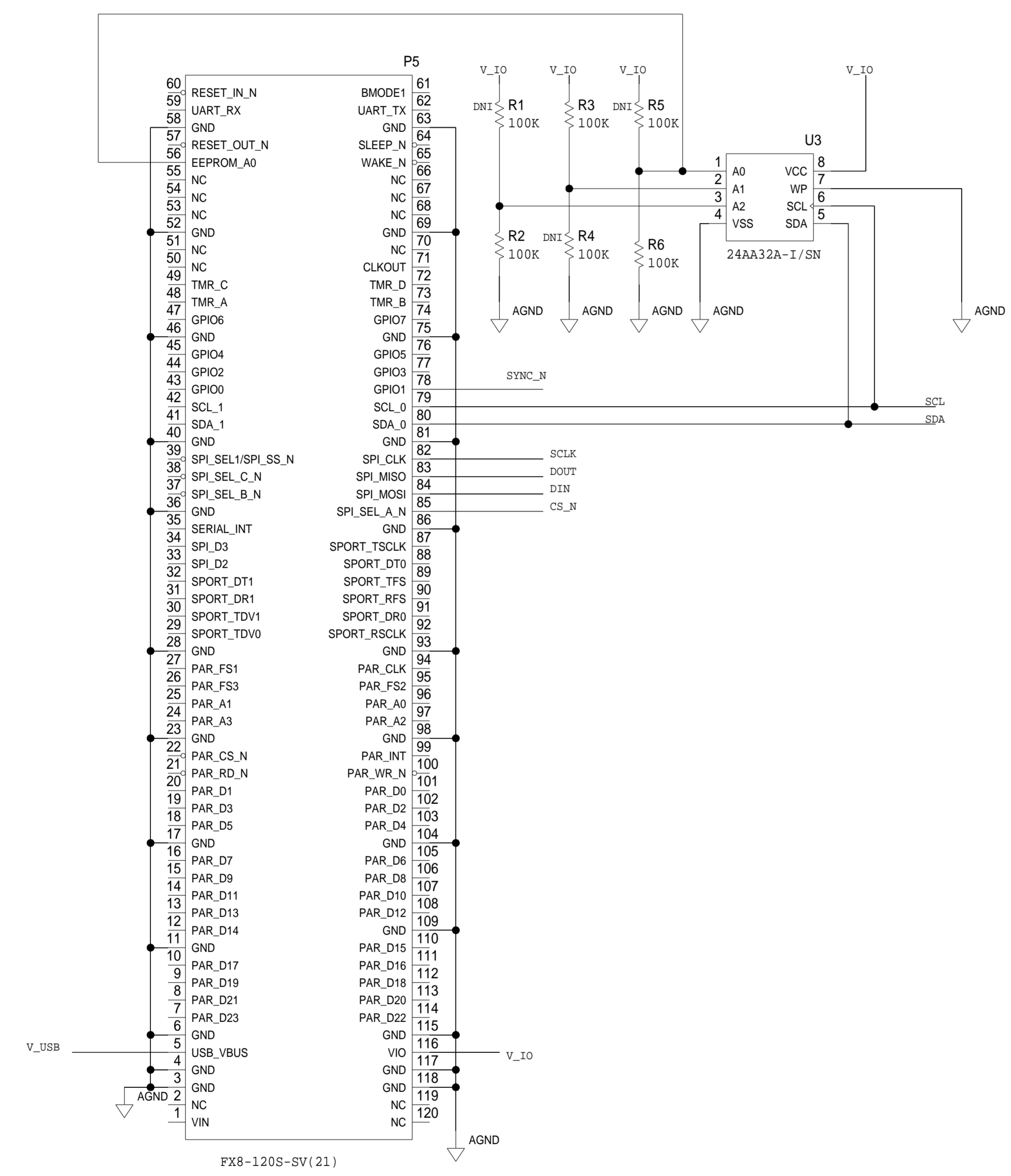
remove this text

ANALOG DEVICES		SCHEMATIC	
HW TYPE : Customer Evaluation Z		Product(s) : AD7194	
DESIGN VIEW : <DESIGN_VIEW>		DRAWING NO. : 02_072728	
PTD ENGINEER : P. AGRAWAL		SIZE : D	SCALE : 1:1
		SHEET 3 OF 4	
		REV : A	

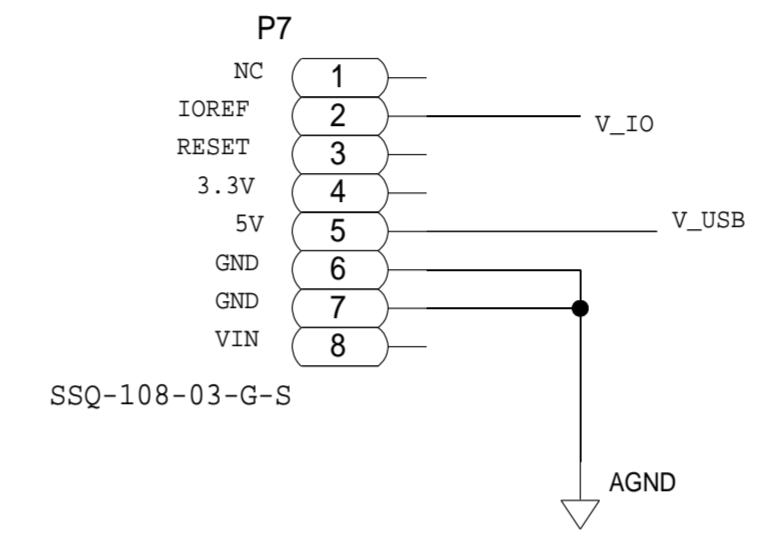
Note: When using external refm from P2 then demount R22 and R24.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

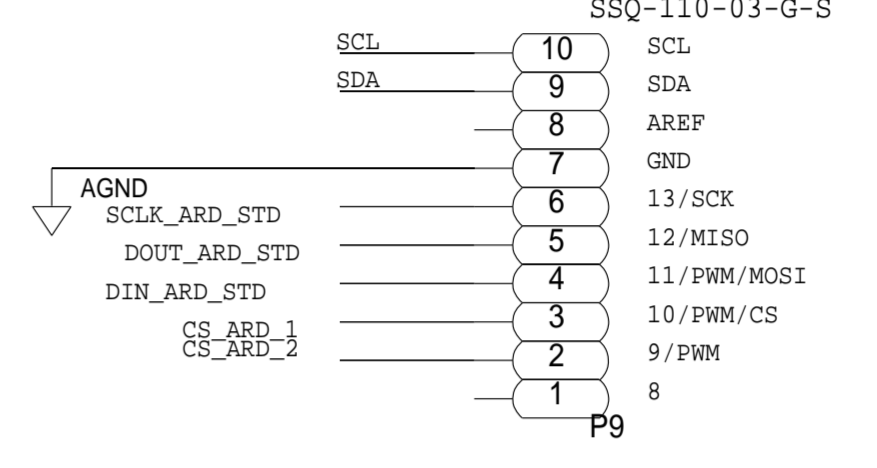
### ARDUNIO HEADER



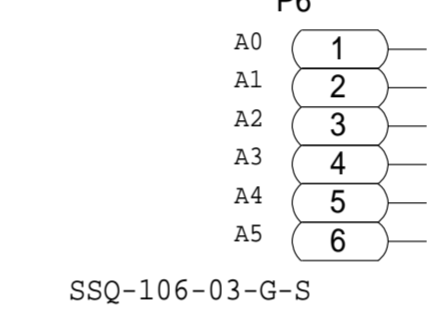
#### POWER



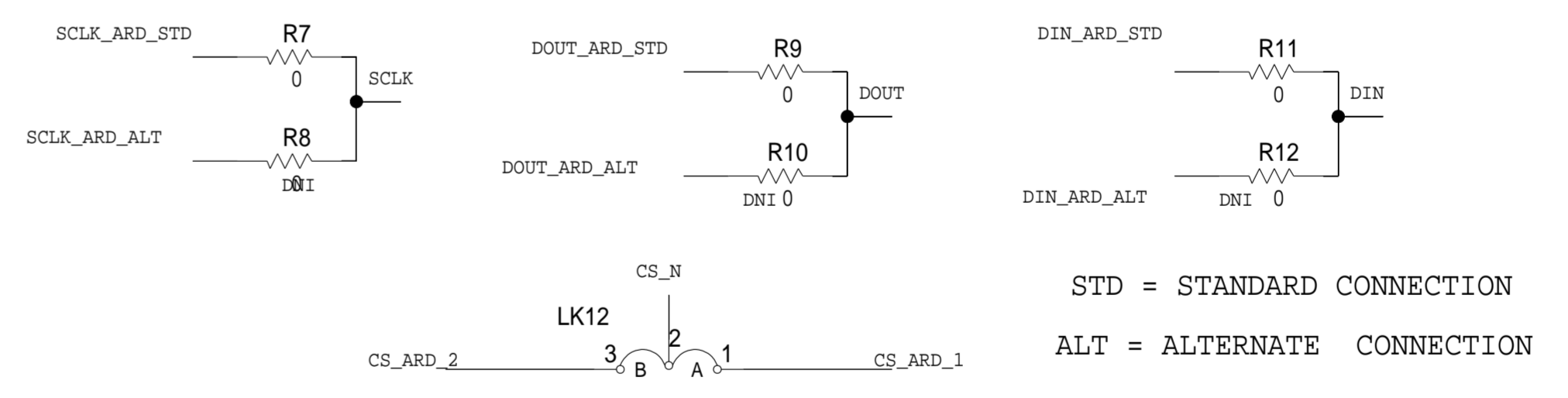
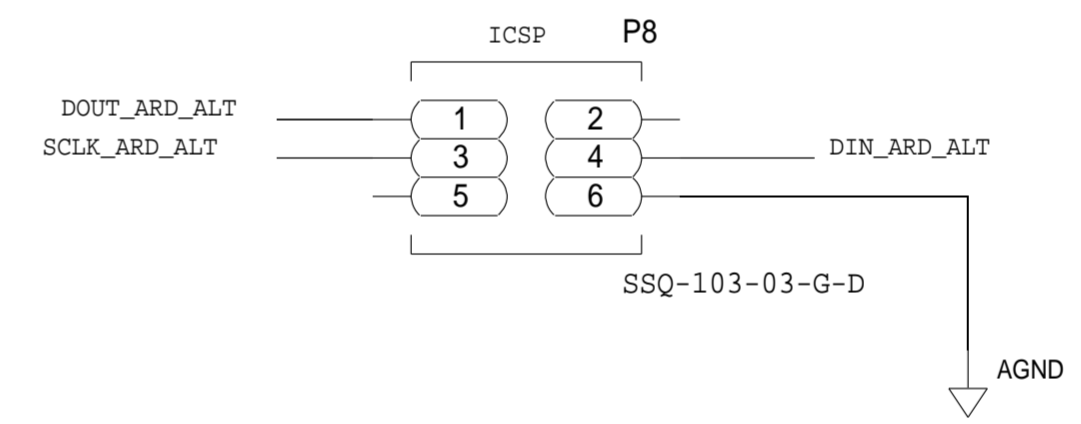
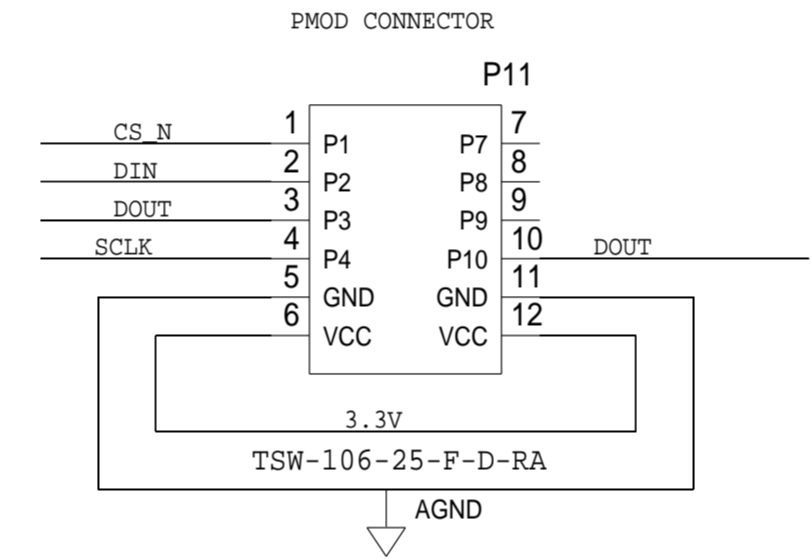
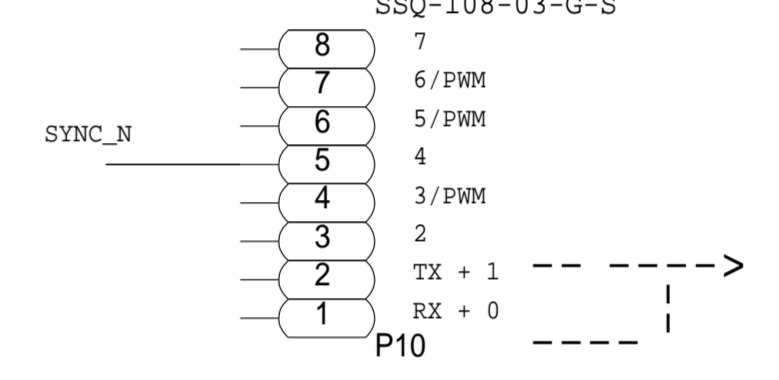
#### DIGI1



#### ANALOG IN



#### DIGI0



#### DEFAULT A

STD = STANDARD CONNECTION  
ALT = ALTERNATE CONNECTION

	<b>SCHEMATIC</b>		
	HW TYPE : Customer Evaluation Z Product(s): AD7194 : NA		
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_072728	REV A	
PTD ENGINEER P. AGRAWAL	SIZE D	SCALE 1:1	SHEET 4 OF 4