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JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
D	CHANGES TO THE SUPPLIES	7-AUG-14	P.H.

RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

AD6676 FMC MEZZANINE

17-OCT-2014

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

TEMPLATE ENGINEER	P ALONGI
DATE	
HARDWARE SERVICES	-
HARDWARE SYSTEMS	-
TEST ENGINEER	-
COMPONENT ENGINEER	-
TEST PROCESS	-
HARDWARE RELEASE	-
DESIGNER	-
PTD ENGINEER	A. DELMURO
CHECKER	-

SCHEMATIC

ANALOG DEVICES

AD6676 FMC EVAL BOARD

MASTER PROJECT TEMPLATE -

TESTER TEMPLATE -

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

DECIMALS	FRACTIONS	ANGLES
X.XX +-0.010 X.XXX +-0.005	+-1/32	+-2

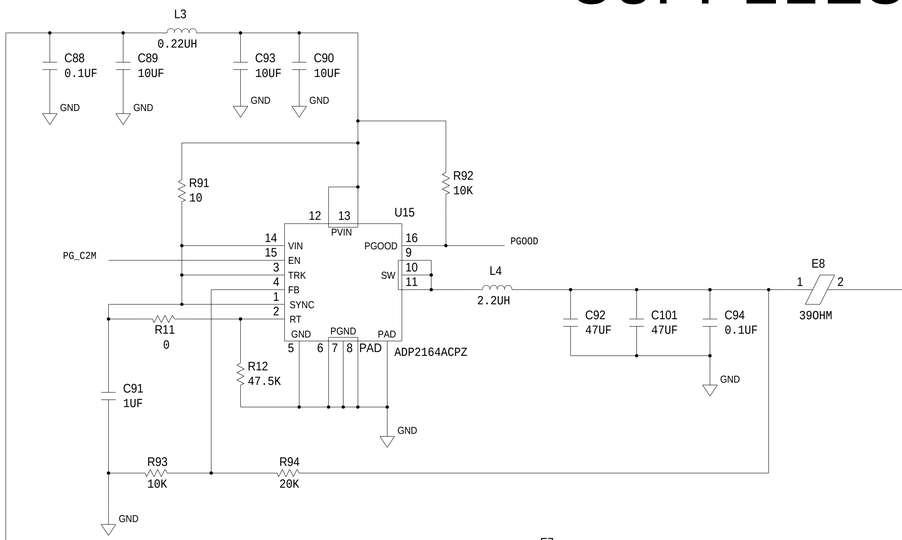
DRAWING NO. HSC 13039

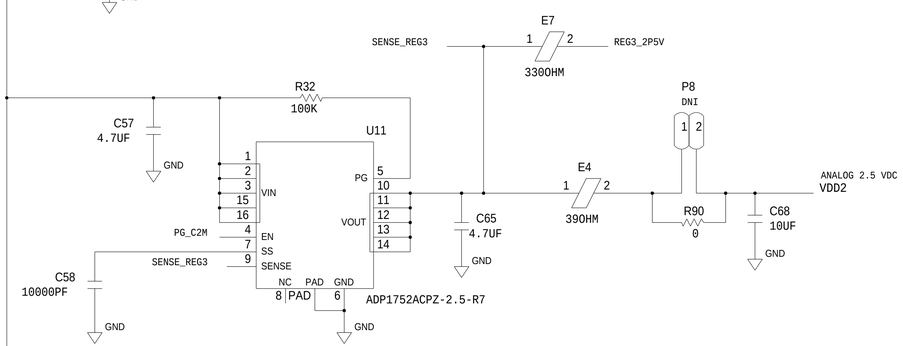
REV. D

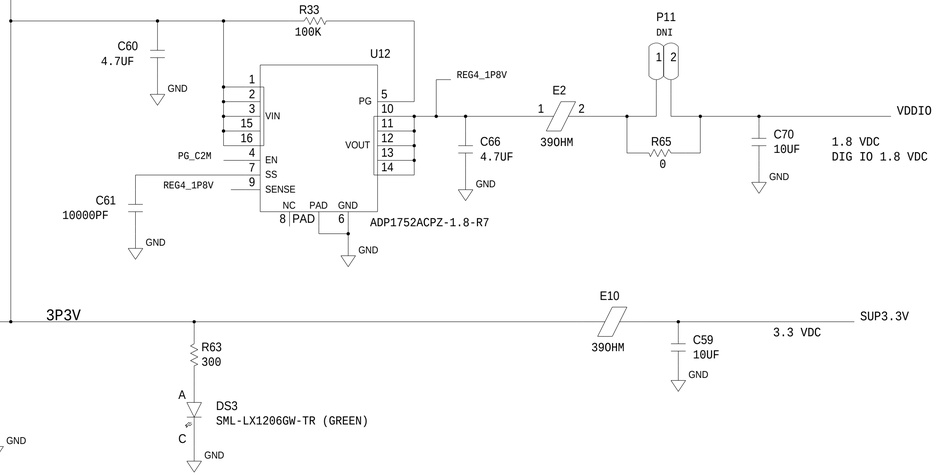
SIZE D | SCALE NONE | CODE ID NO. - | SHEET 1 OF 7

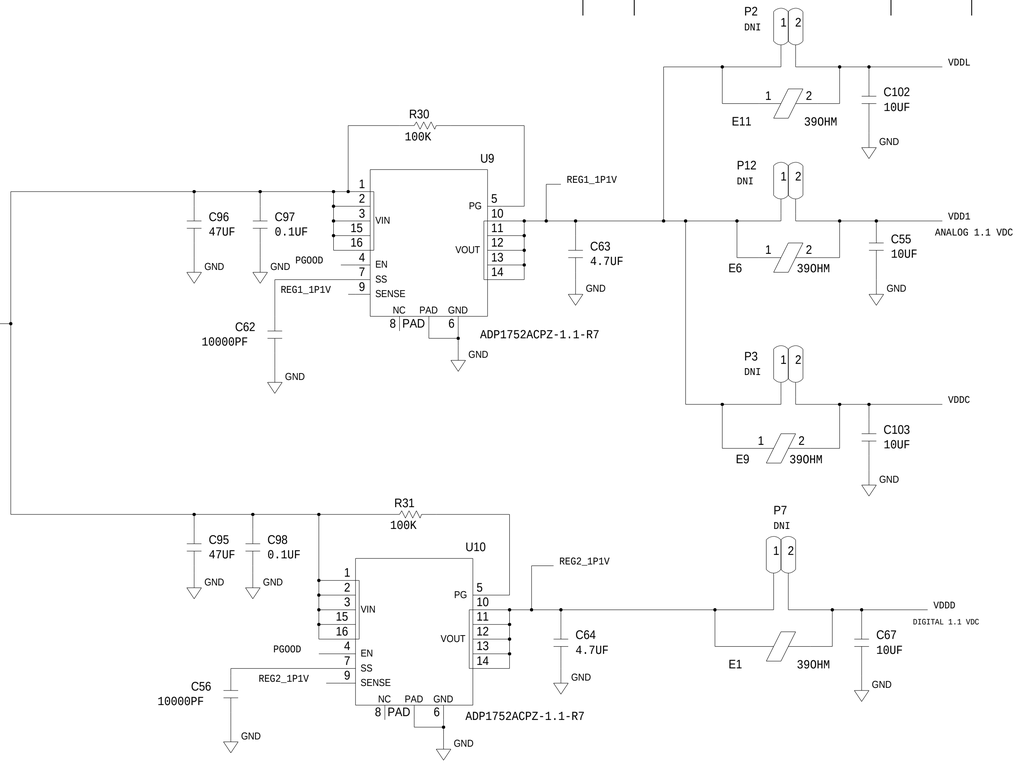
SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

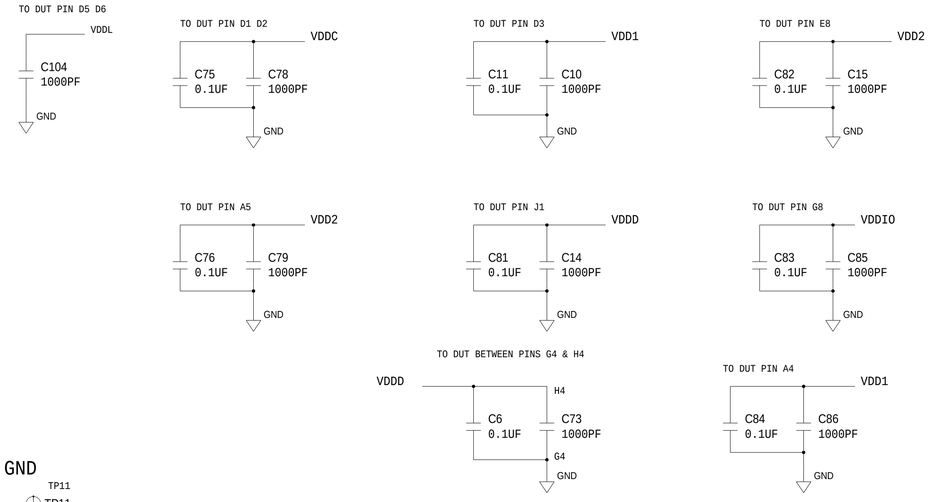


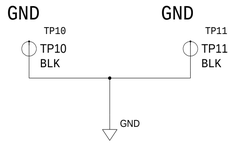






DUT DECOUPLING DETAILS
PLACE .001UF AS CLOSE TO DUT PINS AS POSSIBLE





ANALOG DEVICES

SCHEMATIC

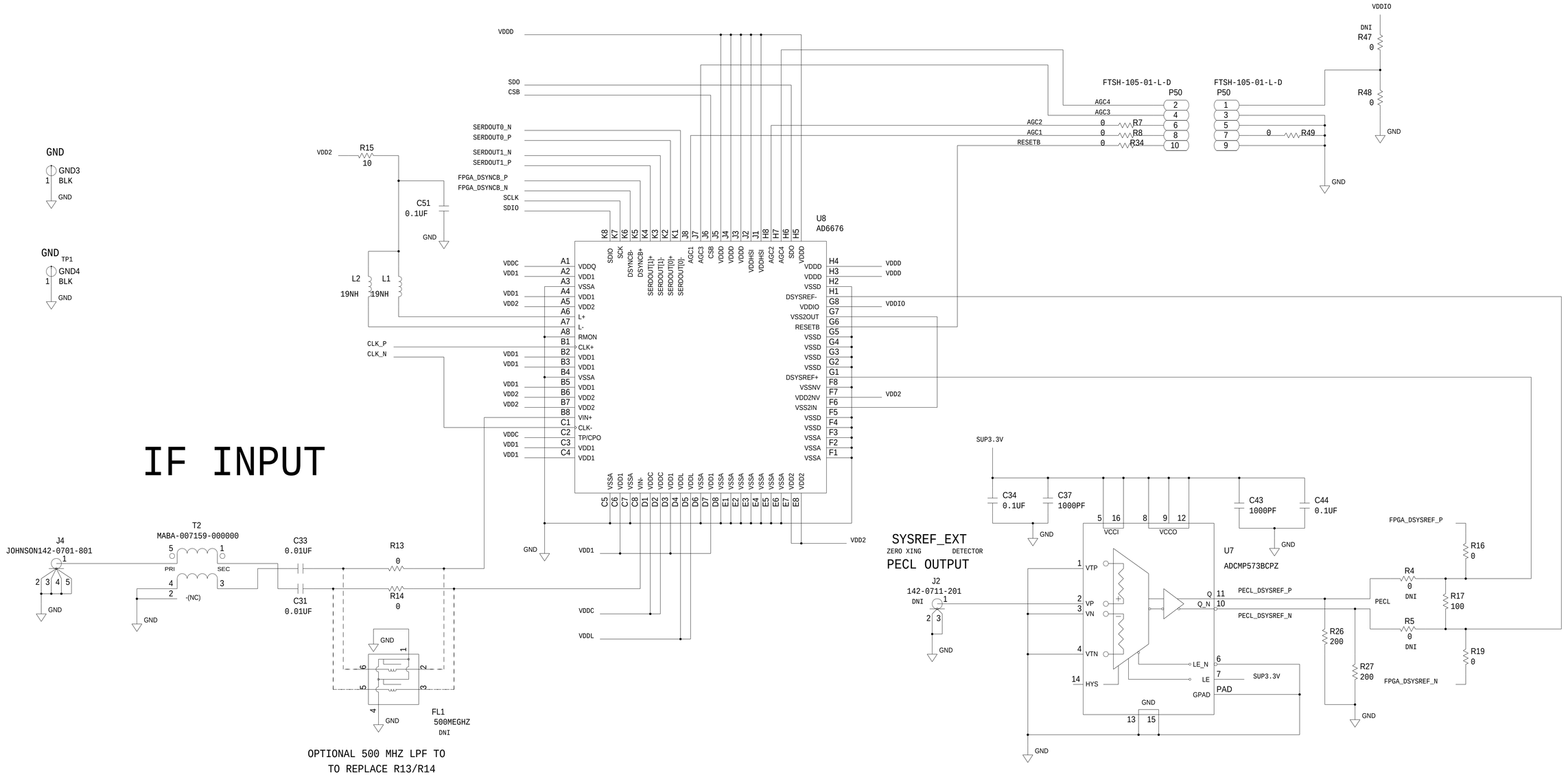
AD6676 FMC EVAL BOARD

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13039		REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 2 OF 7

AD6676 INPUT AND OUTPUTS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

IF INPUT



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

REMOVE BOTH R95 AND R100 WHEN USING EXTERNAL CLKIN SIGNAL SOURCE.

Y1 CAN ALSO USE FOX 774B-200-37
200MHZ FIXED XO

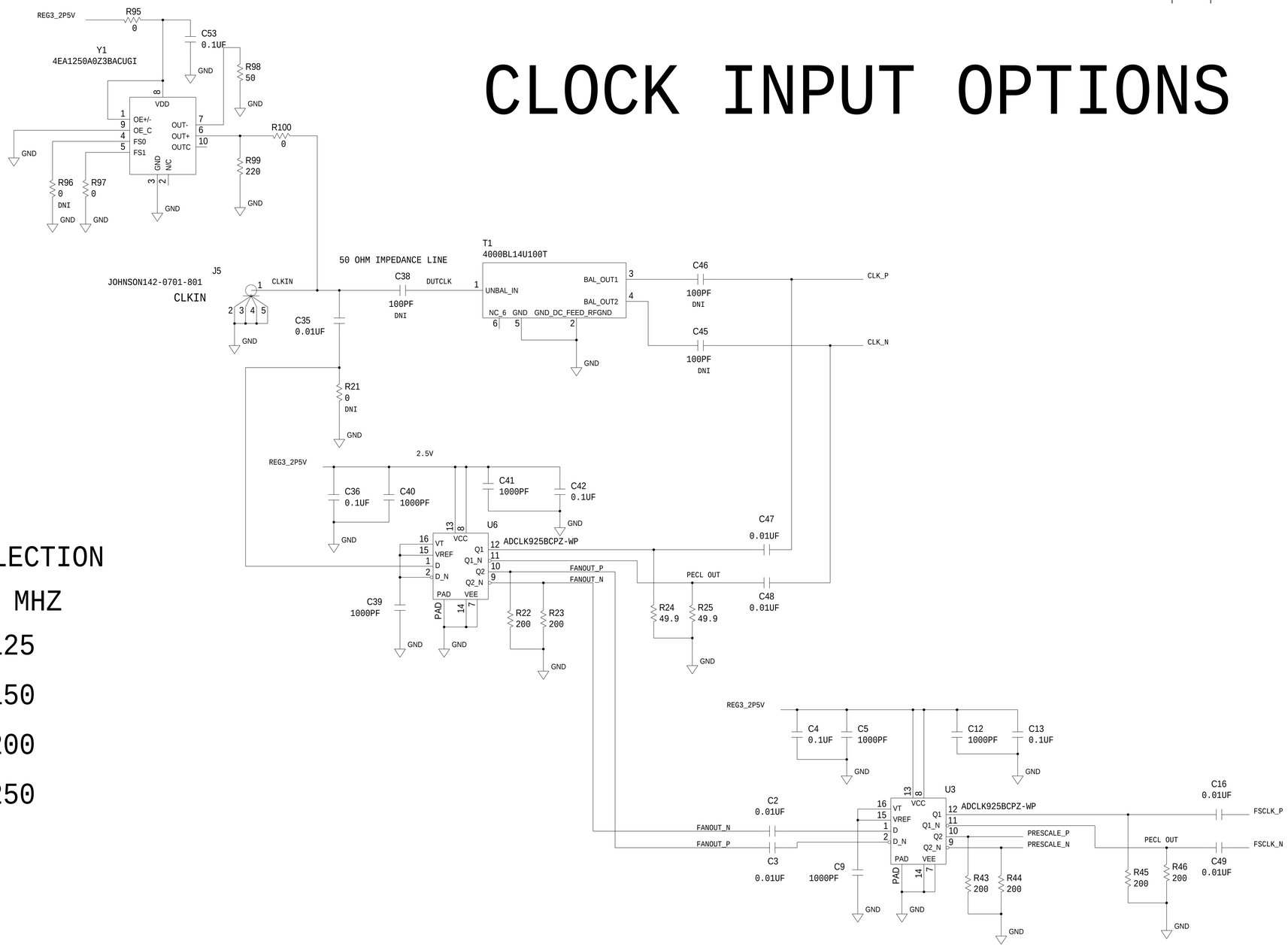
CLOCK INPUT OPTIONS

Y1 FREQUENCY SELECTION

FS0	FS1	FREQ MHZ
0	0	125
S	0	150
0	S	200
S	S	250

0 = OPEN

S = SHORT



ANALOG DEVICES	SCHEMATIC		
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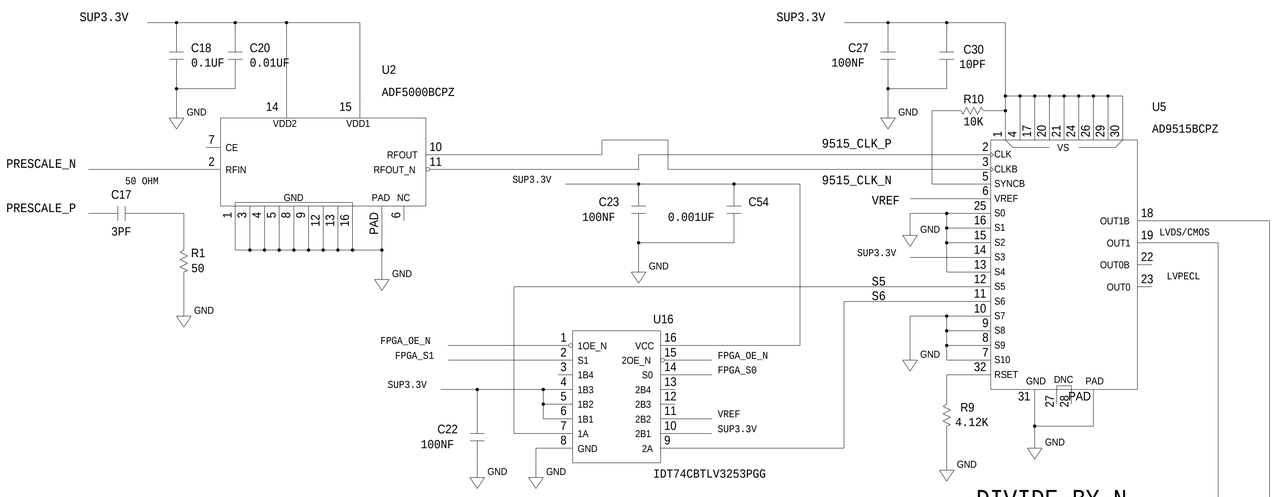
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13039	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 4 OF 7	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

REFERENCE OPTIONS FOR FPGA JESD204B RXPLL

DIVIDER PATH OPTION FOR RF CLKIN

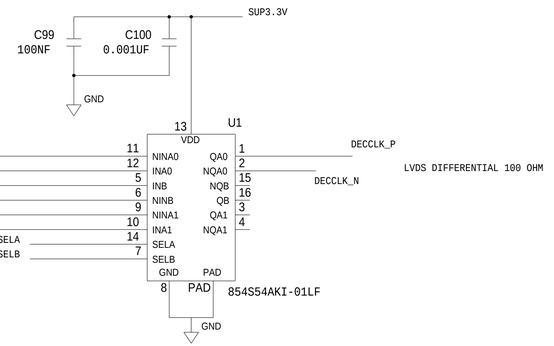


DIVIDE-BY-N

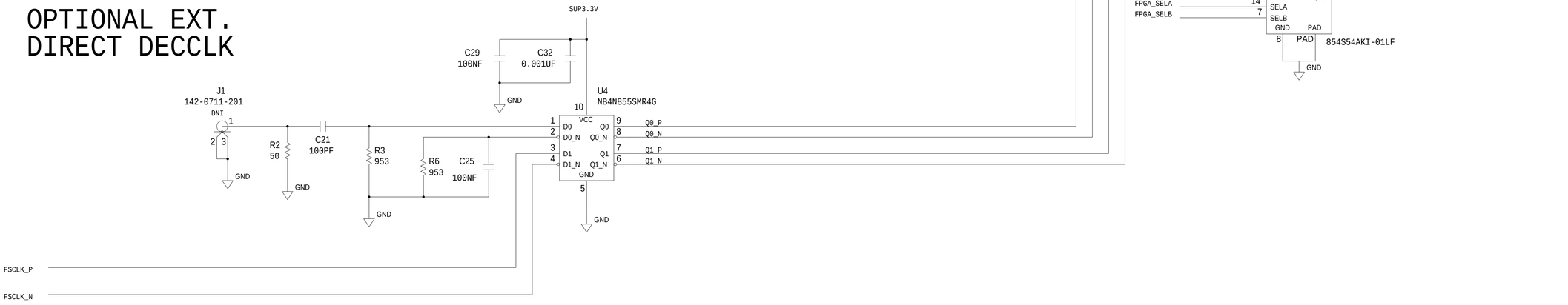
DEC-BY-N	FPGA_OE_N	FPGA_S1	FPGA_S0
32	0	0	0
24	0	0	1
16	0	1	0
12	0	1	1

AD6676

MODE	DEC
1	32
2	24
3	16
4	12



OPTIONAL EXT. DIRECT DECCLK



CLKIN BUFFERED OPTION

ANALOG DEVICES

SCHEMATIC

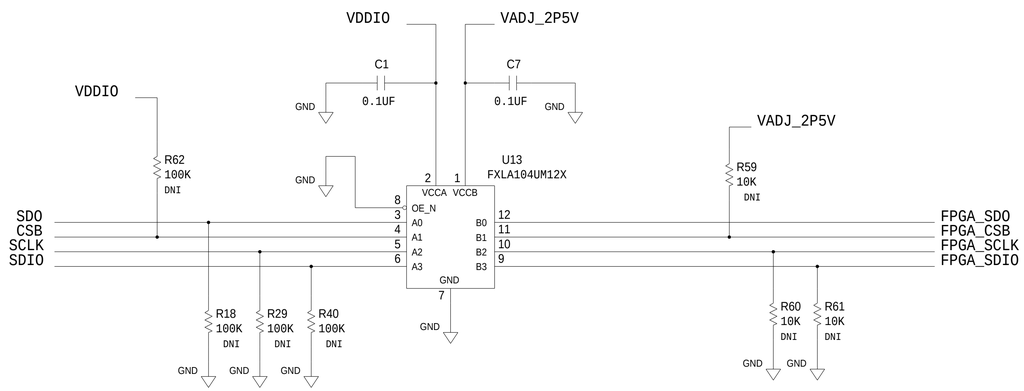
AD6676 FMC EVAL BOARD

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13039	REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 5 OF 7

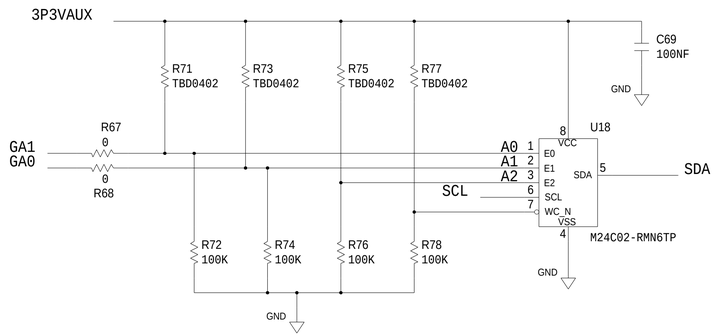
FMC BUFFERED, AC COUPLED SERDOUT & EEPROM
AGC & RESET EXTERNAL OPTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

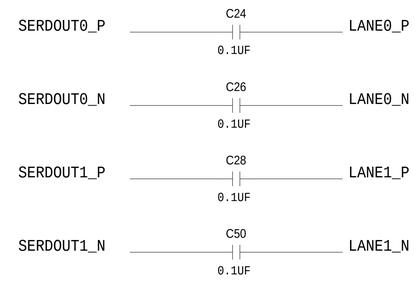
SPI



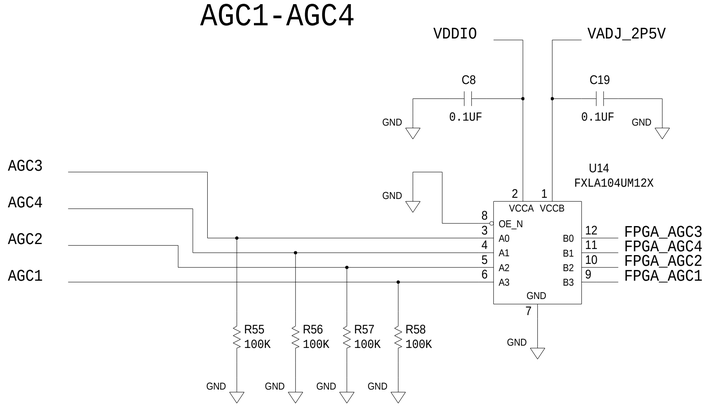
EEPROM



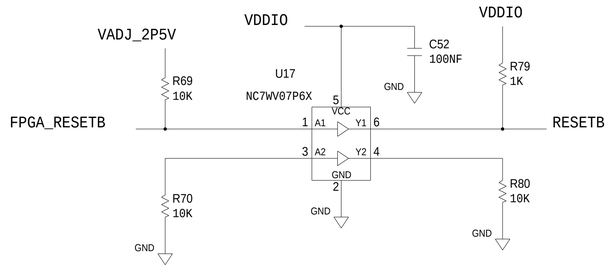
SERDOUT



AGC1-AGC4



RESETB



ANALOG DEVICES	SCHEMATIC	
	AD6676 FMC EVAL BOARD <PRODUCT> <PRODUCT_1>	
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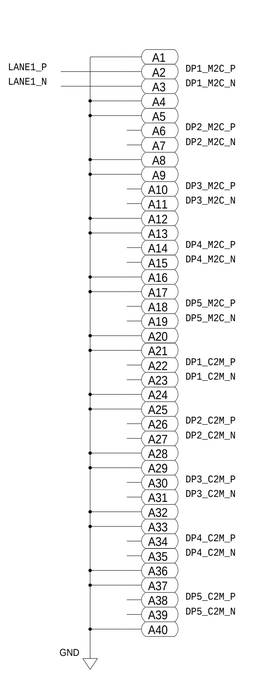
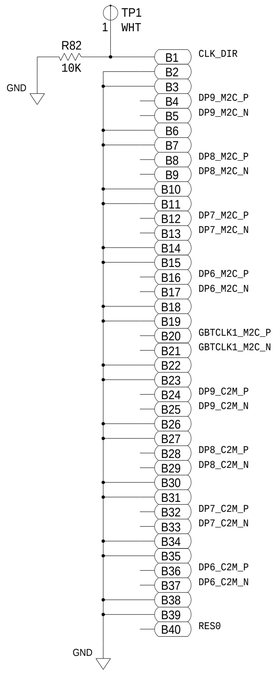
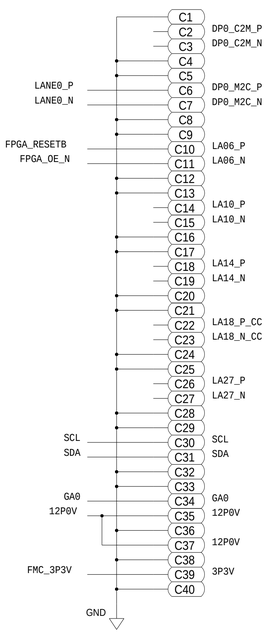
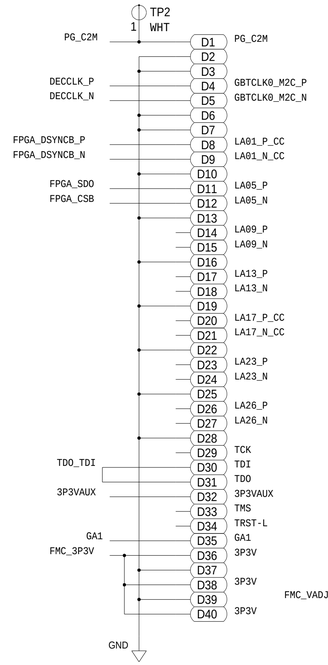
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

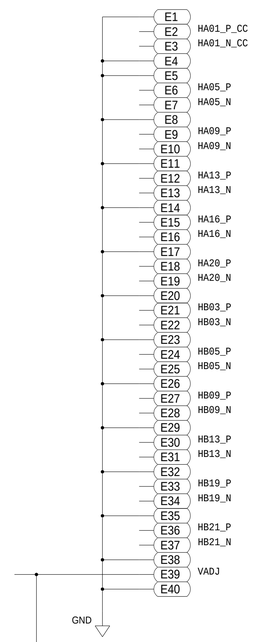
CONNECTOR SHOULD MOUNT ON SOLDER SIDE (BOTTOM).

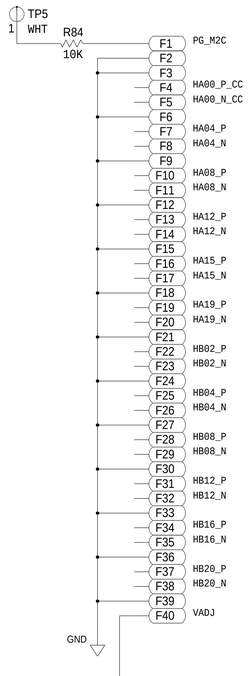


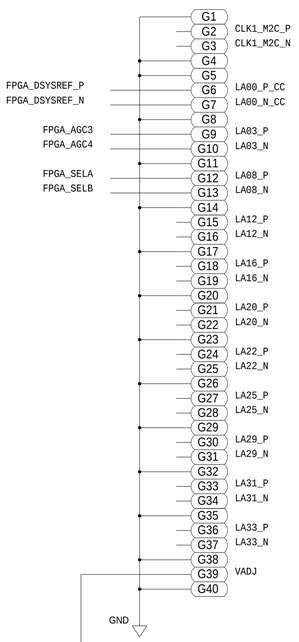


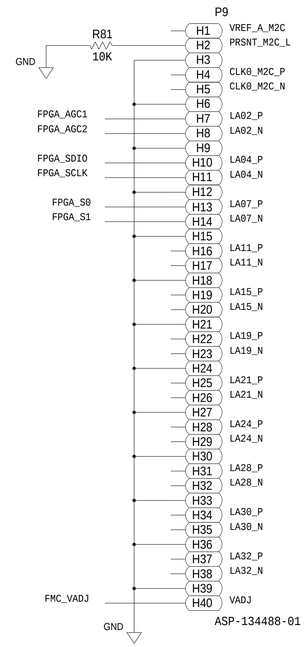


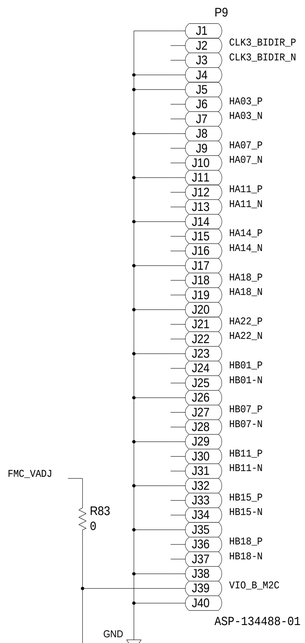


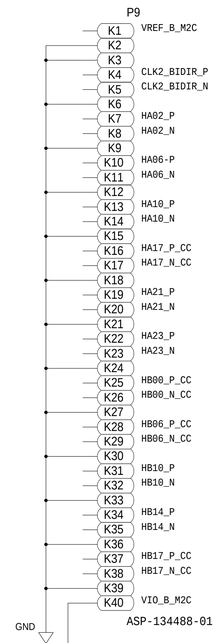


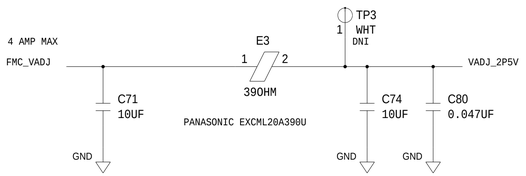




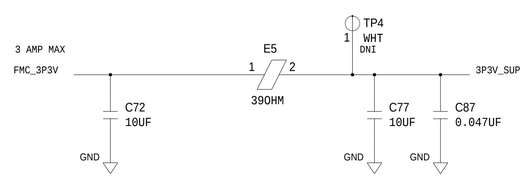








FMC VADJ 2P5V SUPPLY



FMC 3P3V SUPPLY

FILTER NETWORKS NEAR FMC CONNECTOR

DECCLK -> 2.5V LVDS

SERDOUT -> CML

DSYSREF DIFF -> 2.5V LVDS

DSYNCB DIFF -> 2.5V LVDS

CSB, SDO, SDI, SCLK -> LVCMOS 1.8V

AGC1-AGC4, RESETB -> LVCMOS 1.8V

ANALOG DEVICES

SCHEMATIC

AD6676 FMC EVAL BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13039	REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 7 OF 7