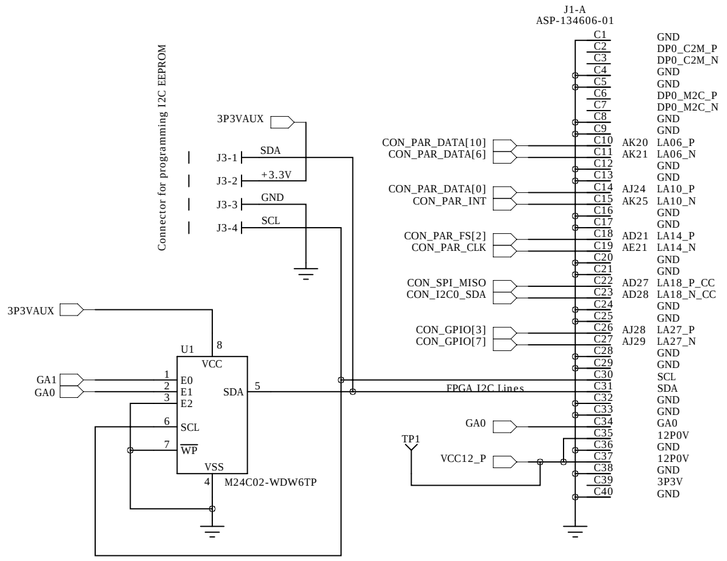
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

FMC-LPC Connector



EEPROM required in VITA standard
I2C line pull-up resistors on FPGA board

J1-A
ASP-134606-01

C1			GND
C2			DP0_C2M_P
C3			DP0_C2M_N
C4			GND
C5			GND
C6			DP0_M2C_P
C7			DP0_M2C_N
C8			GND
C9			GND
C10	AK20	LA06_P	CON_PAR_DATA[10]
C11	AK21	LA06_N	CON_PAR_DATA[6]
C12		GND	
C13		GND	
C14	AJ24	LA10_P	CON_PAR_DATA[0]
C15	AK25	LA10_N	CON_PAR_INT
C16		GND	
C17		GND	
C18	AD21	LA14_P	CON_PAR_FS[2]
C19	AE21	LA14_N	CON_PAR_CLK
C20		GND	
C21		GND	
C22	AD27	LA18_P_CC	CON_SPI_MISO
C23	AD28	LA18_N_CC	CON_I2C0_SDA
C24		GND	
C25		GND	
C26	AJ28	LA27_P	CON_GPIO[3]
C27	AJ29	LA27_N	CON_GPIO[7]
C28		GND	
C29		GND	
C30		SCL	
C31		SDA	
C32		GND	
C33		GND	
C34		GA0	
C35		12P0V	
C36		GND	
C37		12P0V	
C38		GND	
C39		3P3V	
C40		GND	

J1-B
ASP-134606-01

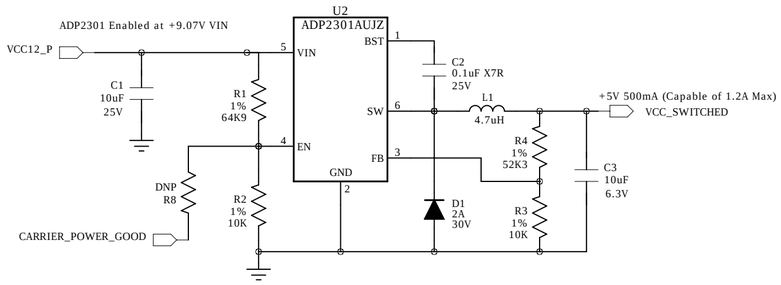
D1			PG_C2M
D2			GND
D3			GND
D4			GBTCLK0_M2C_P
D5			GBTCLK0_M2C_N
D6			GND
D7			GND
D8	AE23	LA01_P_CC	CON_PAR_DATA[15]
D9	AF23	LA01_N_CC	CON_PAR_DATA[12]
D10		GND	
D11	AG22	LA05_P	CON_PAR_DATA[8]
D12	AH22	LA05_N	CON_PAR_DATA[4]
D13		GND	
D14	AK23	LA09_P	CON_PAR_DATA[2]
D15	AK24	LA09_N	CON_PAR_WR
D16		GND	
D17	AB24	LA13_P	CON_PAR_ADDR[2]
D18	AC25	LA13_N	CON_PAR_ADDR[0]
D19		GND	
D20	AB27	LA17_P_CC	CON_SPI_SEL_A
D21	AC27	LA17_N_CC	CON_SPI_MOSI
D22		GND	
D23	AH26	LA23_P	CON_SPI_CLK
D24	AH27	LA23_N	CON_I2C0_SCL
D25		GND	
D26	AK29	LA26_P	CON_GPIO[1]
D27	AK30	LA26_N	CON_GPIO[5]
D28		GND	
D29		TCK	
D30		TDI	
D31		TDO	
D32		3P3VAUX	3P3VAUX
D33		TMS	
D34		TRST_L	
D35		GA1	GA1
D36		3P3V	
D37		GND	
D38		3P3V	
D39		GND	
D40		3P3V	

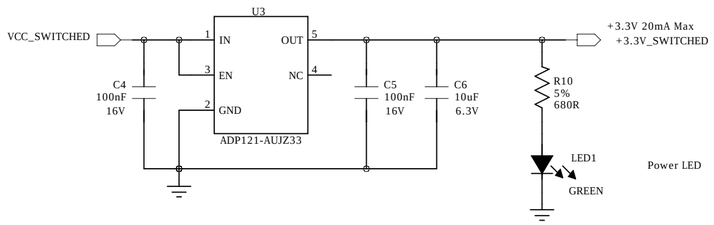
J1-C
ASP-134606-01

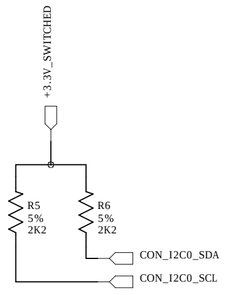
G1			GND
G2			CLK1_M2C_P
G3			CLK1_M2C_N
G4			GND
G5			GND
G6	AD23	LA00_P_CC	CON_PAR_DATA[11]
G7	AE24	LA00_N_CC	CON_PAR_DATA[7]
G8		GND	
G9	AG20	LA03_P	CON_PAR_DATA[3]
G10	AH20	LA03_N	CON_PAR_RD
G11		GND	
G12	AJ22	LA08_P	CON_PAR_ADDR[3]
G13	AJ23	LA08_N	CON_PAR_FS[3]
G14		GND	
G15	AA20	LA12_P	CON_SPORT_DR1
G16	AB20	LA12_N	CON_SPORT_RSCLK
G17		GND	
G18	AC22	LA16_P	CON_SPORT_RFS
G19	AD22	LA16_N	CON_SPORT_DT0
G20		GND	
G21	AF26	LA20_P	CON_SER_INT
G22	AF27	LA20_N	CON_SPI_SEL_C
G23		GND	
G24	AJ27	LA22_P	CON_I2C1_SCL
G25	AK28	LA22_N	CON_GPIO[2]
G26		GND	
G27	AC26	LA25_P	CON_GPIO[6]
G28	AD26	LA25_N	LPC_RESET
G29		GND	
G30	AE28	LA29_P	CON_TMR_B
G31	AF28	LA29_N	CON_CLKOUT
G32		GND	
G33	AD29	LA31_P	
G34	AE29	LA31_N	
G35		GND	
G36	AC29	LA33_P	
G37	AC30	LA33_N	
G38		GND	
G39		VADJ	
G40		GND	

J1-D
ASP-134606-01

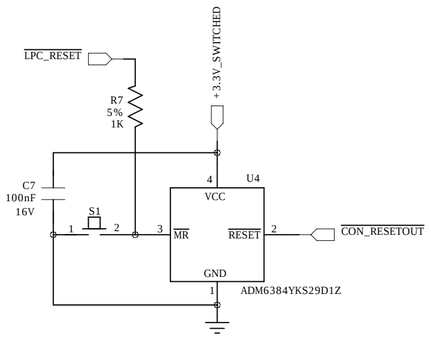
H1			VREF_A_M2C
H2		PRSNT_M2C_L	Board present pin
H3		GND	
H4	AF22	CLK0_M2C_P	CON_PAR_DATA[14]
H5	AG23	CLK0_M2C_N	CON_PAR_DATA[13]
H6		GND	
H7	AF20	LA02_P	CON_PAR_DATA[9]
H8	AF21	LA02_N	CON_PAR_DATA[5]
H9		GND	
H10	AH21	LA04_P	CON_PAR_DATA[1]
H11	AJ21	LA04_N	CON_PAR_CS
H12		GND	
H13	AG25	LA07_P	CON_PAR_ADDR[1]
H14	AH25	LA07_N	CON_PAR_FS[1]
H15		GND	
H16	AE25	LA11_P	CON_SPORT_DT1
H17	AF25	LA11_N	CON_SPORT_DR0
H18		GND	
H19	AC24	LA15_P	CON_SPORT_TFS
H20	AD24	LA15_N	CON_SPORT_TSCLK
H21		GND	
H22	AJ26	LA19_P	CON_SPI_SEL_B
H23	AK26	LA19_N	CON_I2C1_SDA
H24		GND	
H25	AG27	LA21_P	CON_GPIO[0]
H26	AG28	LA21_N	CON_GPIO[4]
H27		GND	
H28	AG30	LA24_P	CON_TMR_A
H29	AH30	LA24_N	CON_UART_RX
H30		GND	
H31	AE30	LA28_P	CON_TMR_D
H32	AF30	LA28_N	CON_UART_TX
H33		GND	
H34	AB29	LA30_P	
H35	AB30	LA30_N	
H36		GND	
H37	Y30	LA32_P	
H38	AA30	LA32_N	
H39		GND	
H40		VADJ	







2K2 Pull-ups for 1st I2C bus
(None needed for 2nd I2C bus)

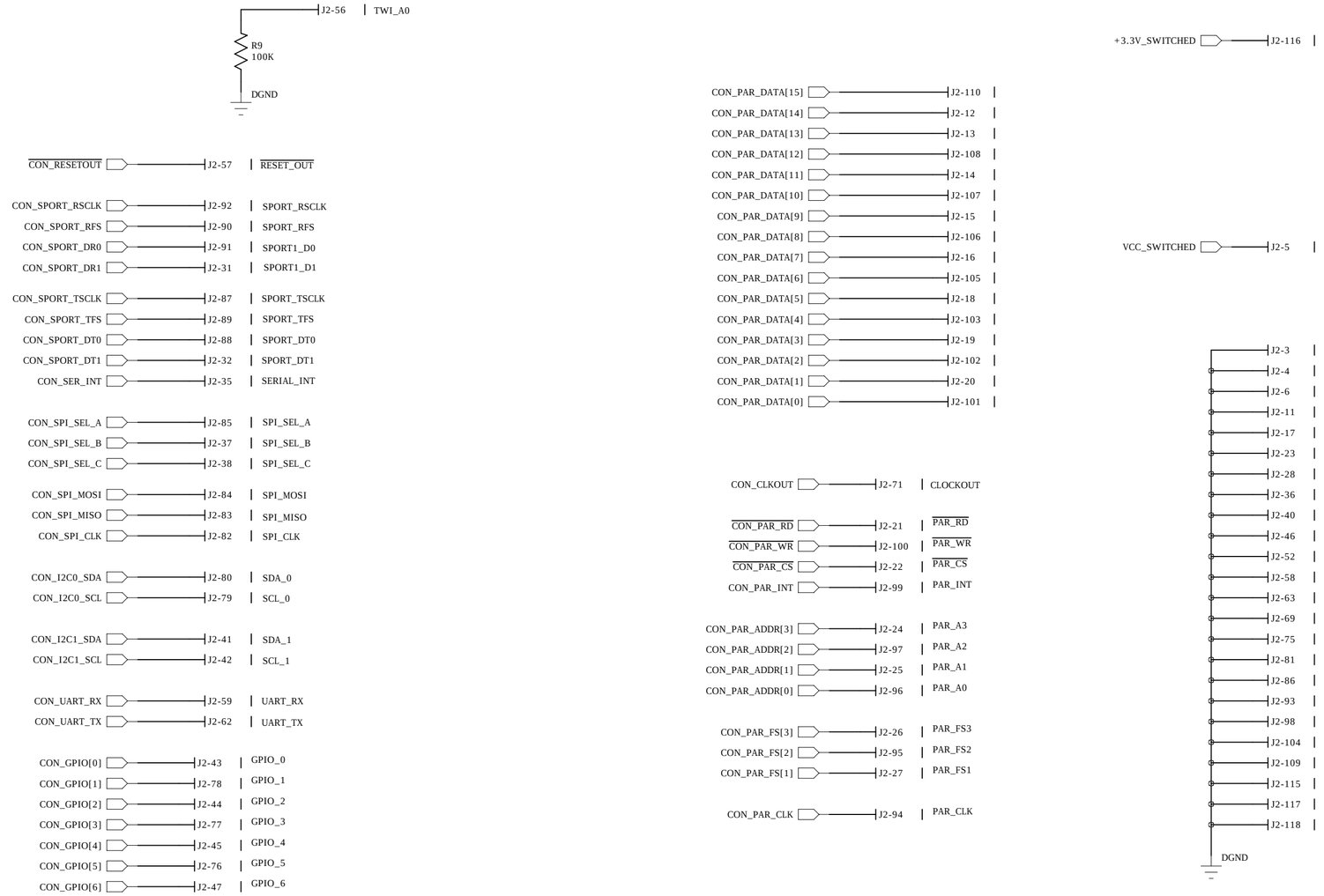


Power-on reset and reset by FPGA of SDP daughter board

DRAWN: E. WALSH	DATED: 14/12/11	COMPANY: ANALOG DEVICES	
CHECKED: E.WALSH	DATED: <Checked Date>	TITLE: SDP-FMC INTERPOSER BOARD	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: SDP-I-FMC	REV: 1
		SCALE: <Scale>	SHEET: 1OF 2

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

SDP Connector



DRAWN: E. WALSH	DATED: 14/12/11	
CHECKED: E.WALSH	DATED: <Checked Date>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	
RELEASED: <Released By>	DATED: <Release Date>	

COMPANY: ANALOG DEVICES

TITLE: SDP-FMC INTERPOSER BOARD

CODE:	SIZE:	DRAWING NO:	REV:
<Code>	C	SDP-I-FMC	1

SCALE: <Scale> SHEET: 2OF 2