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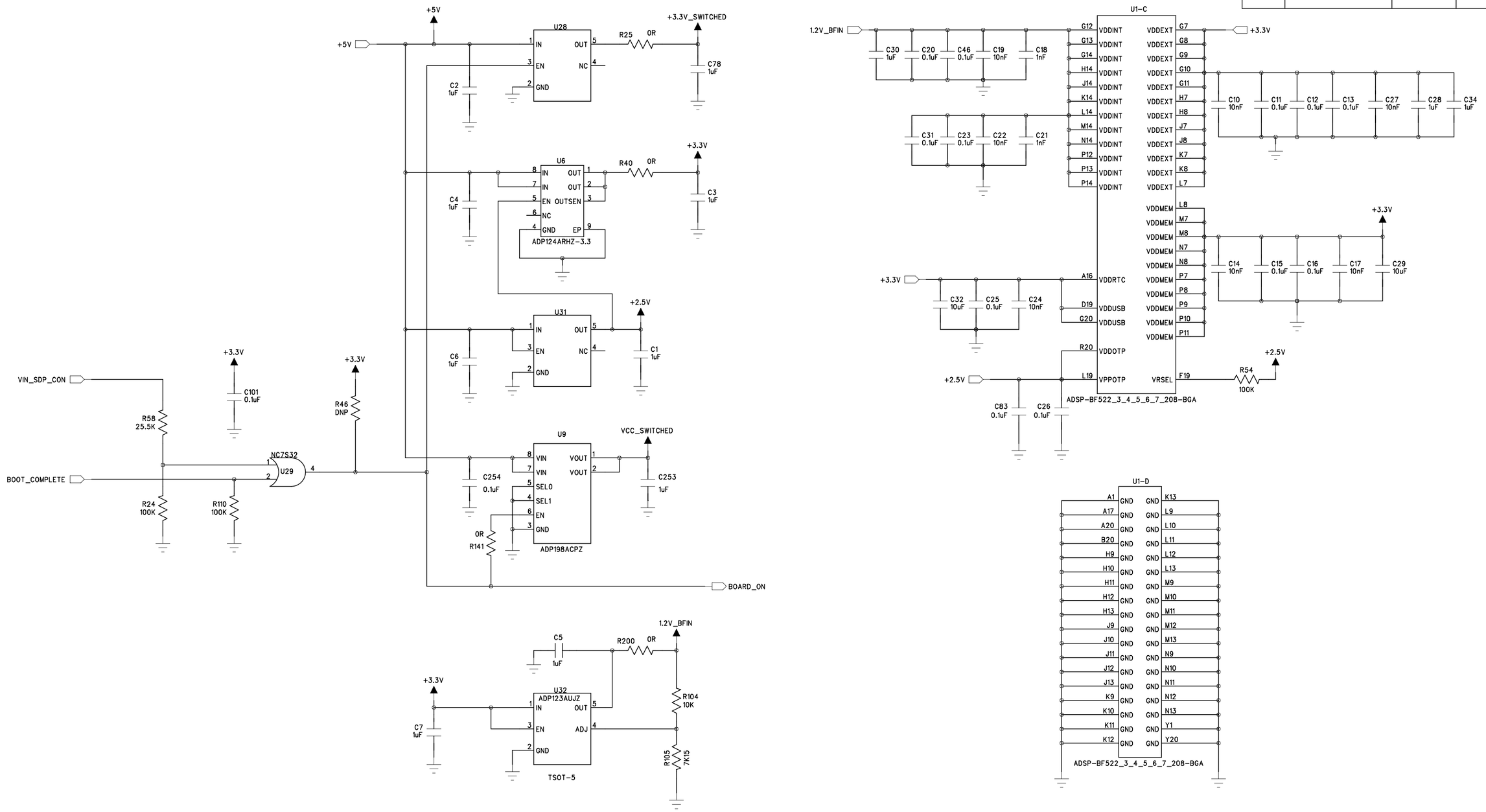

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QUALITY CONTROL:	DATED:	CODE:	SIZE: A2 / DRAWING NO: TBD SAP # / REV: 1.3
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REVISION RECORD			
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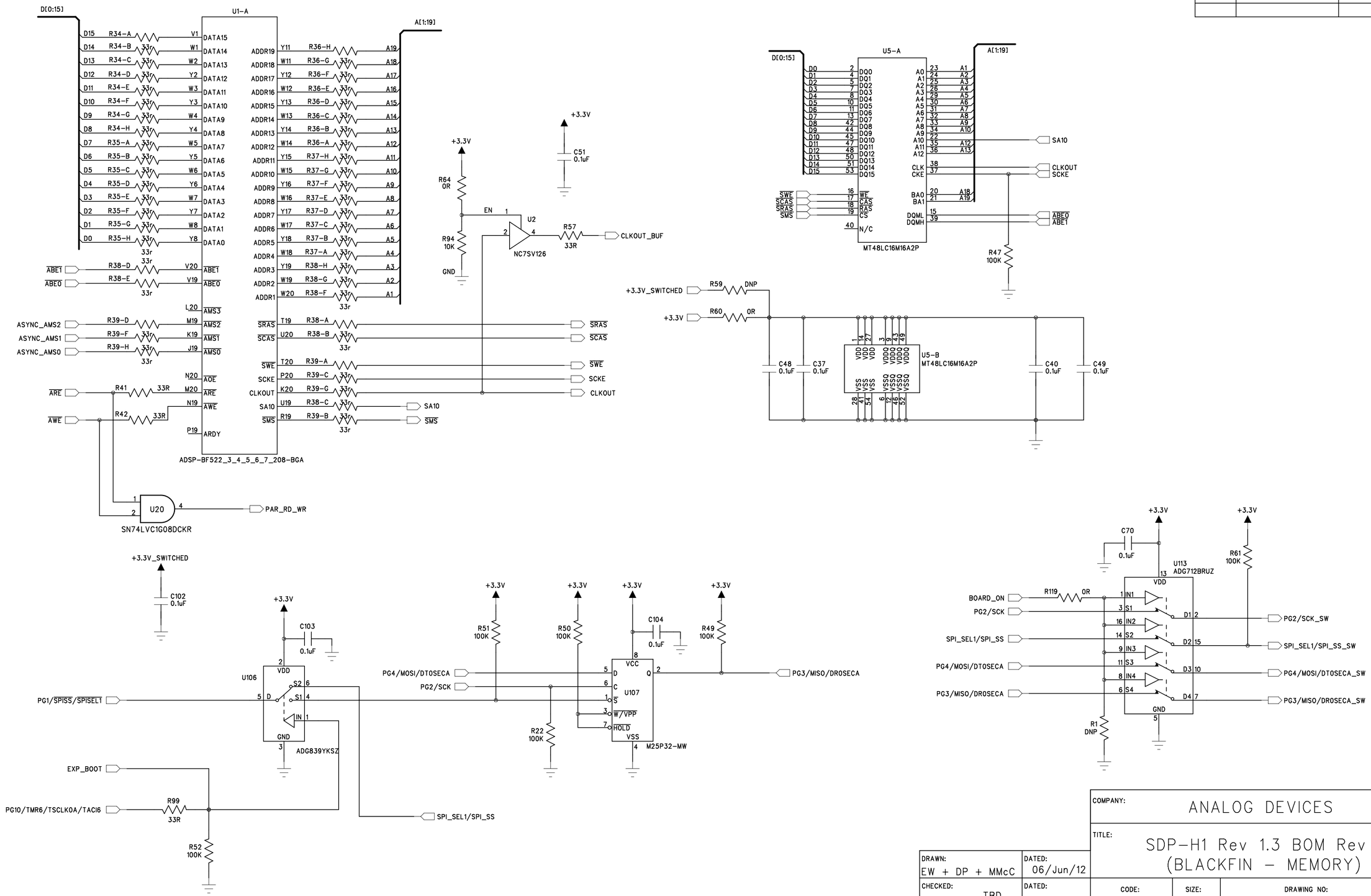

COMPANY:	ANALOG DEVICES		
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QUALITY CONTROL:	DATED:		
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REVISION RECORD			
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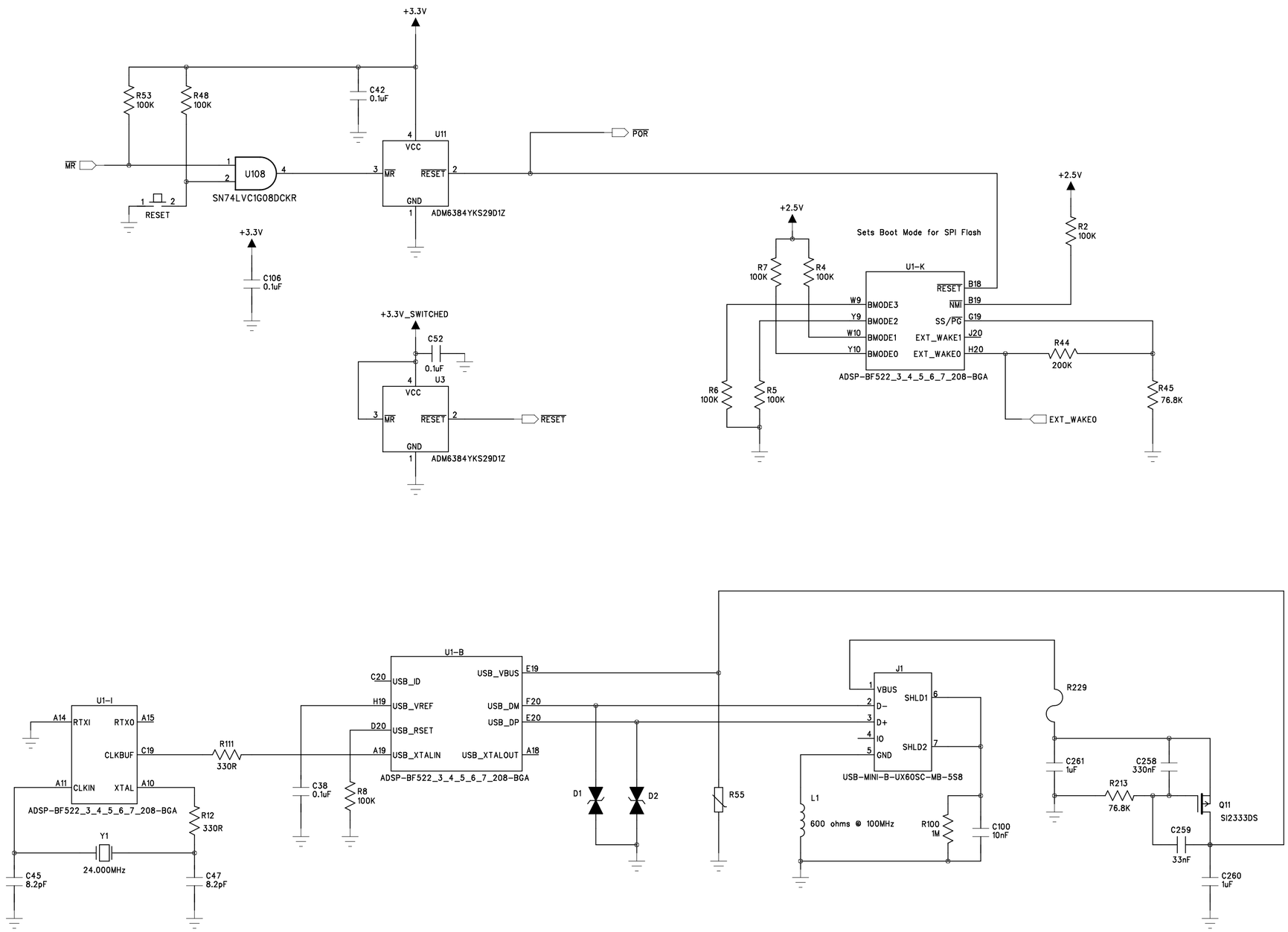

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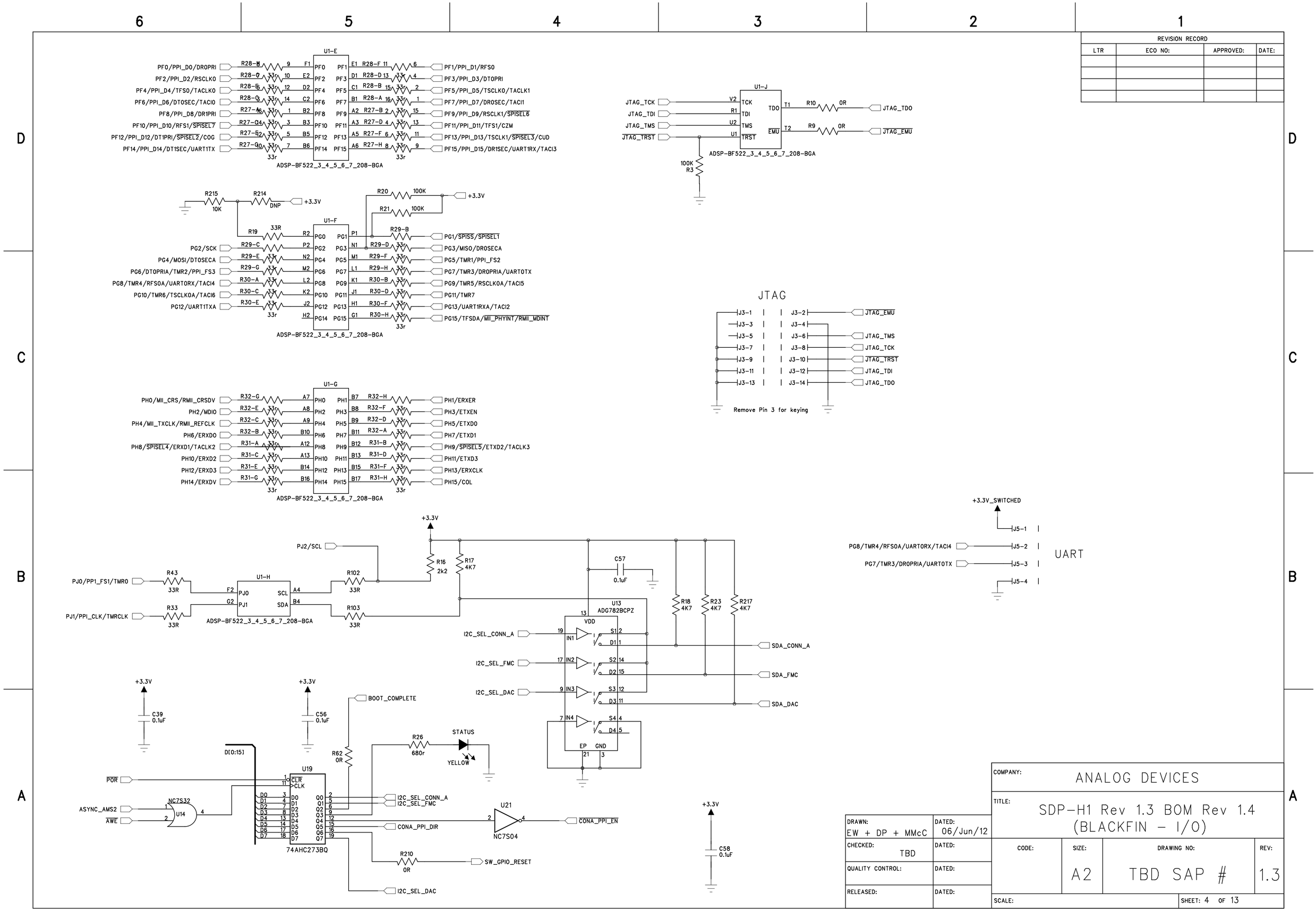

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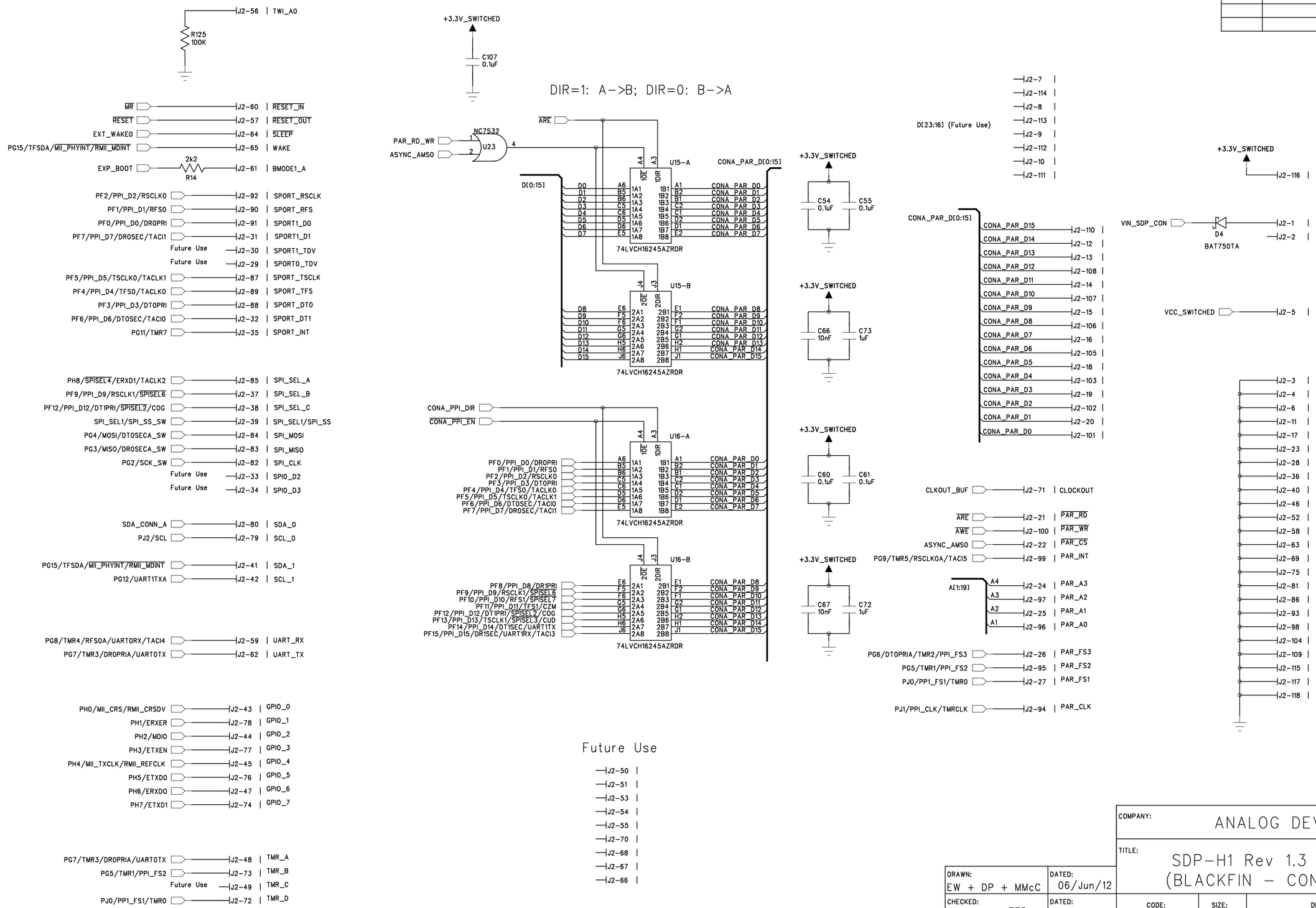

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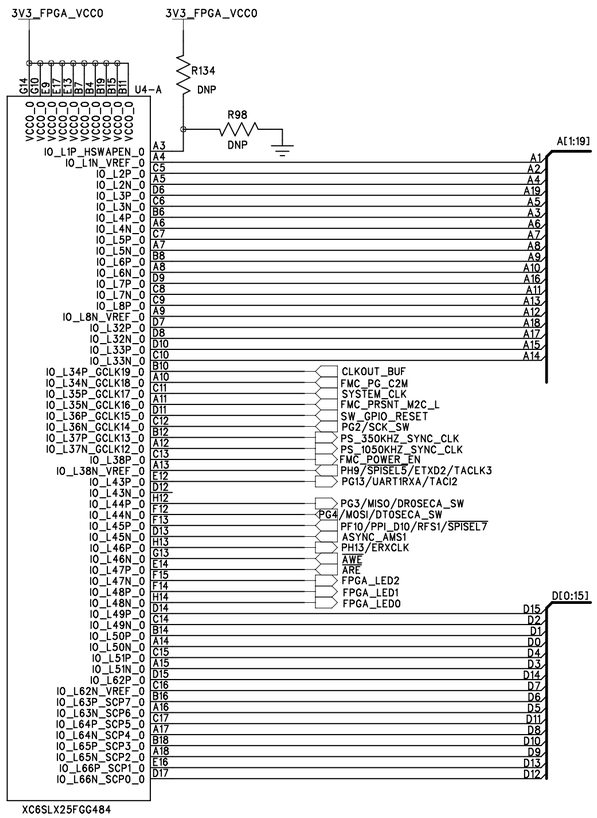

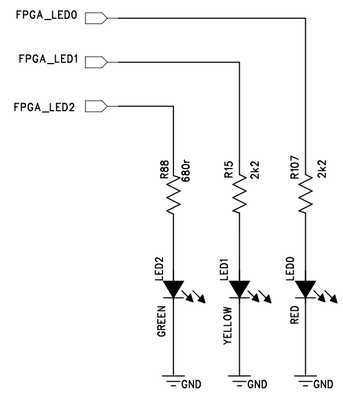

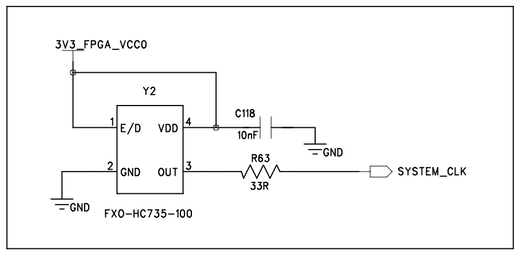

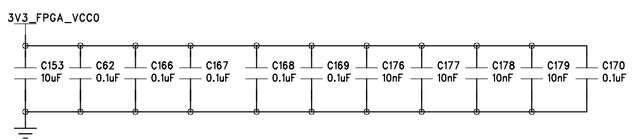

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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 6 OF 13

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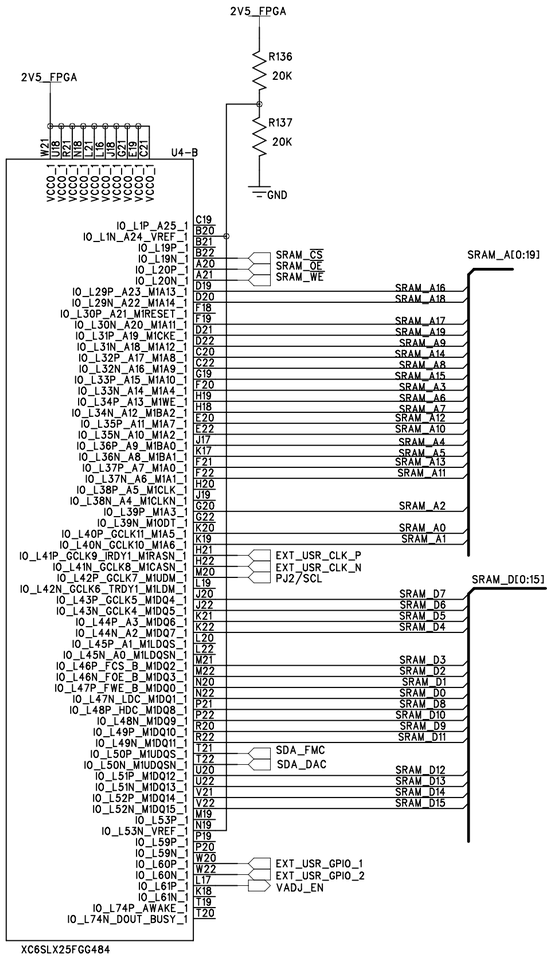
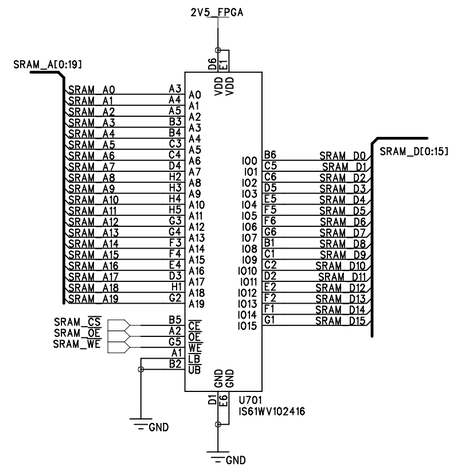
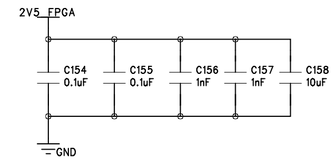
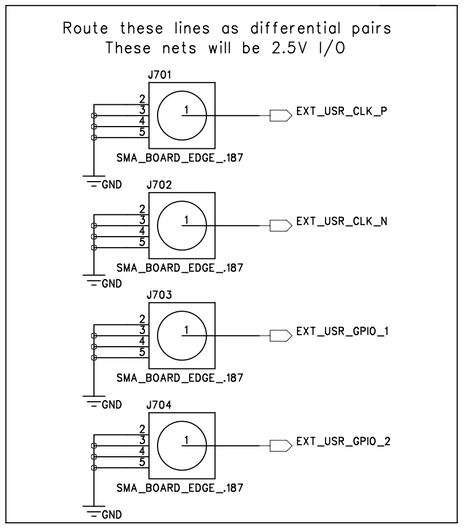




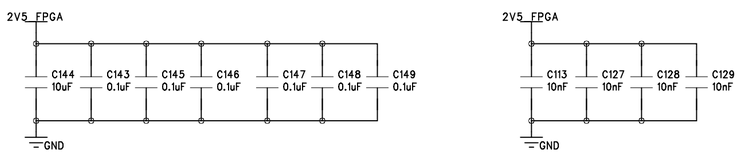
SRAM decoupling



USER SMA (DNP)



FPGA decoupling



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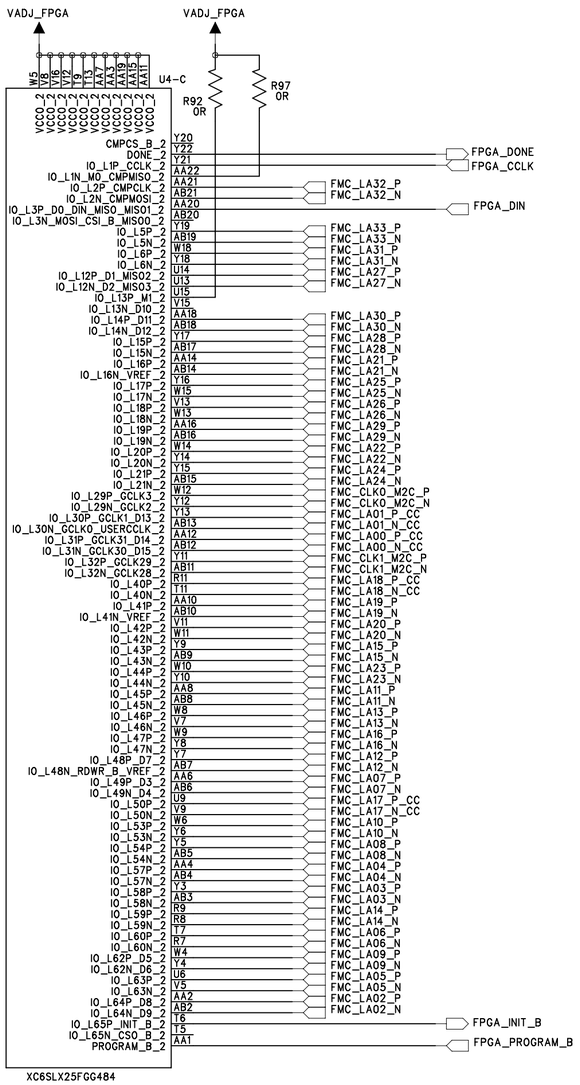
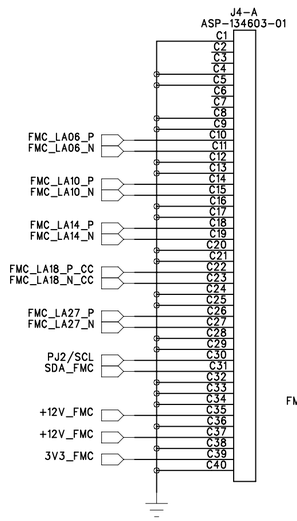
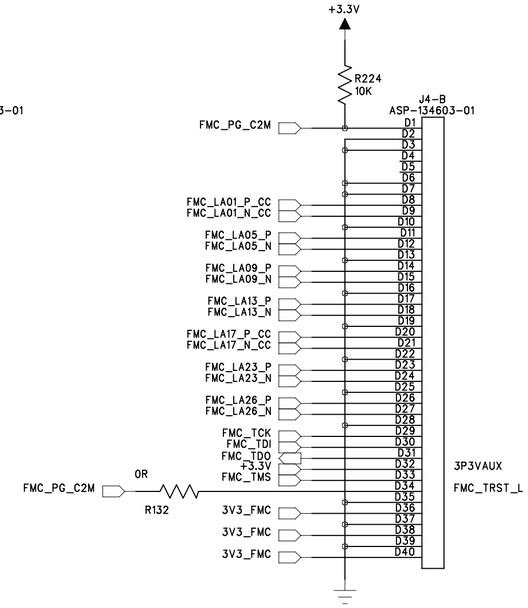
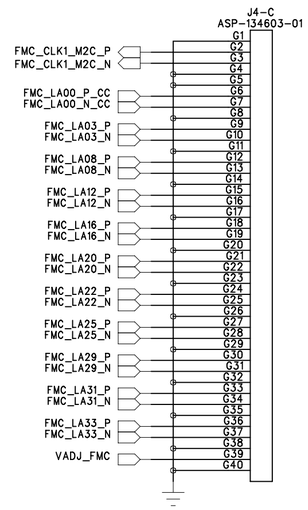
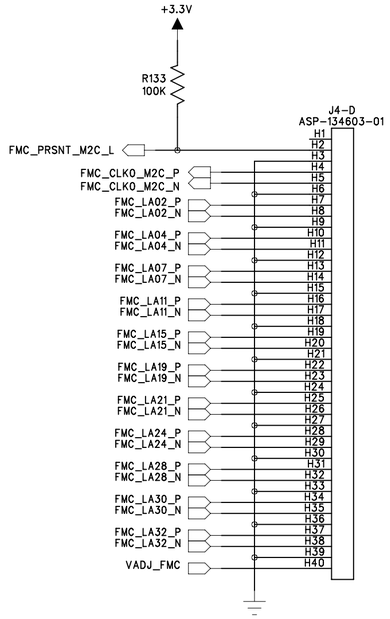
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



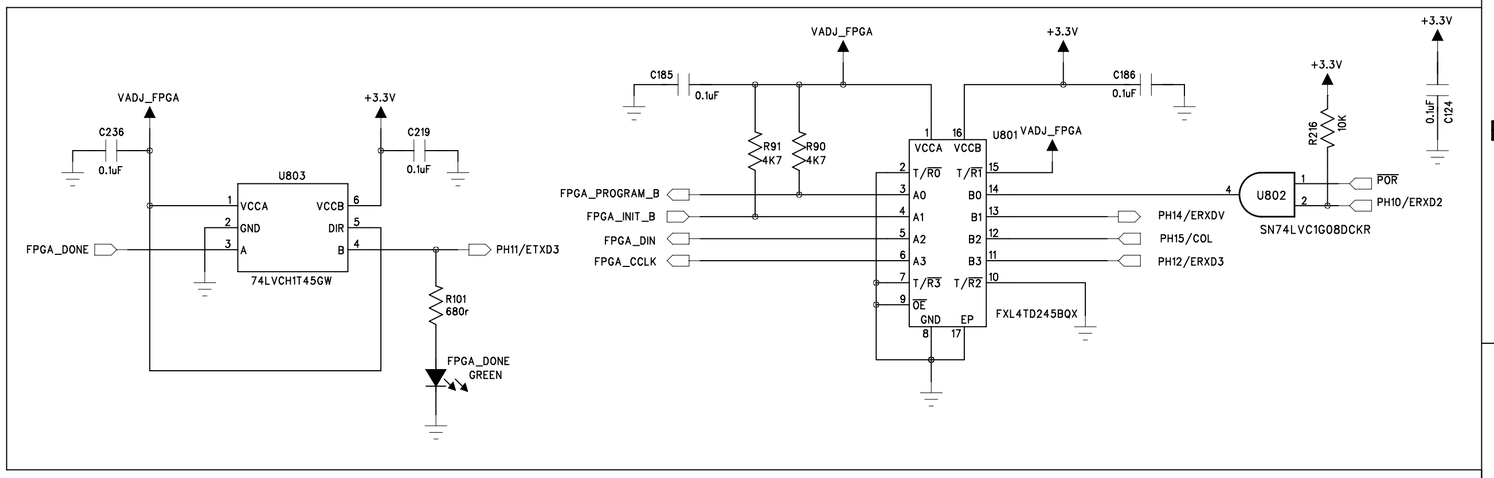




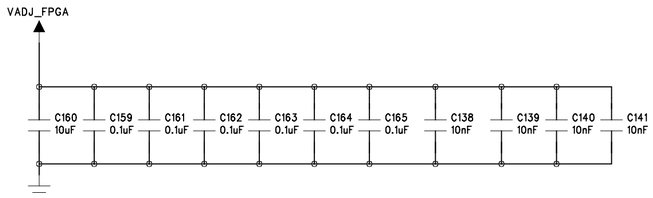




BF-FPGA Configuration Interface



FPGA decoupling



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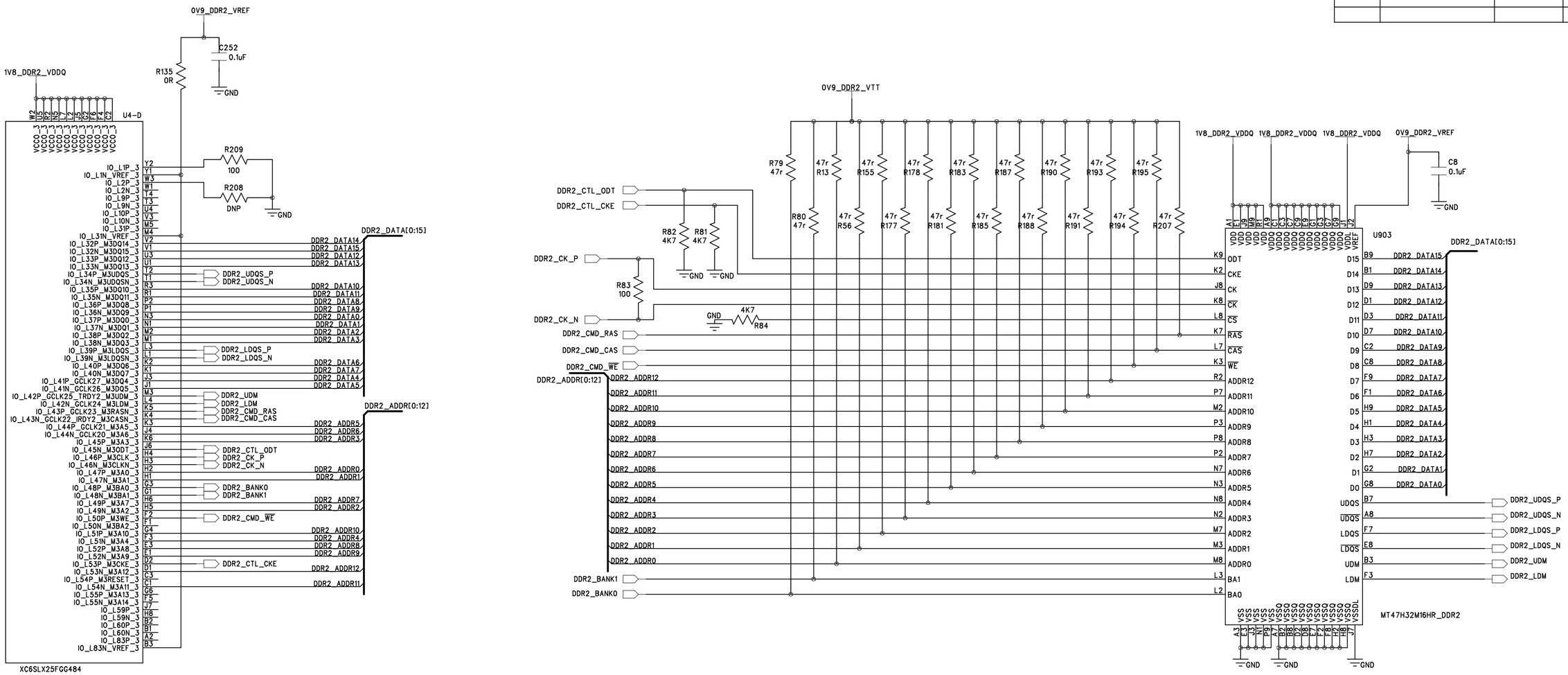
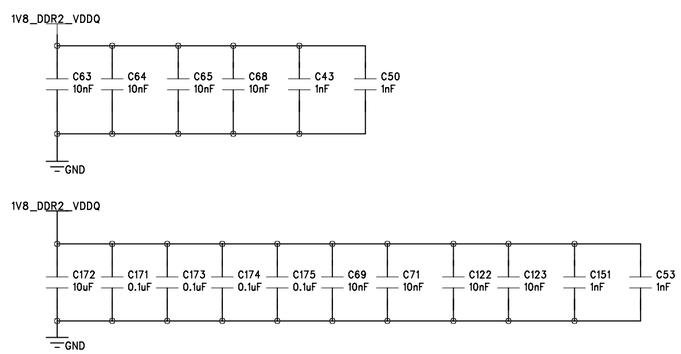
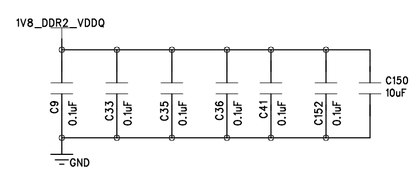


FPGA Decoupling



DDR2 Decoupling



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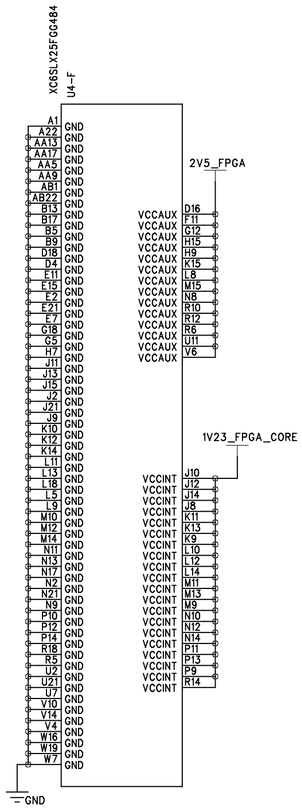
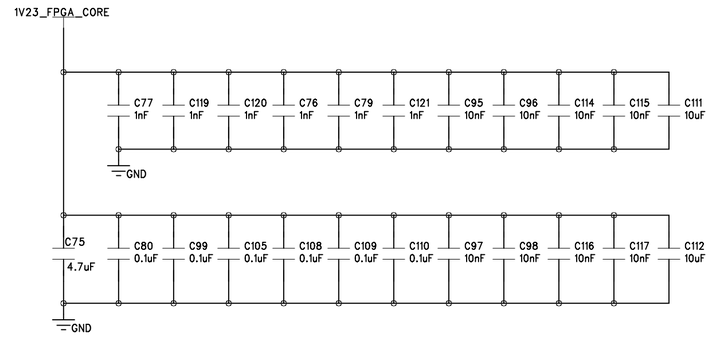
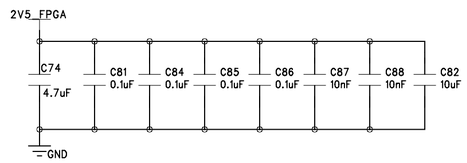
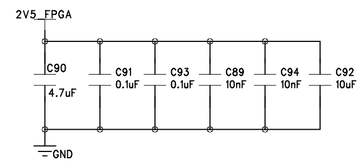


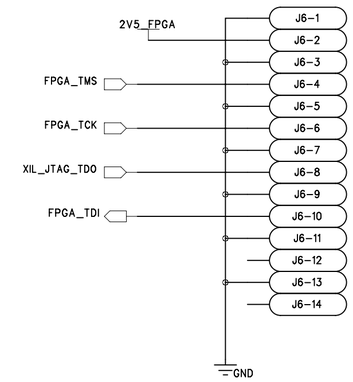


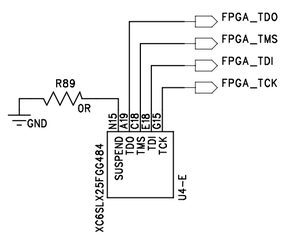


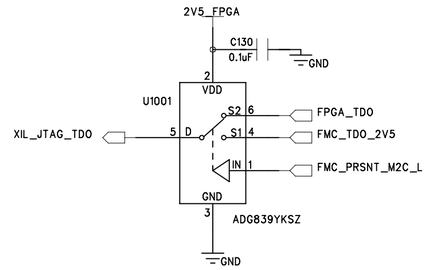


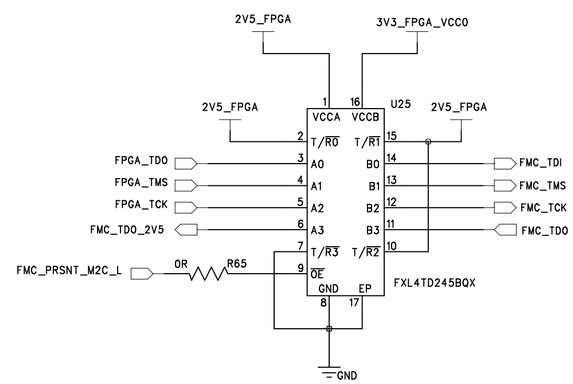
Xilinx FPGA JTAG Connector

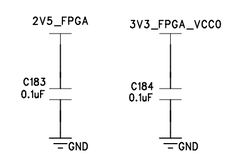
87832-1420-TB32











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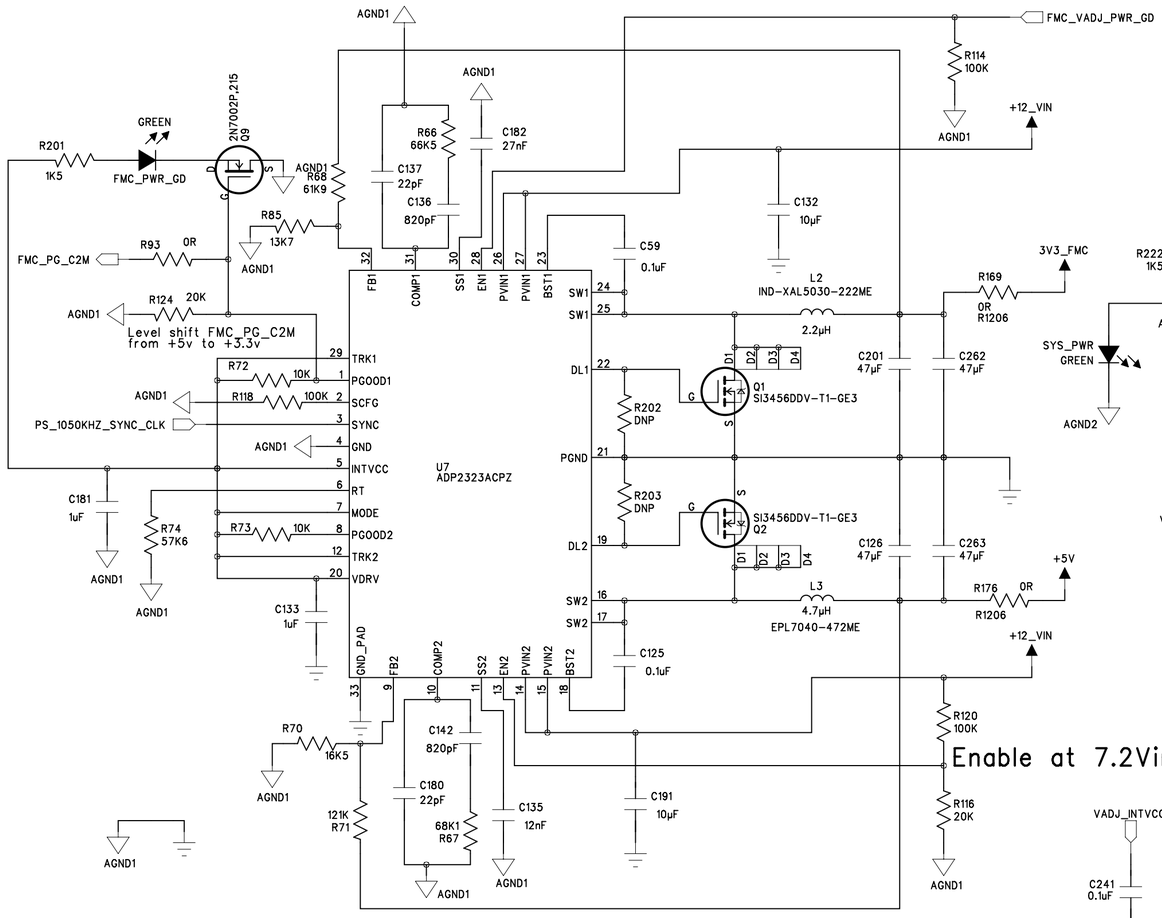
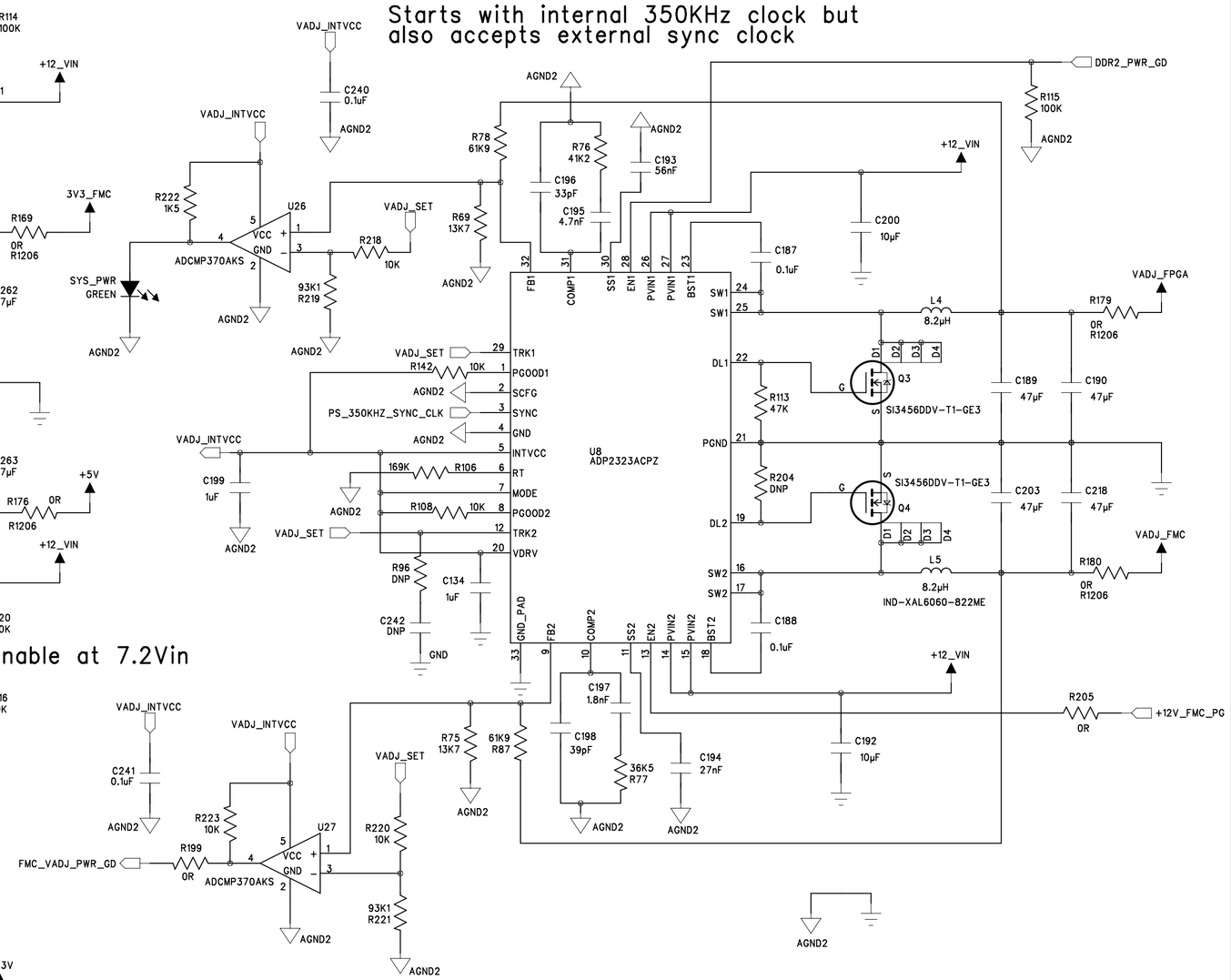
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 10 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

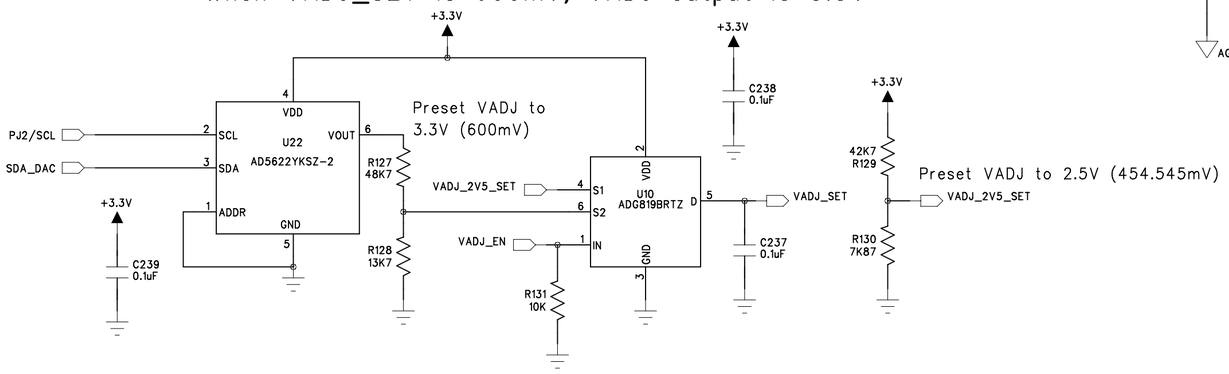
Power supply #1 for:
CH1: 12Vin. 3.3Vout 3A for FMC Conn
CH2: 12Vin. 5Vout 1.84A for Intermediate
Starts with internal 1050KHz clock but
also accepts external sync clock



Power supply #2 for:
CH1: 12Vin. VADJ 0.5A for FPGA VCC2 (1.2V, 1.8V, 2.5V, 3.3V)
CH2: 12Vin. VADJ 2A for FMC Conn (1.2V, 1.8V, 2.5V, 3.3V)
Channels track input voltage to create programmable VADJ
Starts with internal 350KHz clock but
also accepts external sync clock



For setting VADJ to 1.2V, 1.8V, 2.5V or 3.3V
When VADJ_SET is 600mV, VADJ output is 3.3V



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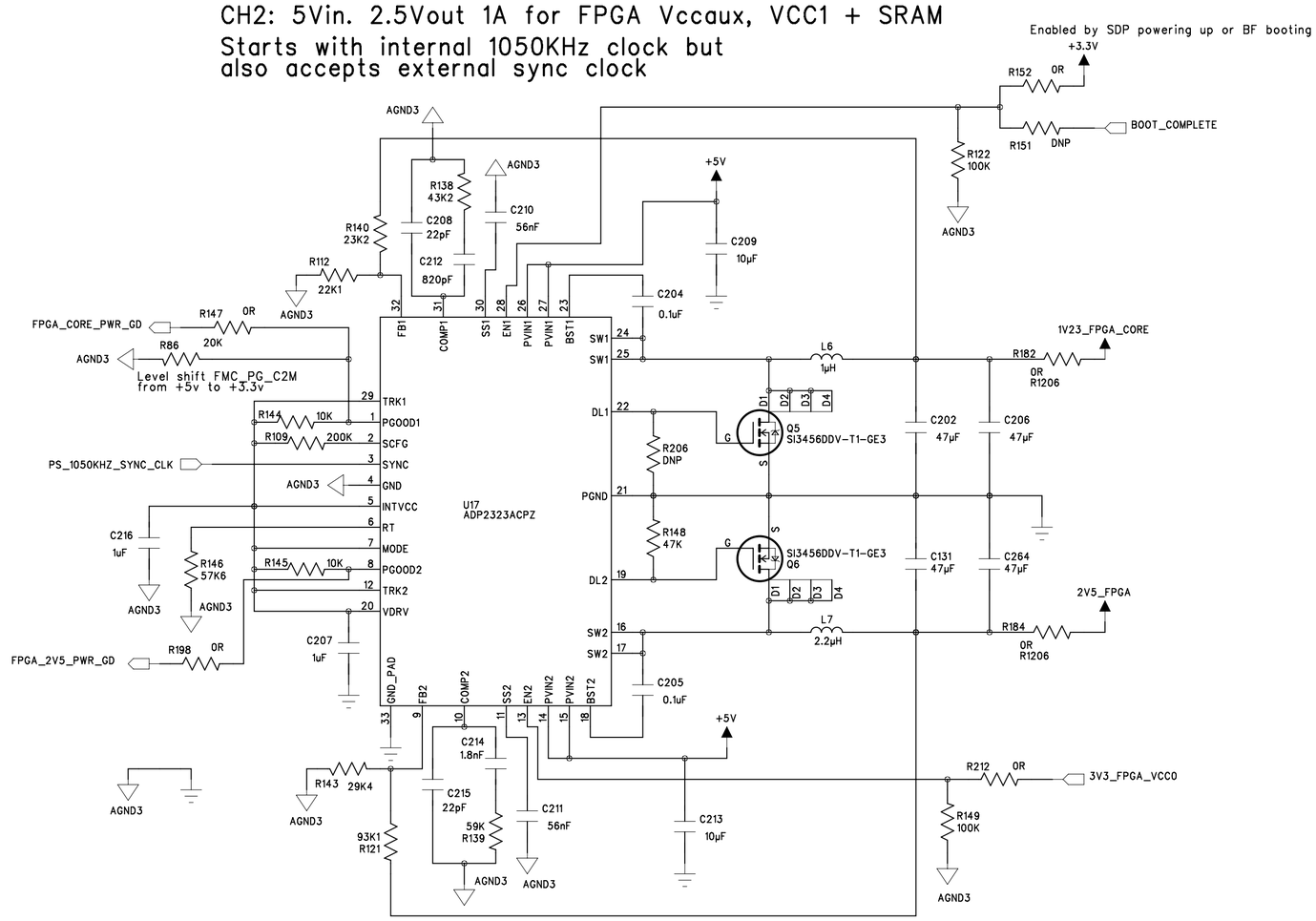
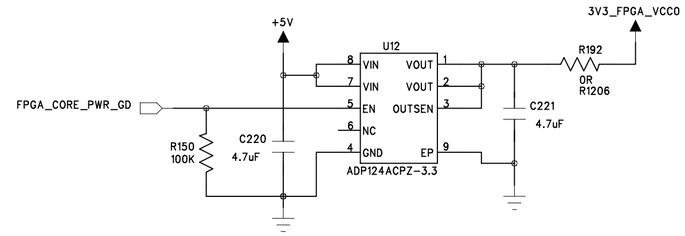
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 11 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

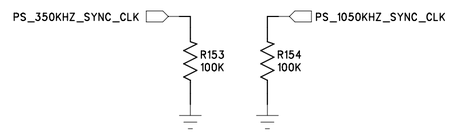
Power supply #3 for:
CH1: 5Vin. 1.23Vout 2A for FPGA core
CH2: 5Vin. 2.5Vout 1A for FPGA Vccaux, VCC1 + SRAM
Starts with internal 1050KHz clock but
also accepts external sync clock



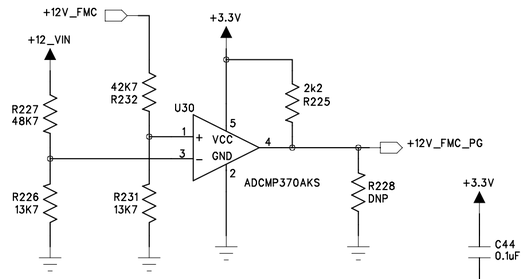
Power supply #5 for FPGA VCCO
5Vin 3.3Vout 250mA



Pull-downs to keep ADP2323 clock sync lines low while FPGA is unconfigured



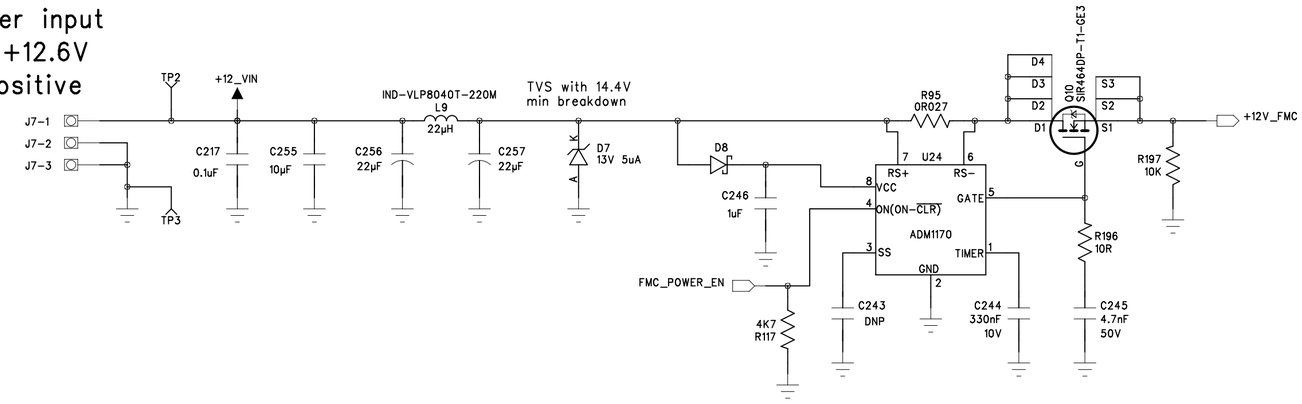
Power good circuit for detecting when switched +12V_FMC is above 10.83V



V divider values adjusted to compensate for I/P bias current of approx 71uA

Switched 12V power supply to FMC connector

Main power input
+12V to +12.6V
Centre positive



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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 12 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Switcher/LDO for DDR2 supply, termination and reference

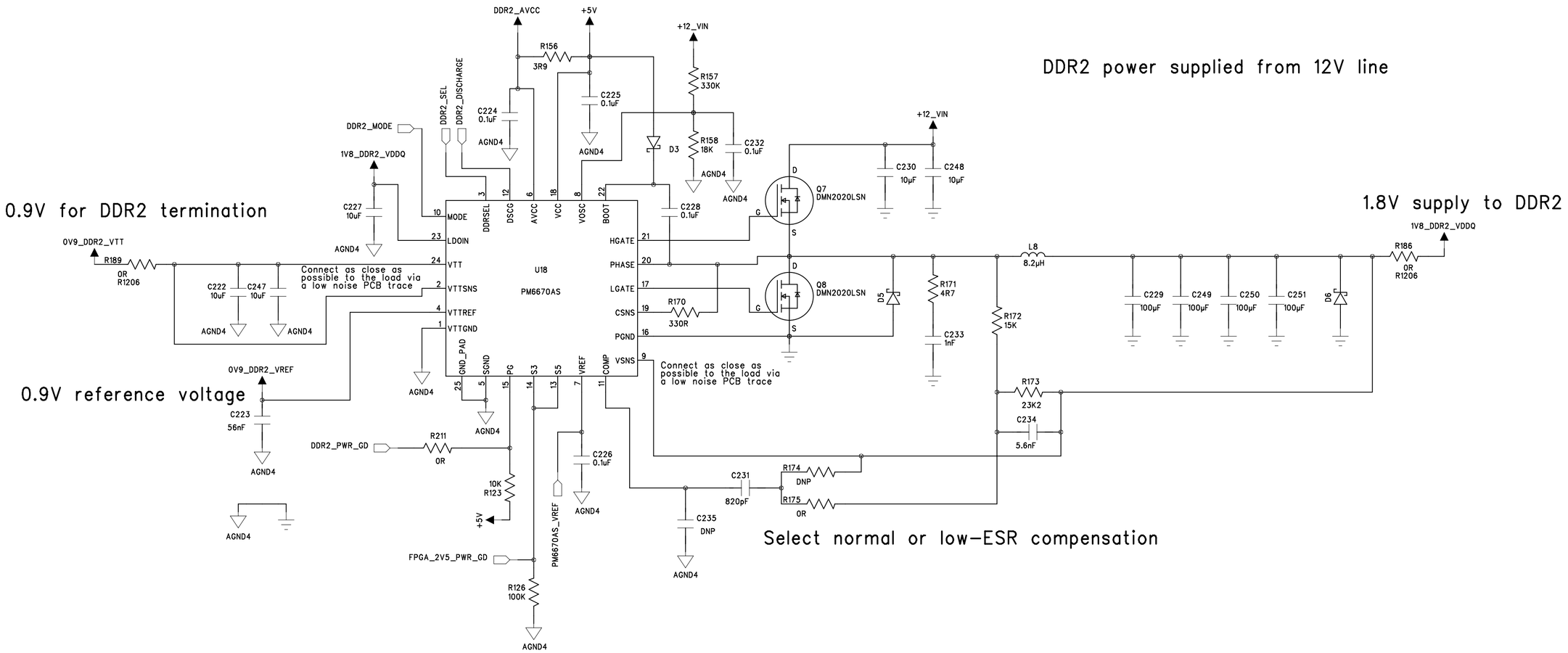
Logic supply taken from intermediate 5V

DDR2 power supplied from 12V line

0.9V for DDR2 termination

1.8V supply to DDR2

0.9V reference voltage

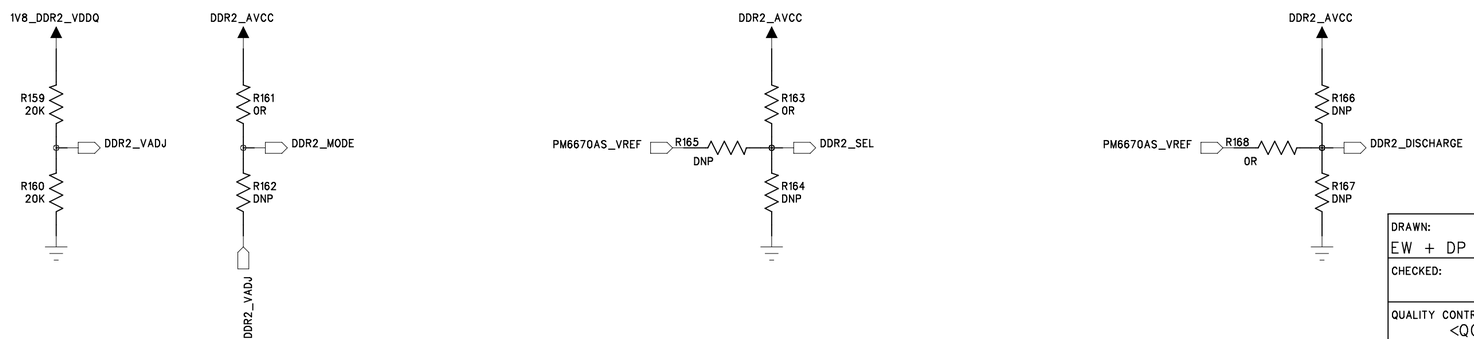


Select normal or low-ESR compensation

See table 8 of PM6670AS datasheet

See table 8 of PM6670AS datasheet

See table 9 of PM6670AS datasheet



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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 13 OF 13