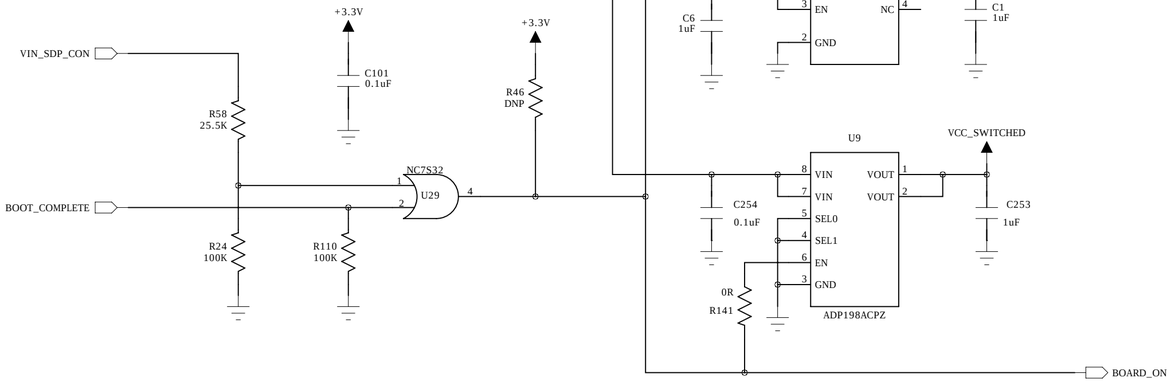
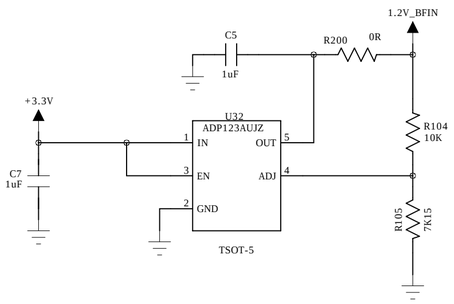
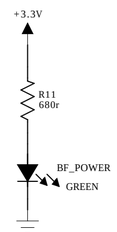
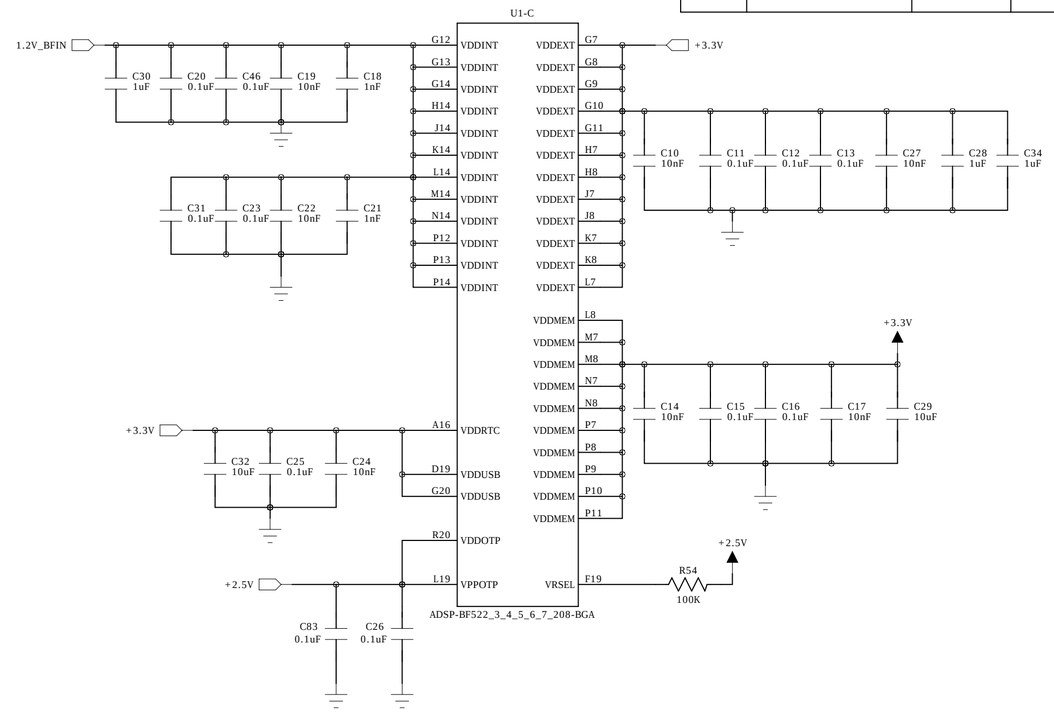
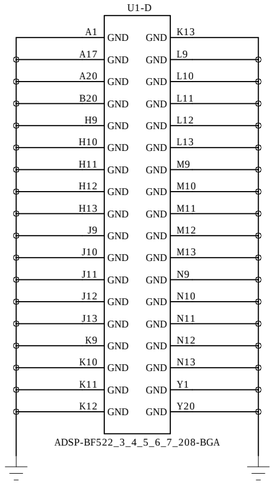
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:





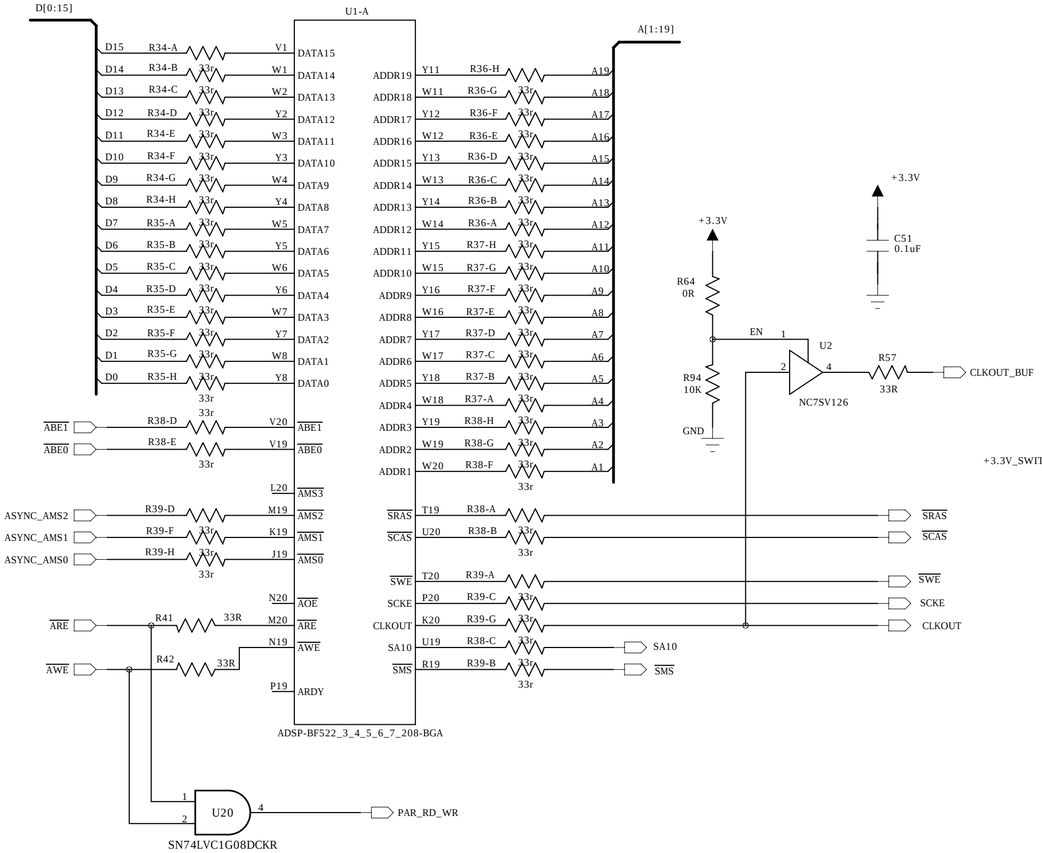


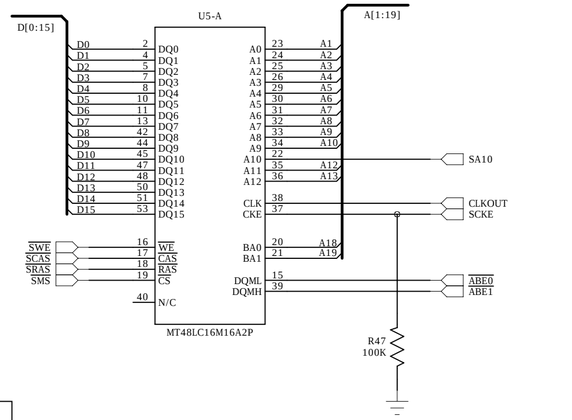


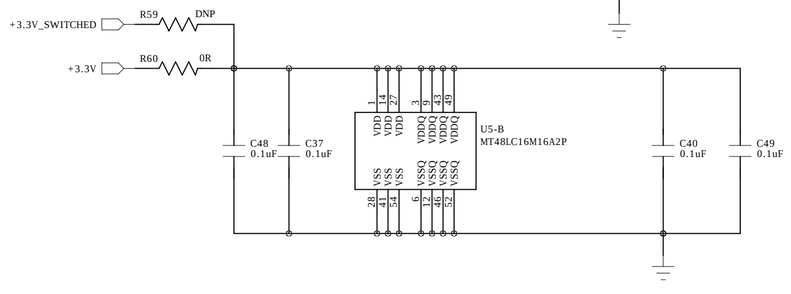


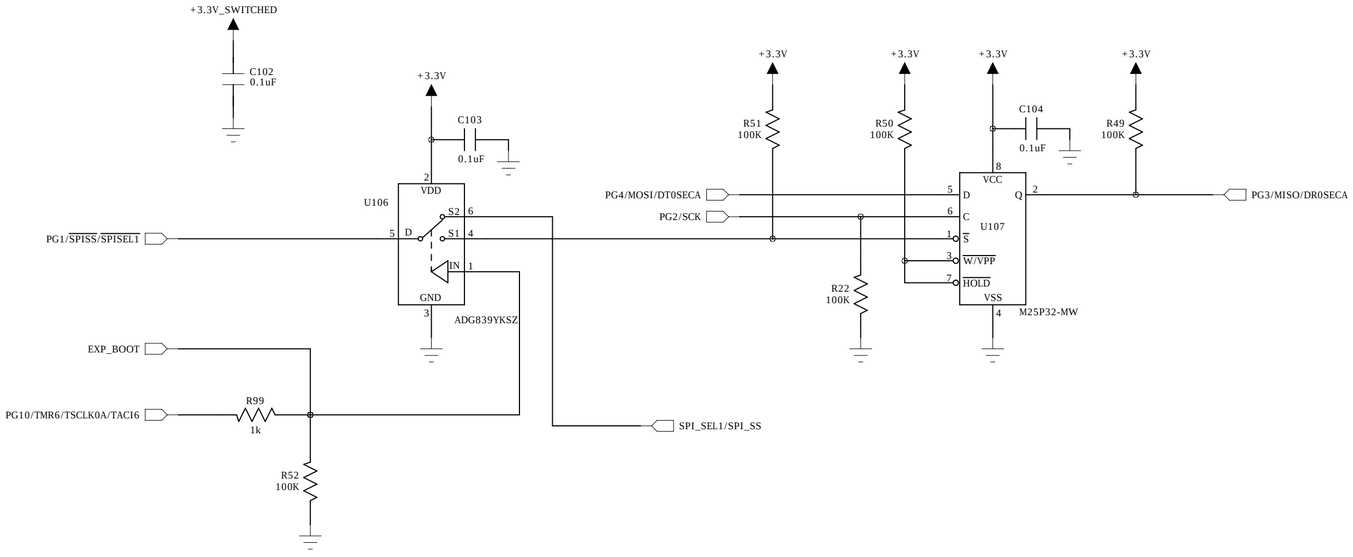
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED:	TITLE: SDP-H1 (BLACKFIN - POWER)	
QUALITY CONTROL:	DATED:	CODE:	SIZE: A2 / DRAWING NO: TBD SAP # / REV: 1.1
RELEASED:	DATED:	SCALE:	SHEET: 1 OF 13

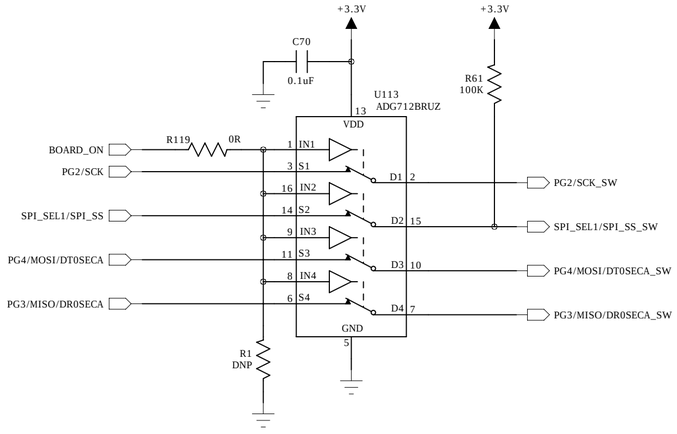
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:





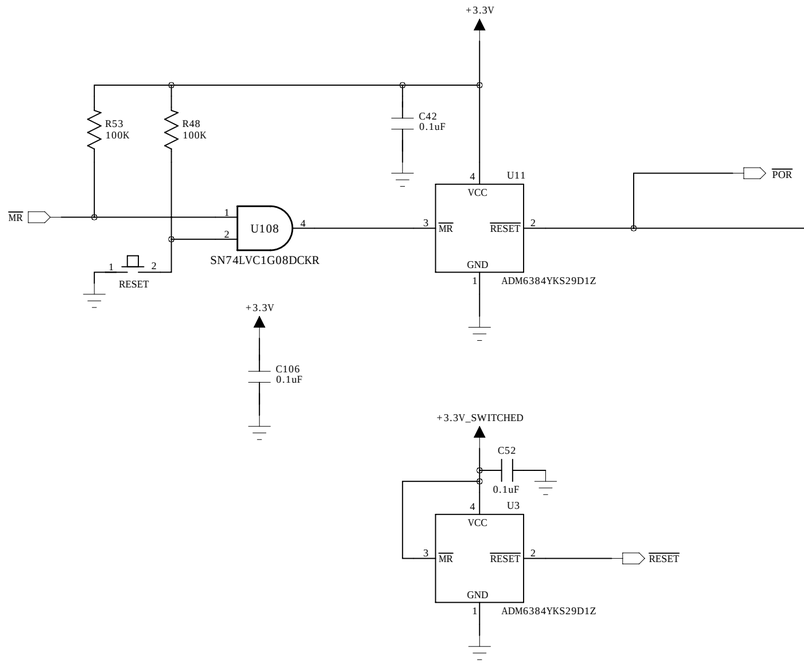


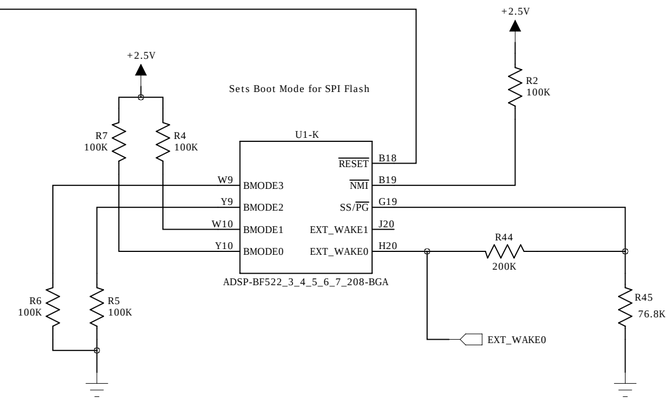


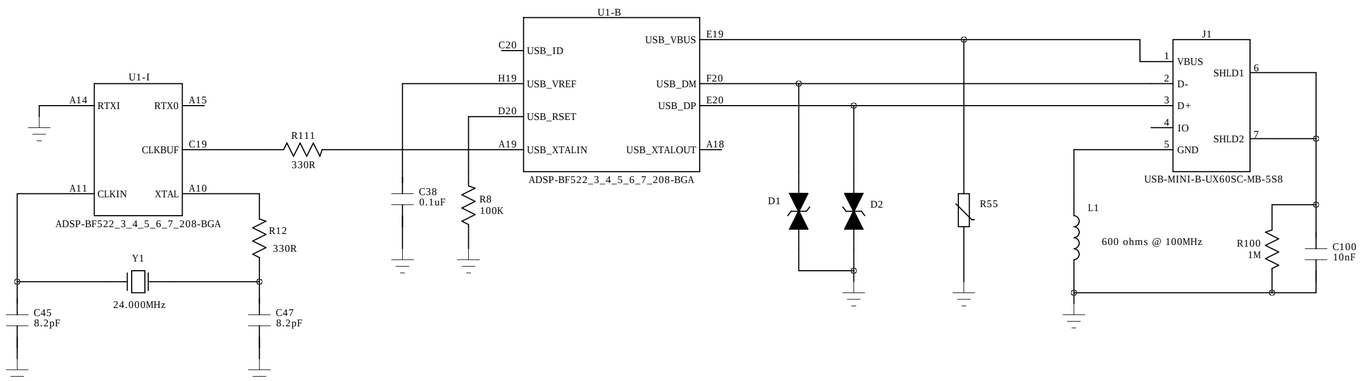


COMPANY:	ANALOG DEVICES		
TITLE:	SDP-H1 (BLACKFIN - MEMORY)		
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	CODE:	SIZE: A2
CHECKED: TBD	DATED:	DRAWING NO: TBD SAP #	REV: 1.1
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: 2 OF 13

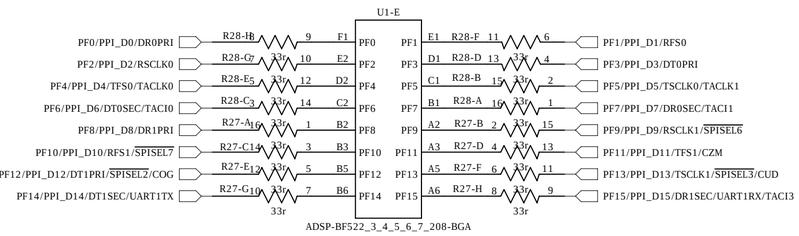
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

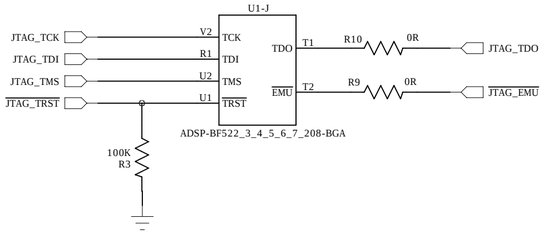


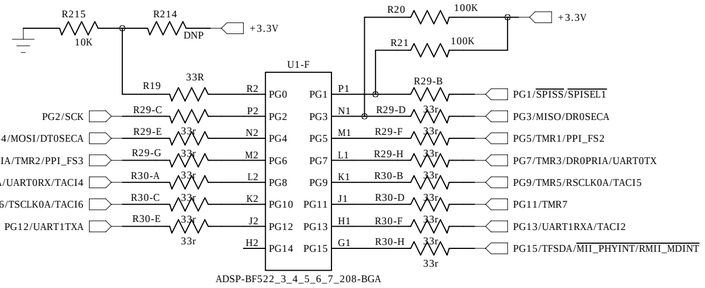


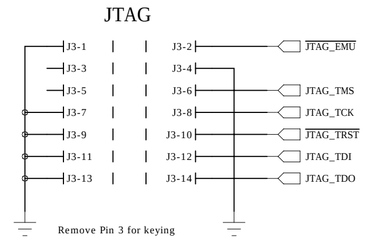


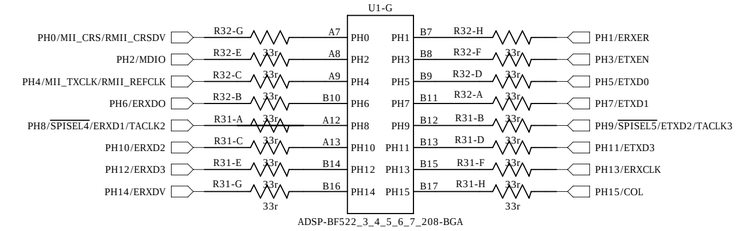
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED:	TITLE: SDP-H1 (BLACKFIN - CLOCK_USB)	
QUALITY CONTROL:	DATED:	CODE:	SIZE: A2 / DRAWING NO: TBD SAP # / REV: 1.1
RELEASED:	DATED:	SCALE:	SHEET: 3 OF 13

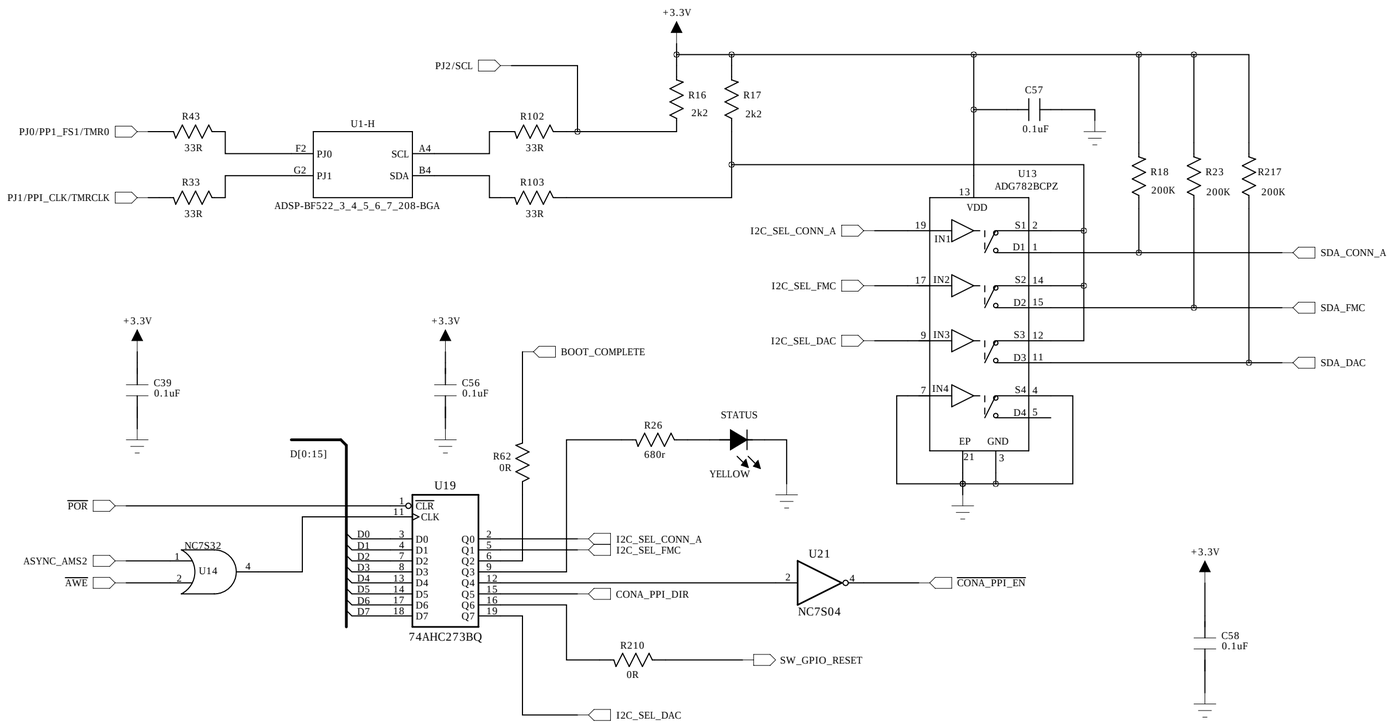


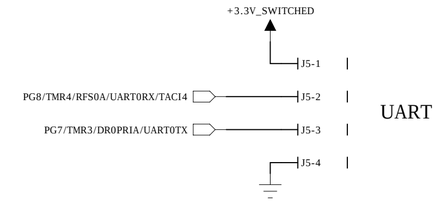












REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED:	TITLE: SDP-H1 (BLACKFIN - I/O)	
QUALITY CONTROL:	DATED:	CODE:	SIZE: A2 / DRAWING NO: TBD SAP # / REV: 1.1
RELEASED:	DATED:	SCALE:	SHEET: 4OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

R125
100K

J2-56 | TWI_A0

MR | J2-60 | RESET_IN
RESET | J2-57 | RESET_OUT
EXT_WAKE0 | J2-64 | SLEEP
PG15/TFSDA/MII_PHYINT/RMII_MDINT | J2-65 | WAKE
R14 0R
EXP_BOOT | J2-61 | BMODE1_A

PF2/PPI_D2/RSCLK0 | J2-92 | SPORT_RSCLK
PF1/PPI_D1/RFS0 | J2-90 | SPORT_RFS
PF0/PPI_D0/DR0PRI | J2-91 | SPORT1_D0
PF7/PPI_D7/DR0SEC/TACI1 | J2-31 | SPORT1_D1
Future Use | J2-30 | SPORT1_TDV
Future Use | J2-29 | SPORT0_TDV
PF5/PPI_D5/TSCLK0/TACLK1 | J2-87 | SPORT_TSCLK
PF4/PPI_D4/TFS0/TACLK0 | J2-89 | SPORT_TFS
PF3/PPI_D3/DT0PRI | J2-88 | SPORT_DT0
PF6/PPI_D6/DT0SEC/TACI0 | J2-32 | SPORT_DT1
PG11/TMR7 | J2-35 | SPORT_INT

PH8/SPISEL4/ERXD1/TACLK2 | J2-85 | SPI_SEL_A
PF9/PPI_D9/RSCLK1/SPISEL6 | J2-37 | SPI_SEL_B
PF12/PPI_D12/DT1PRI/SPISEL2/COG | J2-38 | SPI_SEL_C
SPI_SEL1/SPI_SS_SW | J2-39 | SPI_SEL1/SPI_SS
PG4/MOSI/DT0SECA_SW | J2-84 | SPI_MOSI
PG3/MISO/DR0SECA_SW | J2-83 | SPI_MISO
PG2/SCK_SW | J2-82 | SPI_CLK
Future Use | J2-33 | SPI0_D2
Future Use | J2-34 | SPI0_D3

SDA_CONN_A | J2-80 | SDA_0
PJ2/SCL | J2-79 | SCL_0

PG15/TFSDA/MII_PHYINT/RMII_MDINT | J2-41 | SDA_1
PG12/UART1TXA | J2-42 | SCL_1

PG8/TMR4/RFS0A/UART0RX/TACI4 | J2-59 | UART_RX
PG7/TMR3/DR0PRIA/UART0TX | J2-62 | UART_TX

PH0/MII_CRS/RMII_CRSDV | J2-43 | GPIO_0
PH1/ERXER | J2-78 | GPIO_1
PH2/MDIO | J2-44 | GPIO_2
PH3/ETXEN | J2-77 | GPIO_3
PH4/MII_TXCLK/RMII_REFCLK | J2-45 | GPIO_4
PH5/ETXD0 | J2-76 | GPIO_5
PH6/ERXDO | J2-47 | GPIO_6
PH7/ETXD1 | J2-74 | GPIO_7

PG7/TMR3/DR0PRIA/UART0TX | J2-48 | TMR_A
PG5/TMR1/PPI_FS2 | J2-73 | TMR_B
Future Use | J2-49 | TMR_C
PJ0/PP1_FS1/TMR0 | J2-72 | TMR_D

+3.3V_SWITCHED
C107
0.1uF

DIR=1: A->B; DIR=0: B->A

ARE
PAR_RD_WR
ASYNC_AMS0
NC7S32
U23

U15-A
D[0:15]
CONA_PAR_D[0:15]
1OE 1DIR
D0 A6 1A1 1B1 A1 CONA_PAR_D0
D1 B5 1A2 1B2 B2 CONA_PAR_D1
D2 B6 1A3 1B3 B1 CONA_PAR_D2
D3 C5 1A4 1B4 C2 CONA_PAR_D3
D4 C6 1A5 1B5 C1 CONA_PAR_D4
D5 D5 1A6 1B6 D2 CONA_PAR_D5
D6 D6 1A7 1B7 D1 CONA_PAR_D6
D7 E5 1A8 1B8 E2 CONA_PAR_D7
74LVCH16245AZRDR

U15-B
2OE 2DIR
D8 E6 2A1 2B1 E1 CONA_PAR_D8
D9 F5 2A2 2B2 F2 CONA_PAR_D9
D10 F6 2A3 2B3 F1 CONA_PAR_D10
D11 G5 2A4 2B4 G2 CONA_PAR_D11
D12 G6 2A5 2B5 G1 CONA_PAR_D12
D13 H5 2A6 2B6 H2 CONA_PAR_D13
D14 H6 2A7 2B7 H1 CONA_PAR_D14
D15 J6 2A8 2B8 J1 CONA_PAR_D15
74LVCH16245AZRDR

+3.3V_SWITCHED
C54 0.1uF
C55 0.1uF
+3.3V_SWITCHED
C66 10nF
C73 1uF

CONA_PPI_DIR
CONA_PPI_EN

U16-A
PF0/PPI_D0/DR0PRI
PF1/PPI_D1/RFS0
PF2/PPI_D2/RSCLK0
PF3/PPI_D3/DT0PRI
PF4/PPI_D4/TFS0/TACLK0
PF5/PPI_D5/TSCLK0/TACLK1
PF6/PPI_D6/DT0SEC/TACI0
PF7/PPI_D7/DR0SEC/TACI1
CONA_PAR_D0 … CONA_PAR_D7
74LVCH16245AZRDR

U16-B
PF8/PPI_D8/DR1PRI
PF9/PPI_D9/RSCLK1/SPISEL6
PF10/PPI_D10/RFS1/SPISEL7
PF11/PPI_D11/TFS1/CZM
PF12/PPI_D12/DT1PRI/SPISEL2/COG
PF13/PPI_D13/TSCLK1/SPISEL3/CUD
PF14/PPI_D14/DT1SEC/UART1TX
PF15/PPI_D15/DR1SEC/UART1RX/TACI3
CONA_PAR_D8 … CONA_PAR_D15
74LVCH16245AZRDR

+3.3V_SWITCHED
C60 0.1uF
C61 0.1uF
+3.3V_SWITCHED
C67 10nF
C72 1uF

Future Use
J2-50
J2-51
J2-53
J2-54
J2-55
J2-70
J2-68
J2-67
J2-66

D[23:16] (Future Use)
J2-7
J2-114
J2-8
J2-113
J2-9
J2-112
J2-10
J2-111

CONA_PAR_D[0:15]
CONA_PAR_D15 | J2-110
CONA_PAR_D14 | J2-12
CONA_PAR_D13 | J2-13
CONA_PAR_D12 | J2-108
CONA_PAR_D11 | J2-14
CONA_PAR_D10 | J2-107
CONA_PAR_D9 | J2-15
CONA_PAR_D8 | J2-106
CONA_PAR_D7 | J2-16
CONA_PAR_D6 | J2-105
CONA_PAR_D5 | J2-18
CONA_PAR_D4 | J2-103
CONA_PAR_D3 | J2-19
CONA_PAR_D2 | J2-102
CONA_PAR_D1 | J2-20
CONA_PAR_D0 | J2-101

CLKOUT_BUF | J2-71 | CLOCKOUT
ARE | J2-21 | PAR_RD
AWE | J2-100 | PAR_WR
ASYNC_AMS0 | J2-22 | PAR_CS
PG9/TMR5/RSCLK0A/TACI5 | J2-99 | PAR_INT
A[1:19]
A4 | J2-24 | PAR_A3
A3 | J2-97 | PAR_A2
A2 | J2-25 | PAR_A1
A1 | J2-96 | PAR_A0
PG6/DT0PR1A/TMR2/PPI_FS3 | J2-26 | PAR_FS3
PG5/TMR1/PPI_FS2 | J2-95 | PAR_FS2
PJ0/PP1_FS1/TMR0 | J2-27 | PAR_FS1
PJ1/PPI_CLK/TMRCLK | J2-94 | PAR_CLK

+3.3V_SWITCHED
J2-116
VIN_SDP_CON | J2-1
D4 BAT750TA
J2-2
VCC_SWITCHED | J2-5

J2-3
J2-4
J2-6
J2-11
J2-17
J2-23
J2-28
J2-36
J2-40
J2-46
J2-52
J2-58
J2-63
J2-69
J2-75
J2-81
J2-86
J2-93
J2-98
J2-104
J2-109
J2-115
J2-117
J2-118

DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	
CHECKED: TBD	DATED:	
QUALITY CONTROL:	DATED:	
RELEASED:	DATED:	

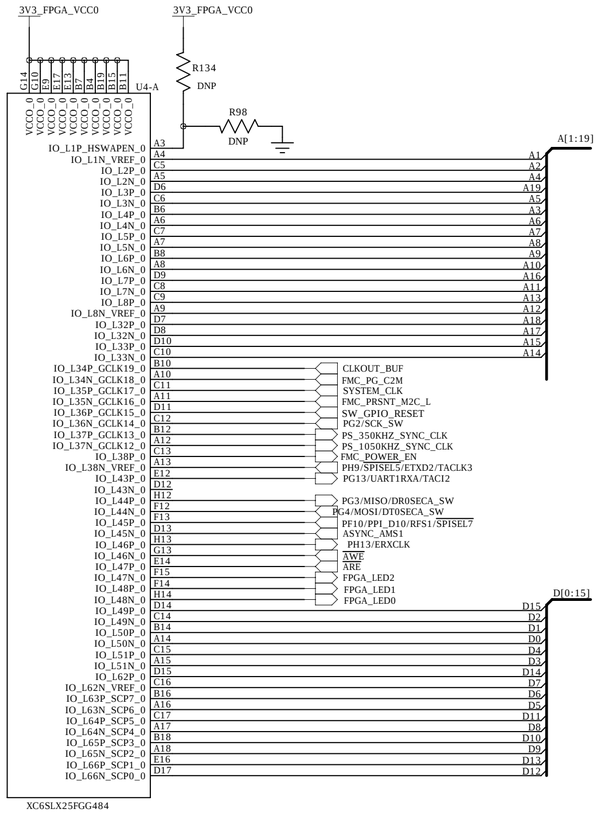
COMPANY: ANALOG DEVICES

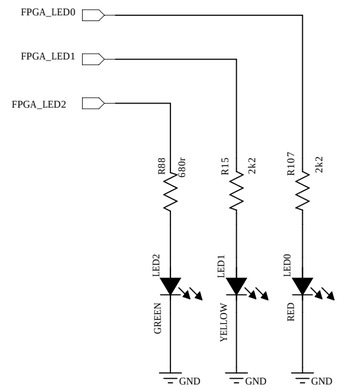
TITLE: SDP-H1 (BLACKFIN - CONNECTOR A)

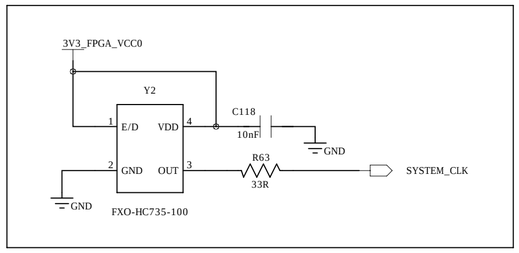
CODE:	SIZE:	DRAWING NO:	REV:
	A2	TBD SAP #	1.1

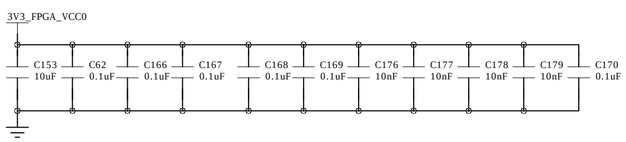
SCALE: | SHEET: 5 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



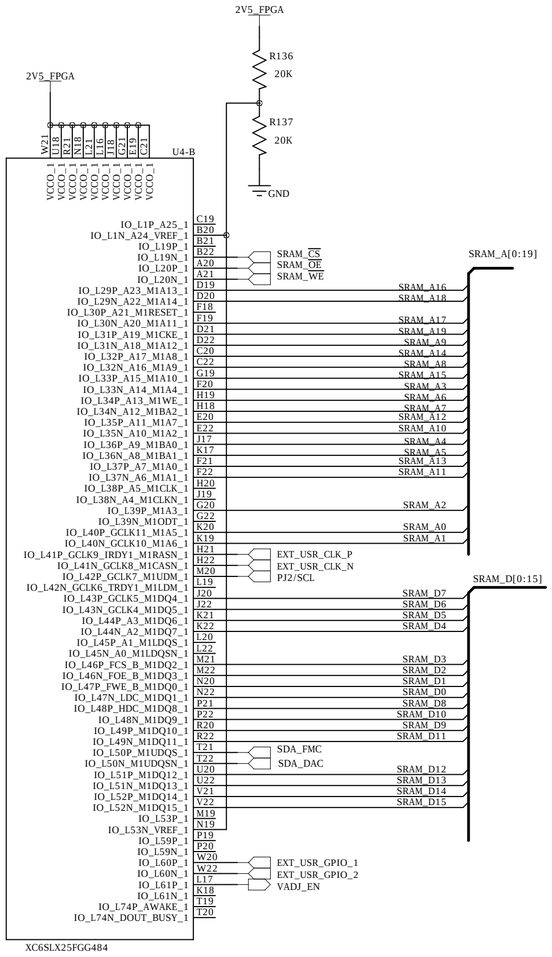


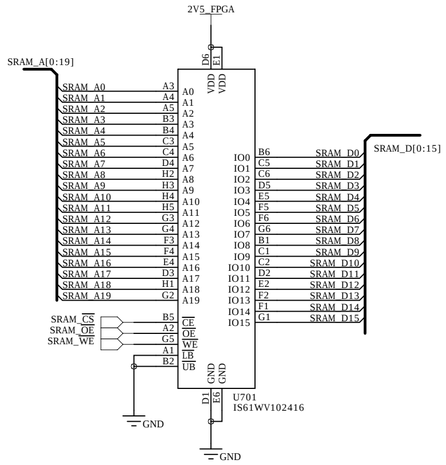




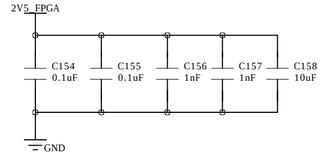
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED: <Checked Date>	TITLE: SDP-H1 (FPGA BANK 0 - BLACKFIN)	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: TBD SAP #	REV: 1.1
		SCALE: <Scale>	SHEET: 6 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



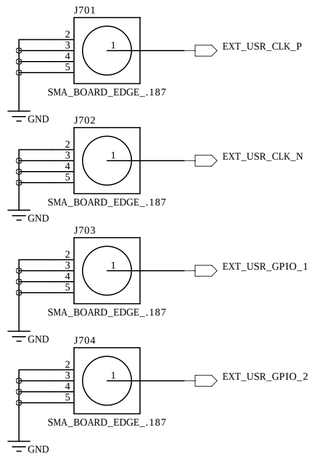


SRAM decoupling

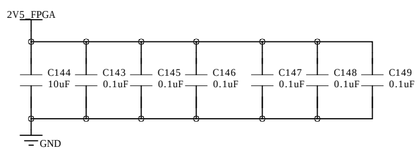


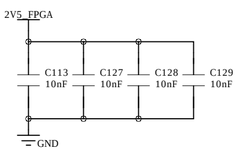
USER SMA (DNP)

Route these lines as differential pairs
These nets will be 2.5V I/O



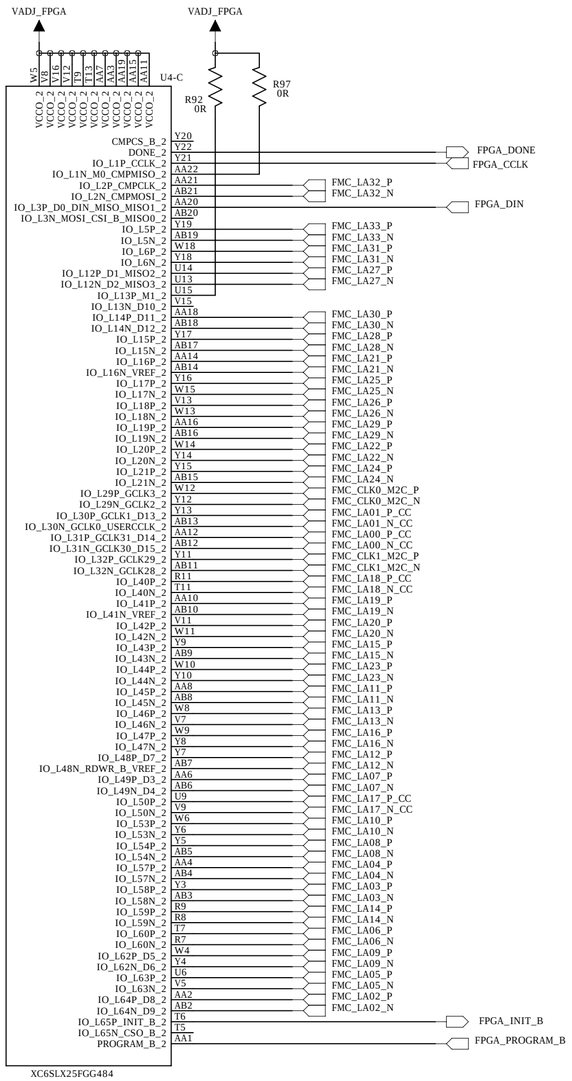
FPGA decoupling

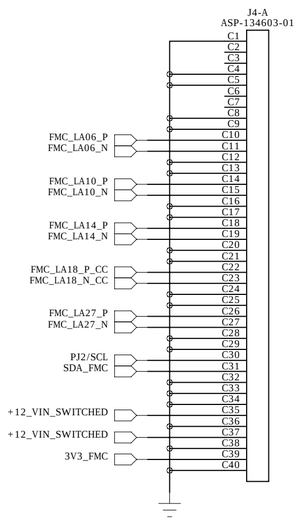


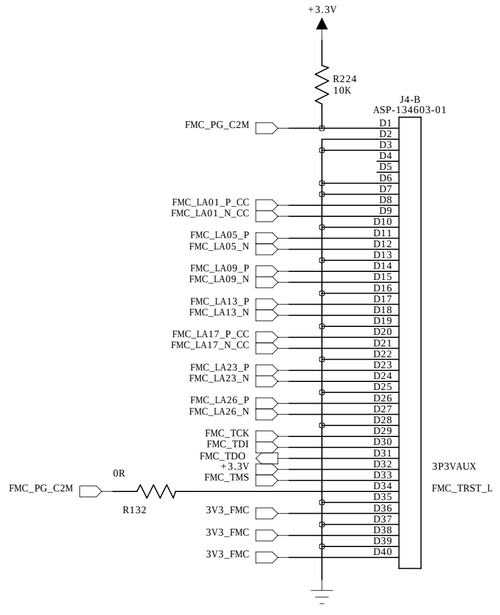


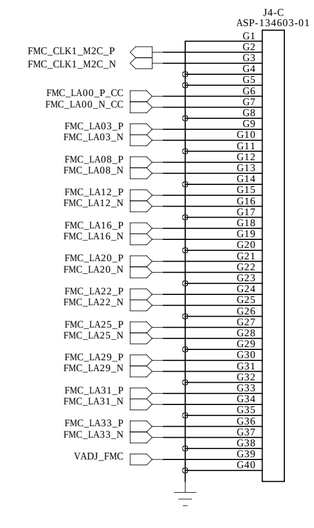
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED: <Checked Date>	TITLE: SDP-H1 (FPGA BANK 1 - SRAM)	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: TBD SAP #	REV: 1.1
		SCALE: <Scale>	SHEET: 7 OF 13

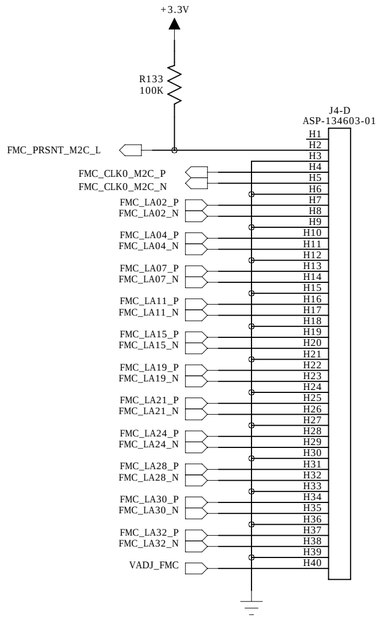
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



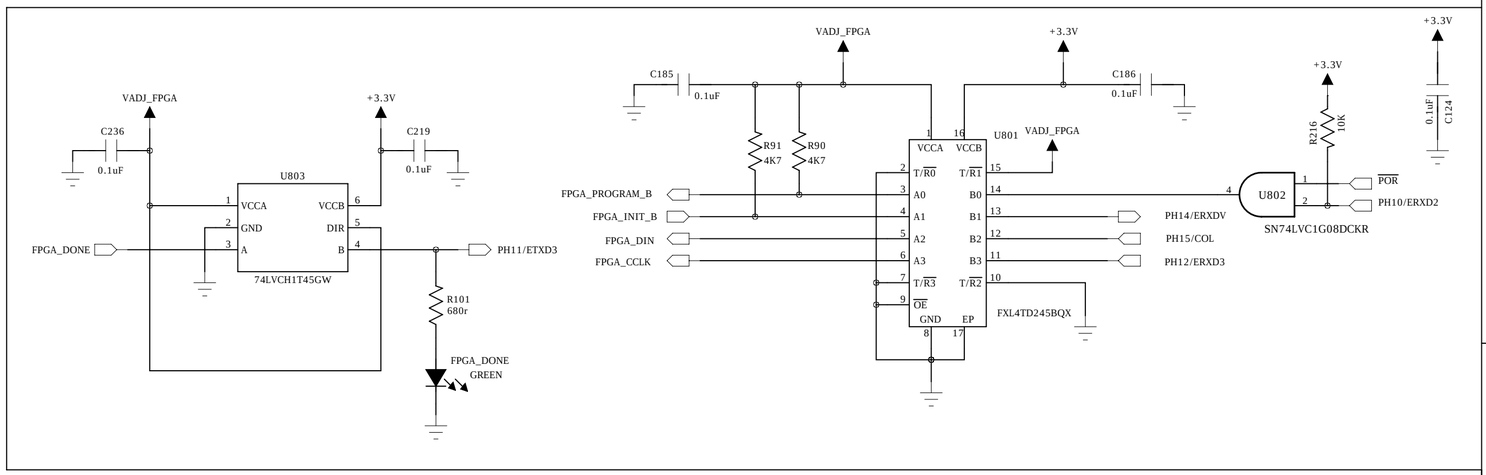




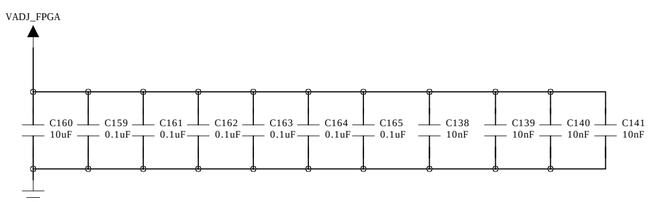




BF-FPGA Configuration Interface

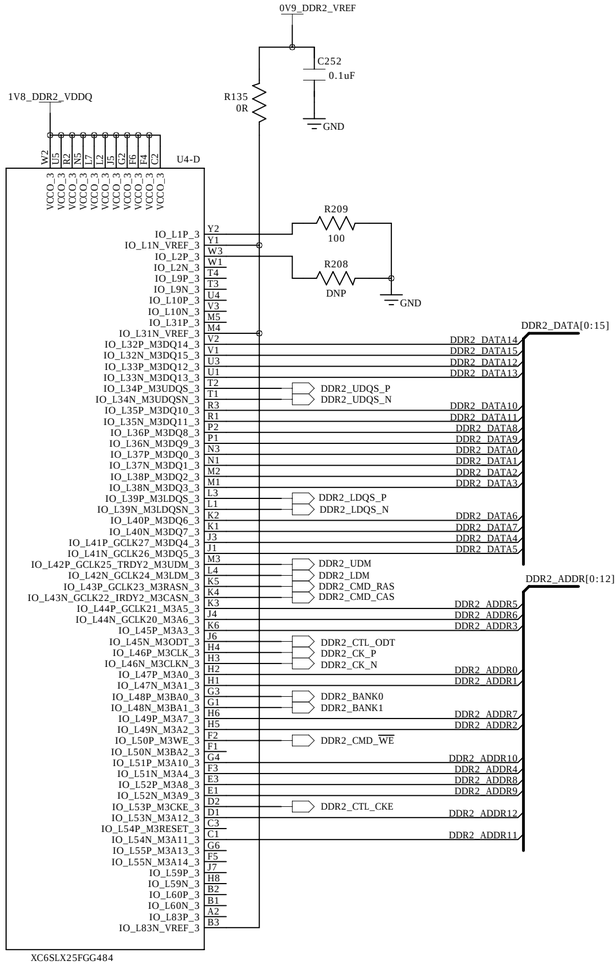


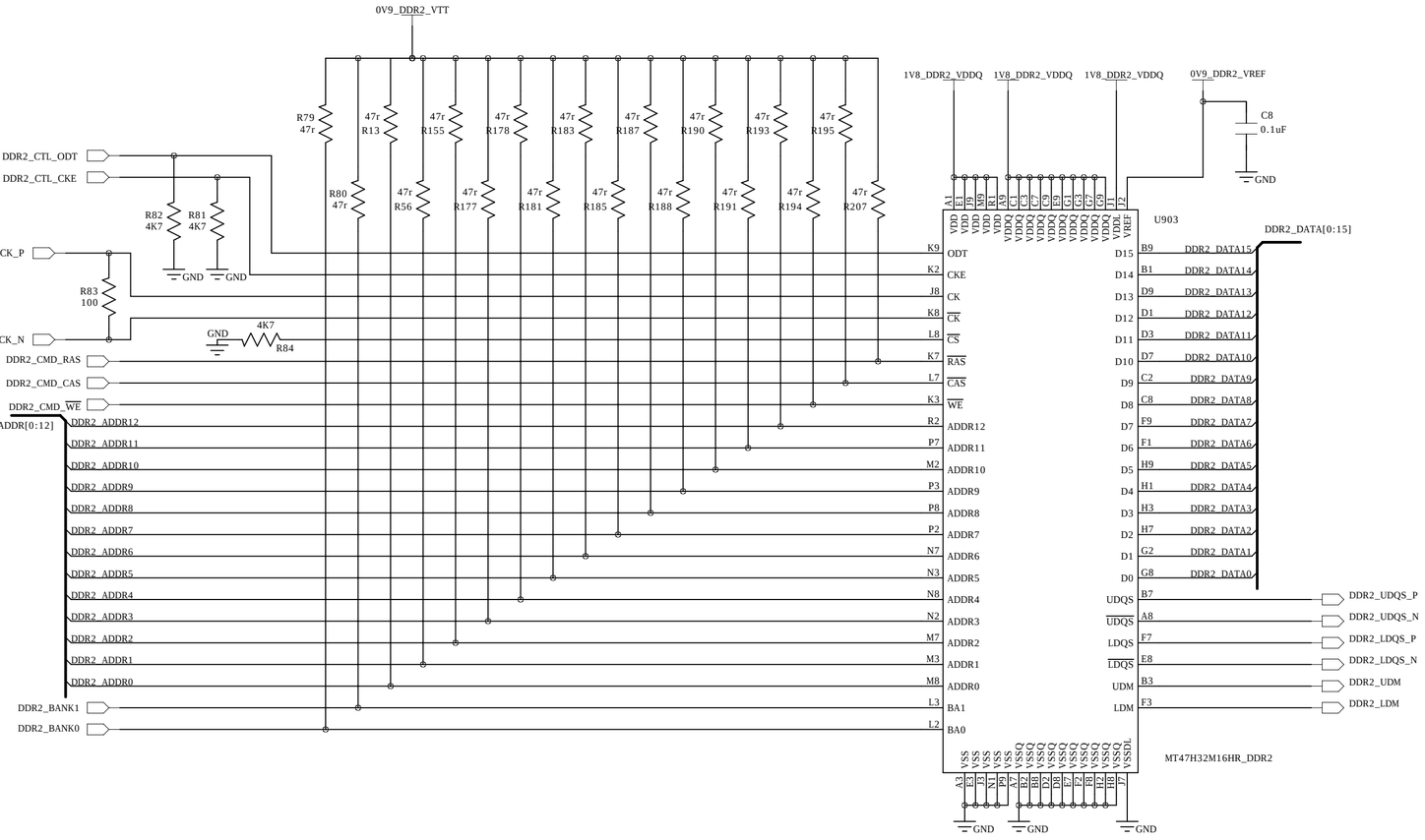
FPGA decoupling



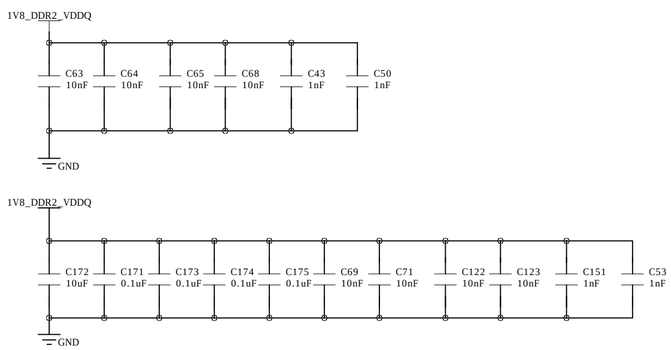
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED: <Checked Date>	TITLE: SDP-H1 (FPGA BANK 2 - FMC)	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: TBD SAP #	REV: 1.1
		SCALE: <Scale>	SHEET: 8 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

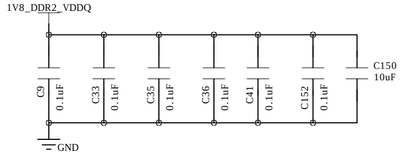




FPGA Decoupling

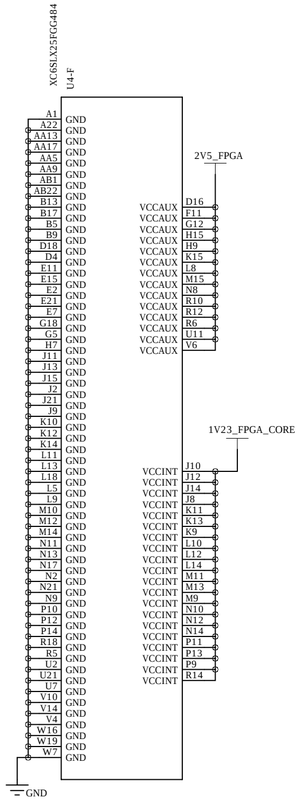


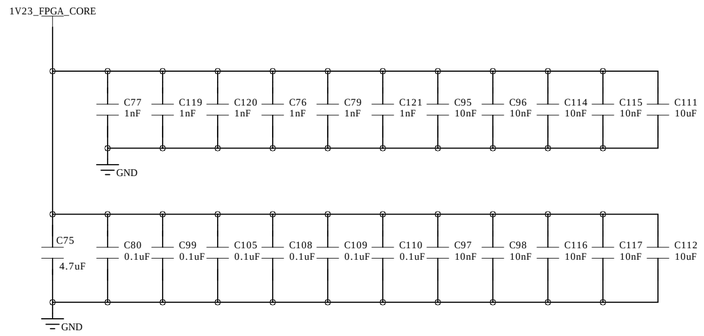
DDR2 Decoupling

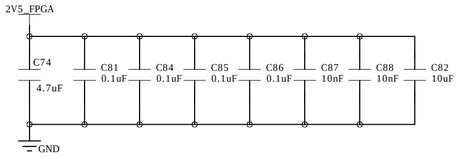


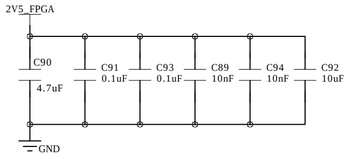
COMPANY: ANALOG DEVICES			
TITLE: SDP-H1 (FPGA BANK 3 - SDRAM)			
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	CODE: <Code>	SIZE: A2
CHECKED: TBD	DATED: <Checked Date>	DRAWING NO: TBD SAP #	REV: 1.1
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 9 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



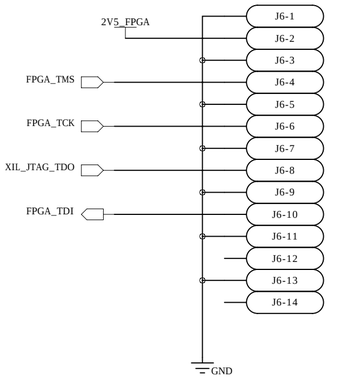


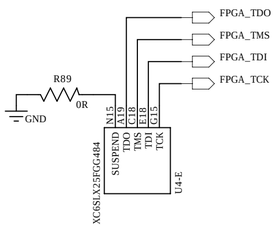


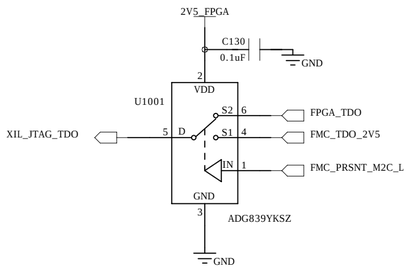


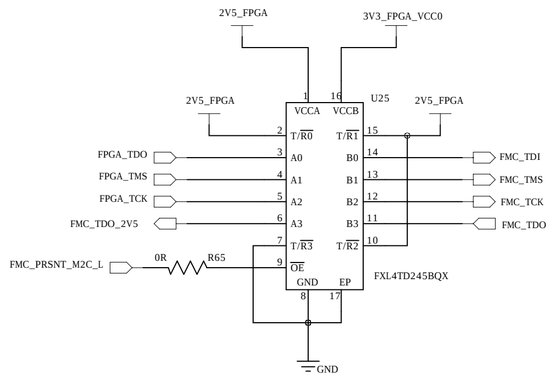
Xilinx FPGA JTAG Connector

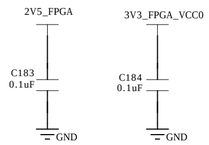
87832-1420-TB32







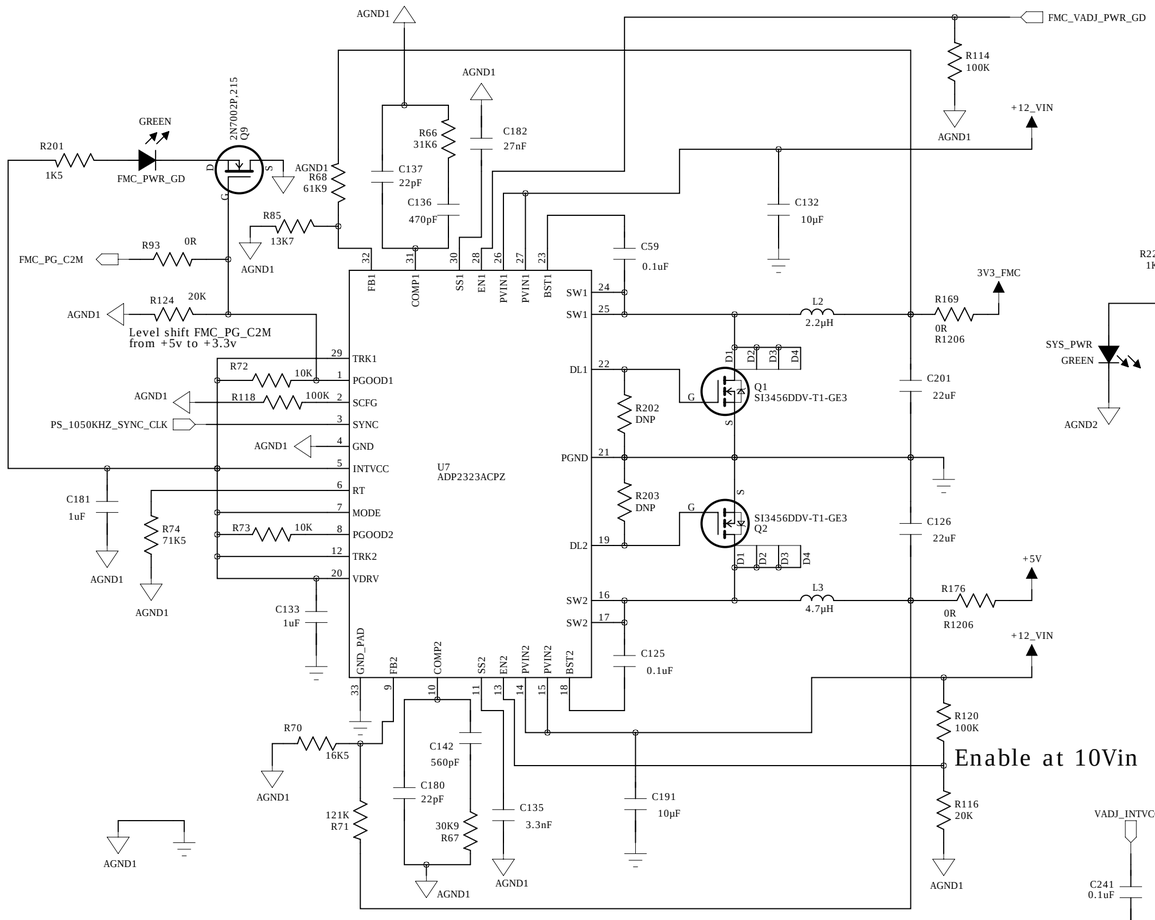




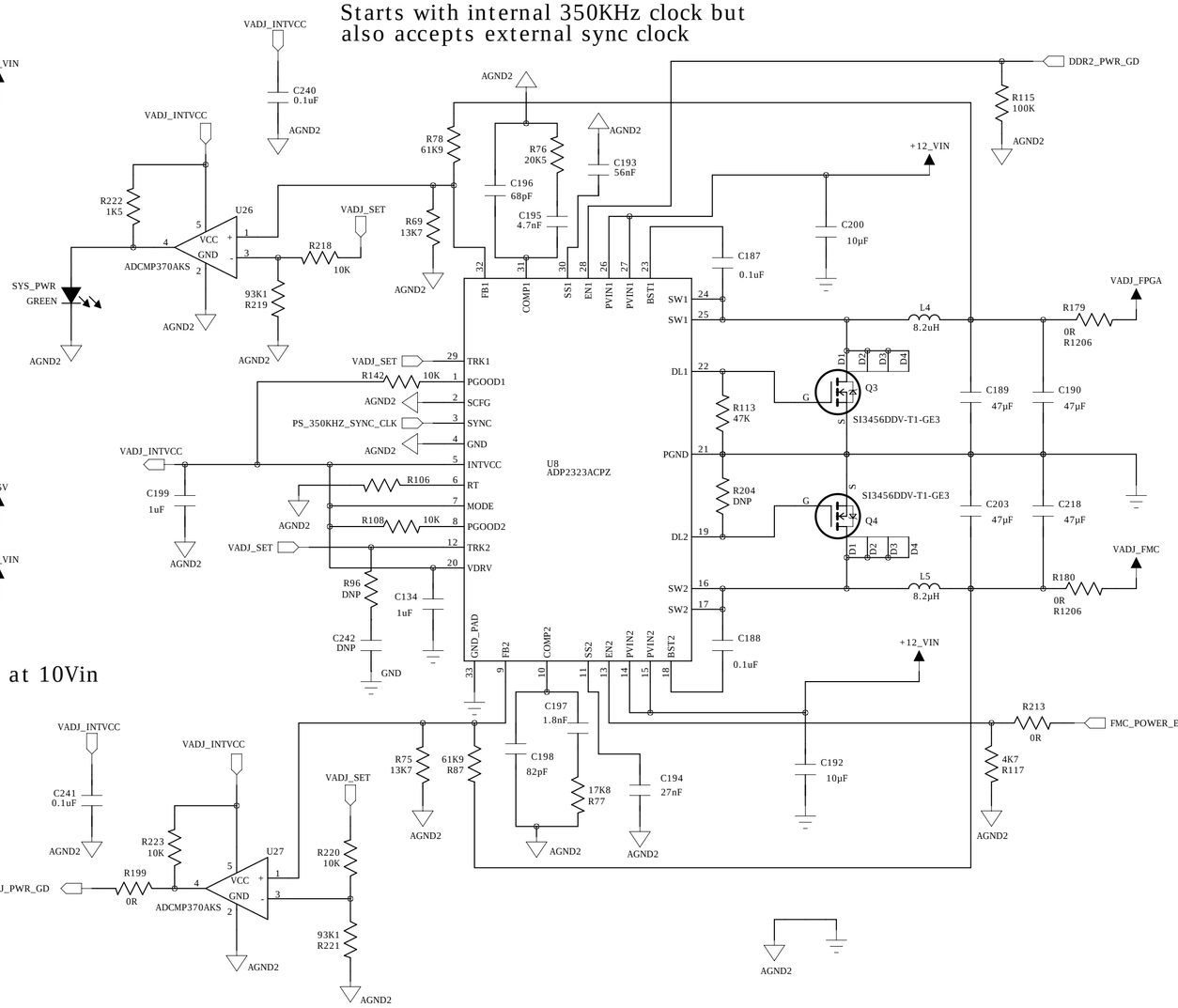
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED: <Checked Date>	TITLE: SDP-H1 (FPGA POWER)	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: TBD SAP #	REV: 1.1
		SCALE: <Scale>	SHEET: 10 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

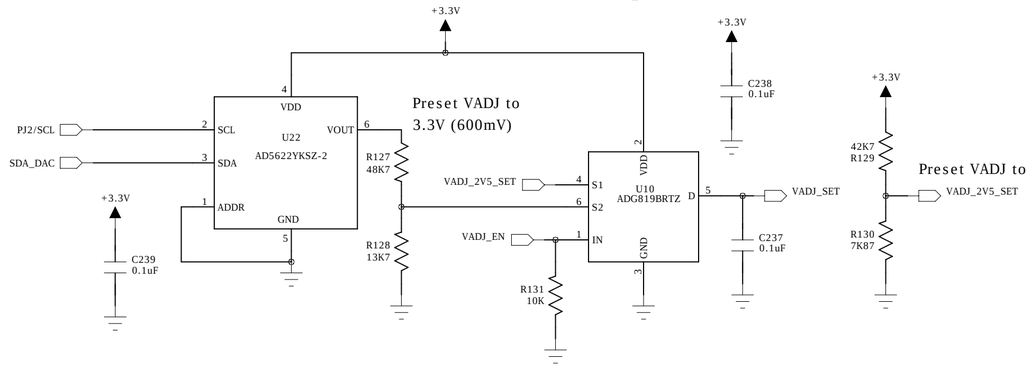
Power supply #1 for:
CH1: 12Vin. 3.3Vout 3A for FMC Conn
CH2: 12Vin. 5Vout 1.84A for Intermediate
Starts with internal 1050KHz clock but
also accepts external sync clock



Power supply #2 for:
CH1: 12Vin. VADJ 0.5A for FPGA VCC2 (1.2V, 1.8V, 2.5V, 3.3V)
CH2: 12Vin. VADJ 2A for FPGA VCC2 (1.2V, 1.8V, 2.5V, 3.3V)
Channels track input voltage to create programmable VADJ
Starts with internal 350KHz clock but
also accepts external sync clock



For setting VADJ to 1.2V, 1.8V, 2.5V or 3.3V
When VADJ_SET is 600mV, VADJ output is 3.3V

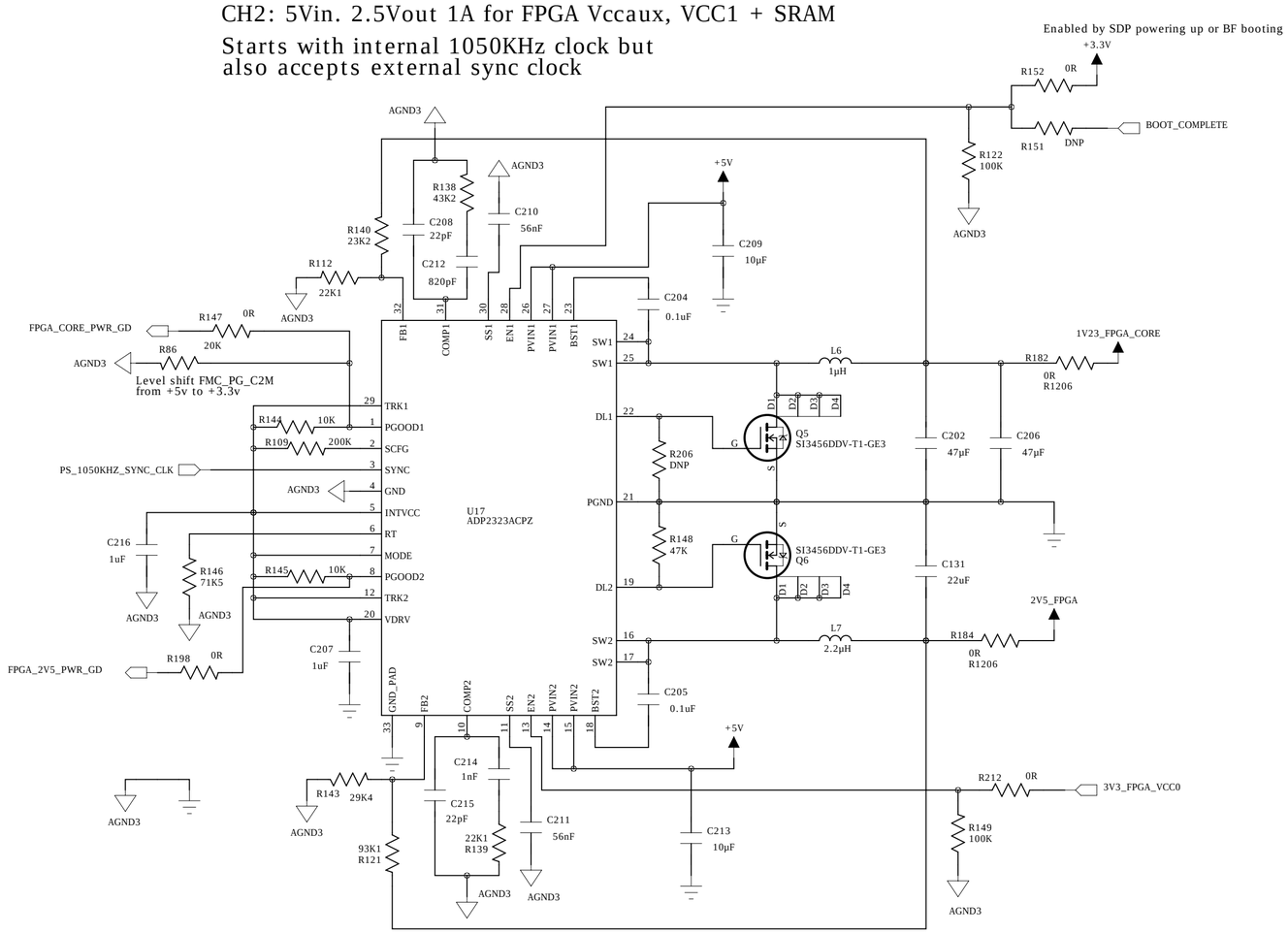


Enable at 10Vin

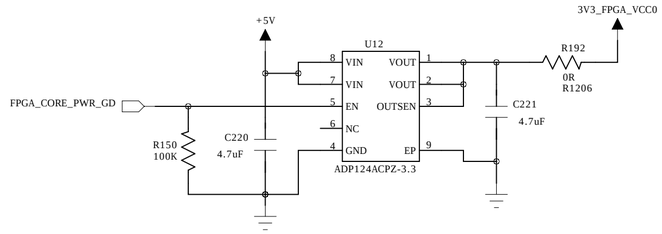
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED: <Checked Date>	TITLE: SDP-H1 (POWER SUPPLY PART 1)	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: TBD SAP #	REV: 1.1
		SCALE: <Scale>	SHEET: 10F 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

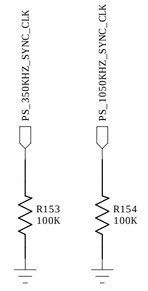
Power supply #3 for:
CH1: 5Vin. 1.23Vout 2A for FPGA core
CH2: 5Vin. 2.5Vout 1A for FPGA Vccaux, VCC1 + SRAM
Starts with internal 1050KHz clock but
also accepts external sync clock



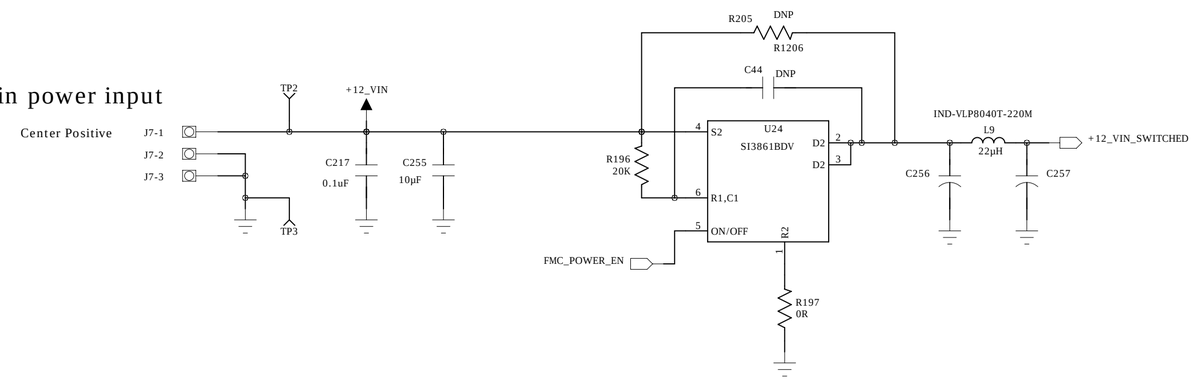
Power supply #5 for FPGA VCC0
4.25-4.75Vin 3.3Vout 250mA



Pull-downs to keep ADP2323 clock sync
lines low while FPGA is unconfigured



Main power input



DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	COMPANY: ANALOG DEVICES	
CHECKED: TBD	DATED: <Checked Date>	TITLE: SDP-H1 (POWER SUPPLY PART 2)	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: TBD SAP #	REV: 1.1
		SCALE: <Scale>	SHEET: 12 OF 13

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Switcher/LDO for DDR2 supply, termination and reference

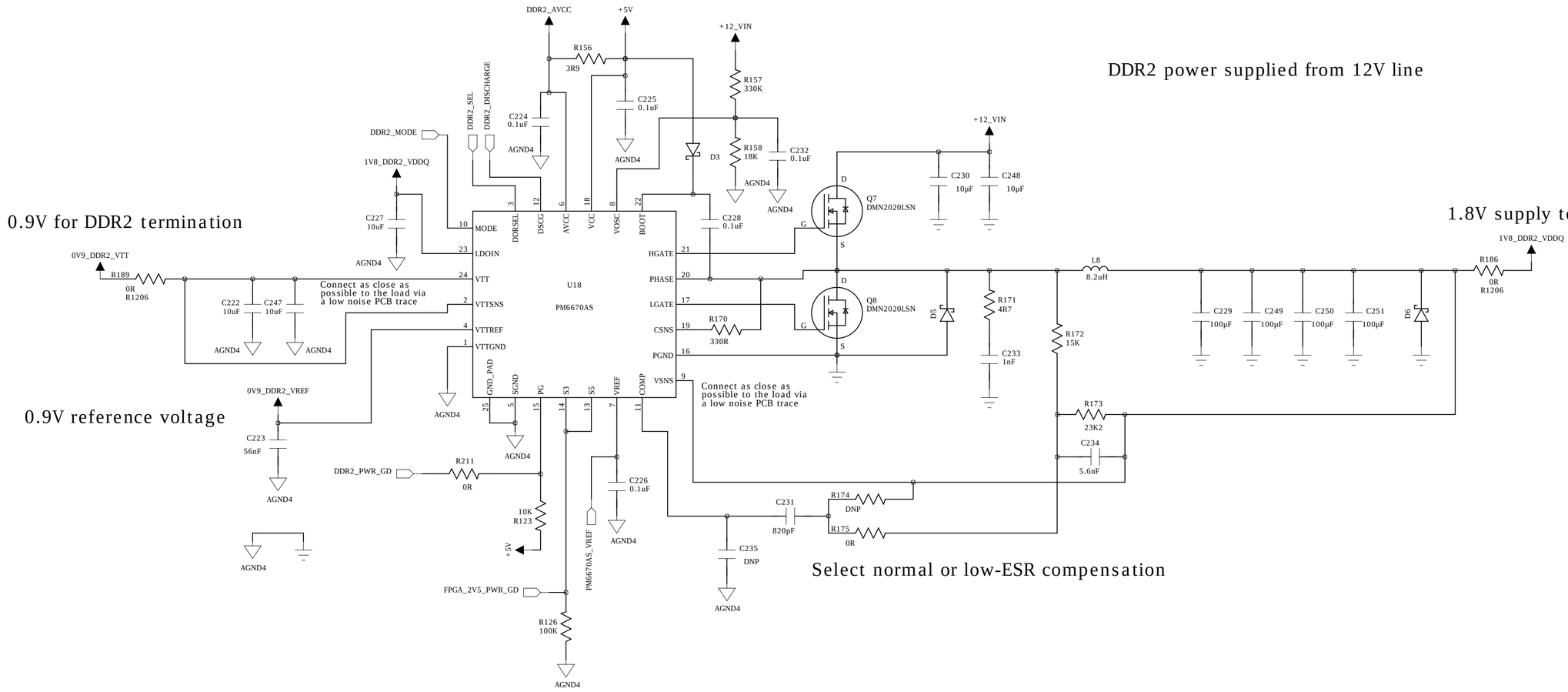
Logic supply taken from intermediate 5V

DDR2 power supplied from 12V line

0.9V for DDR2 termination

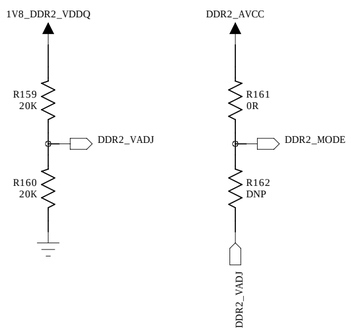
1.8V supply to DDR2

0.9V reference voltage

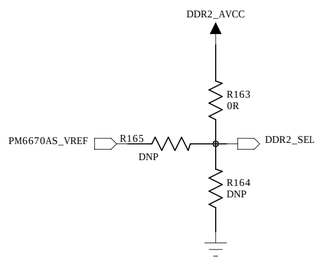


Select normal or low-ESR compensation

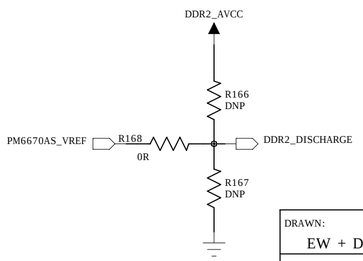
See table 8 of PM6670AS datasheet



See table 8 of PM6670AS datasheet



See table 9 of PM6670AS datasheet



COMPANY: ANALOG DEVICES			
TITLE: SDP-H1 (POWER SUPPLY PART 3)			
DRAWN: EW + DP + MMcC	DATED: 06/Jun/12	CODE: <Code>	SIZE: A2
CHECKED: TBD	DATED: <Checked Date>	DRAWING NO: TBD SAP #	REV: 1.1
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 13 OF 13