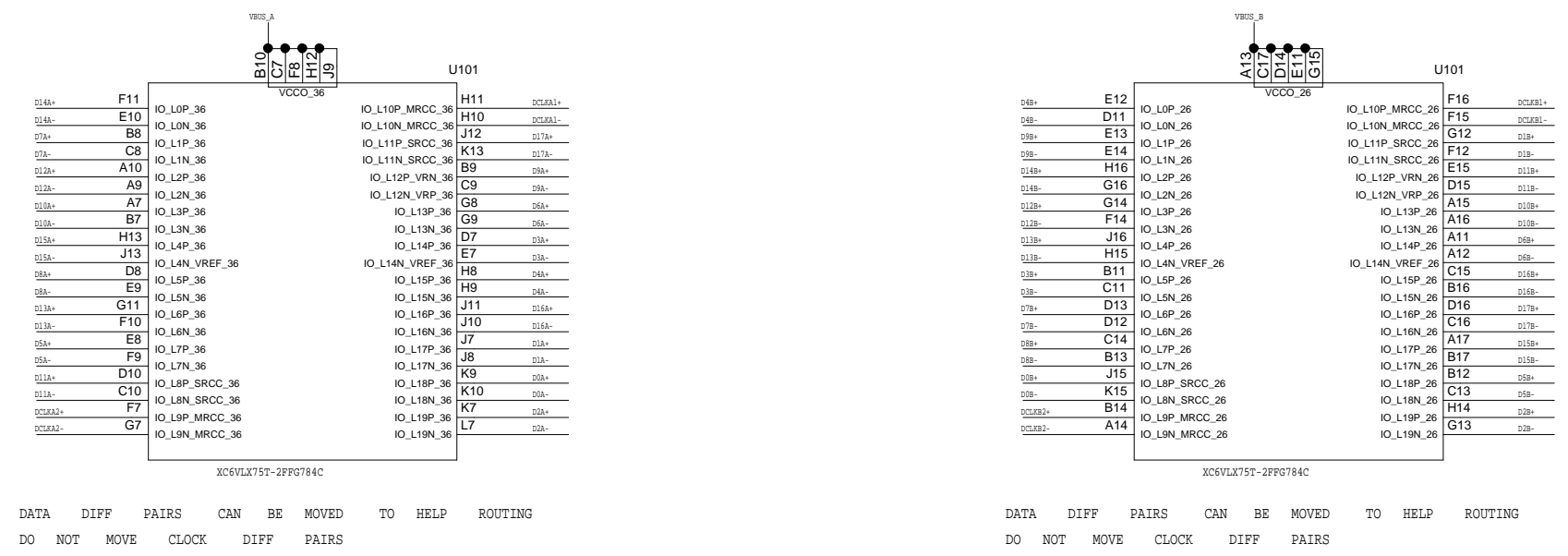


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1		APR-2011	

PARALLEL DATA BUS A AND B



DIFF PAIR ROUTING LENGTHS MUST BE MATCHED TO WITHIN 50 MILS
BUS ROUTING LENGTHS MUST BE MATCHED TO WITHIN 250 MILS

NOTE: J1 IS ON SHEET 10

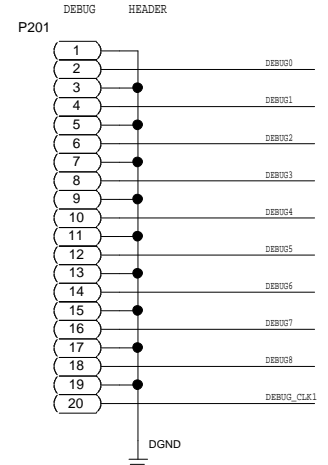
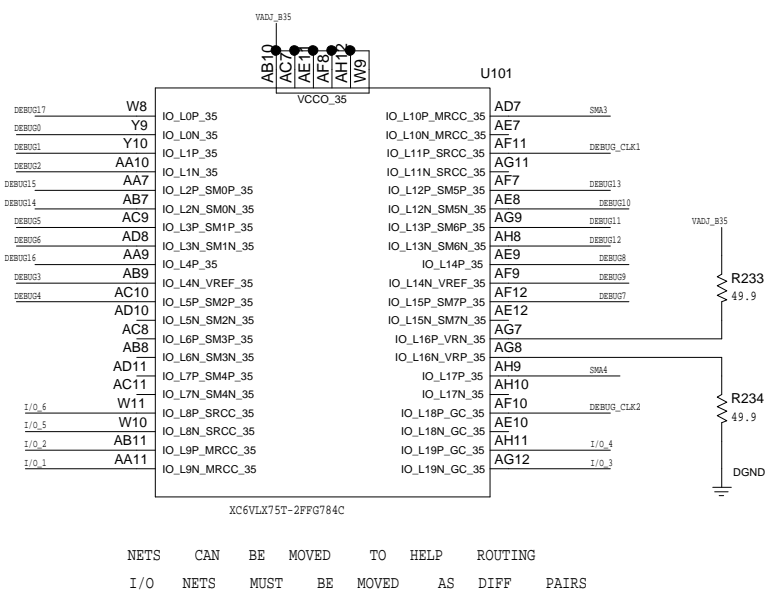
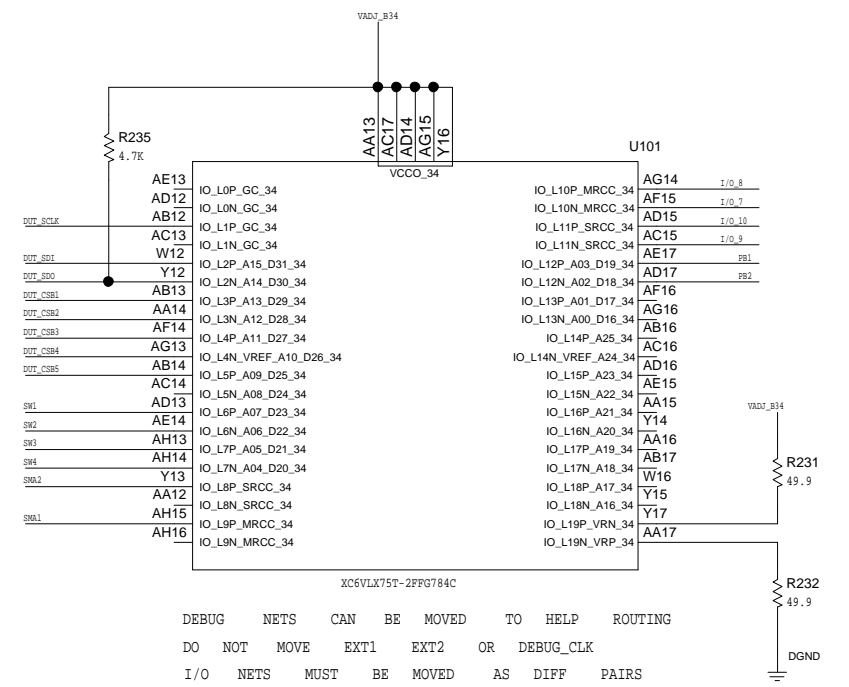


HADV6-REVD

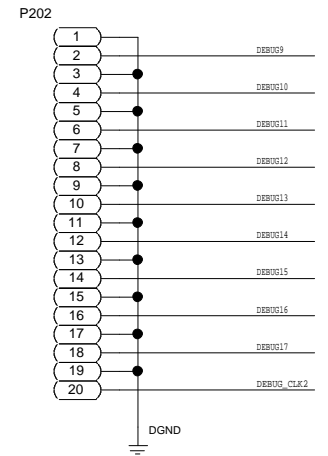
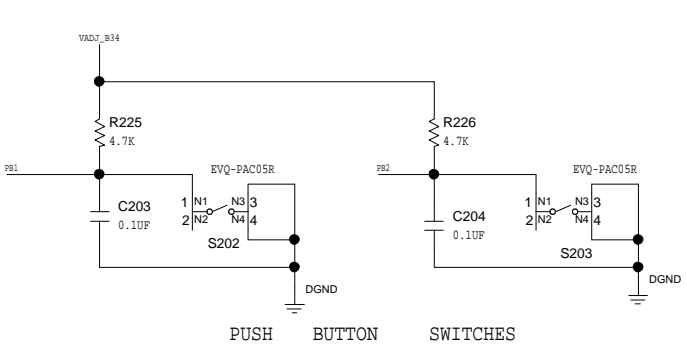
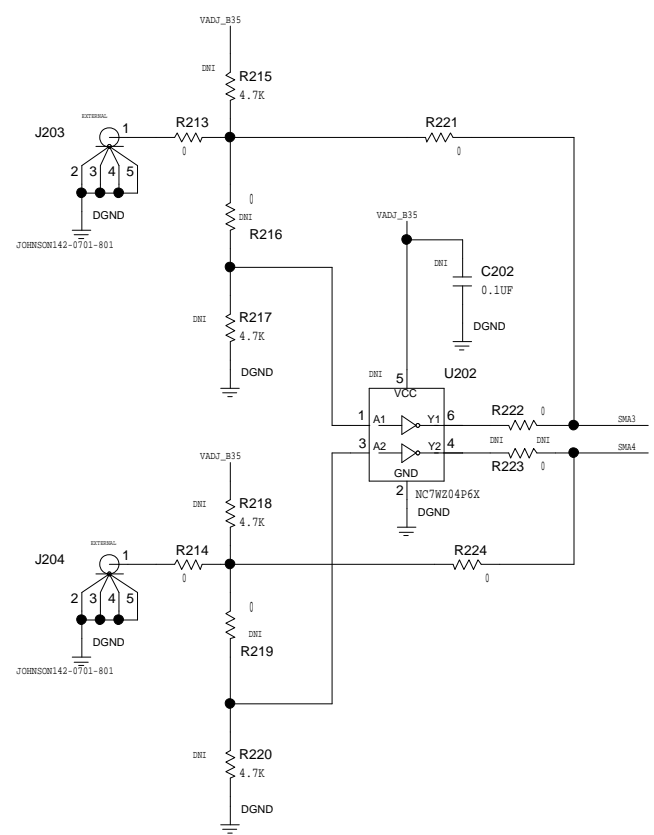
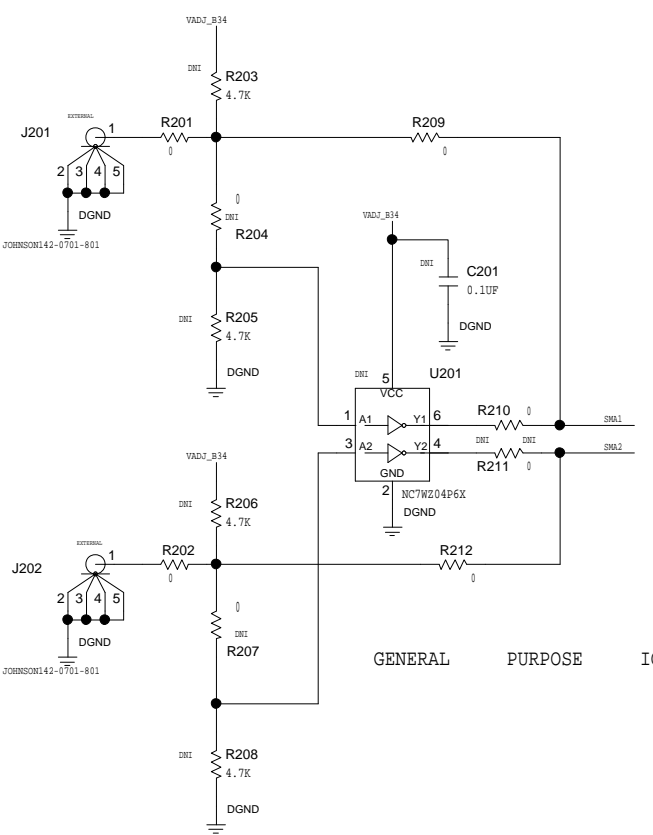
	SCHEMATIC		
	HADV6 <PRODUCT_1>		
<small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN ANY MANNER THAT WOULD BE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.</small>	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 1 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

MISC. BANKS 34 AND 35



CA-D20-24C-44

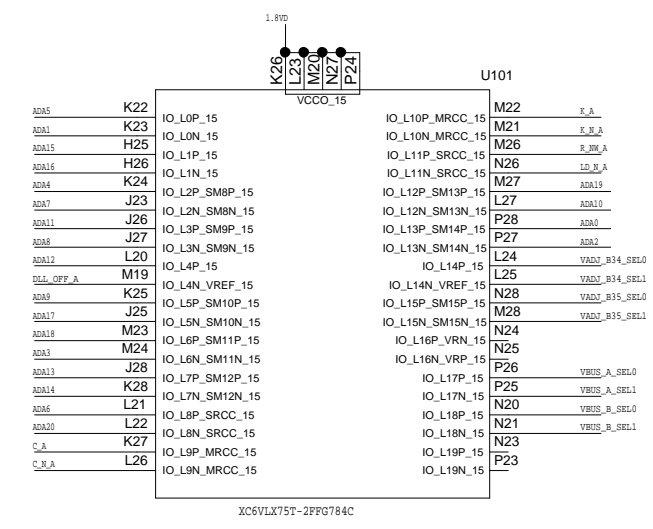
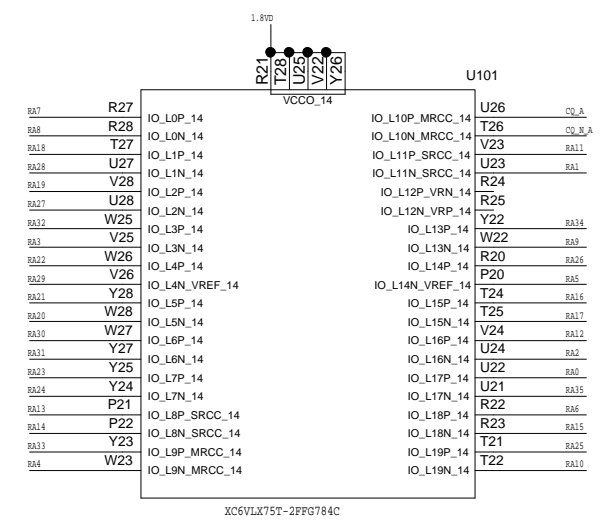


CA-D20-24C-44

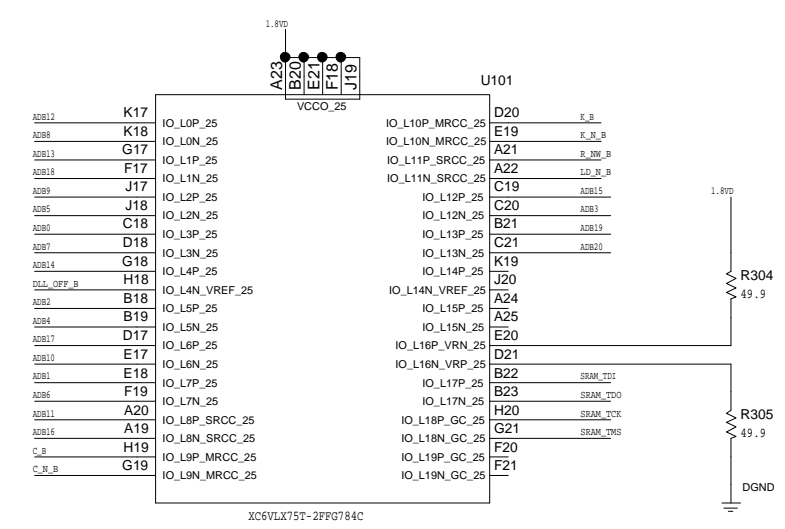
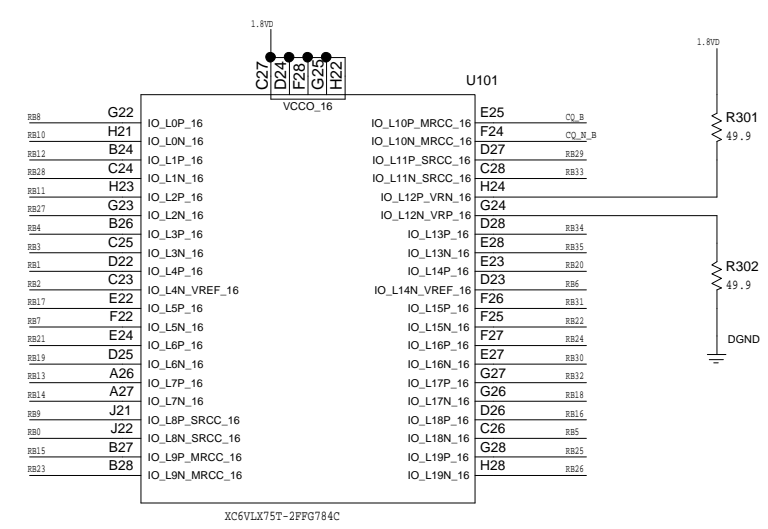
	SCHEMATIC		
	HADV6 <PRODUCT_1>	DRAWING NO.	REV
DESIGN VIEW <DESIGN_VIEW>			D
PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE>	SHEET 2 OF 17	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FPGA - SRAM INTERFACE AND BANK CONTROLS



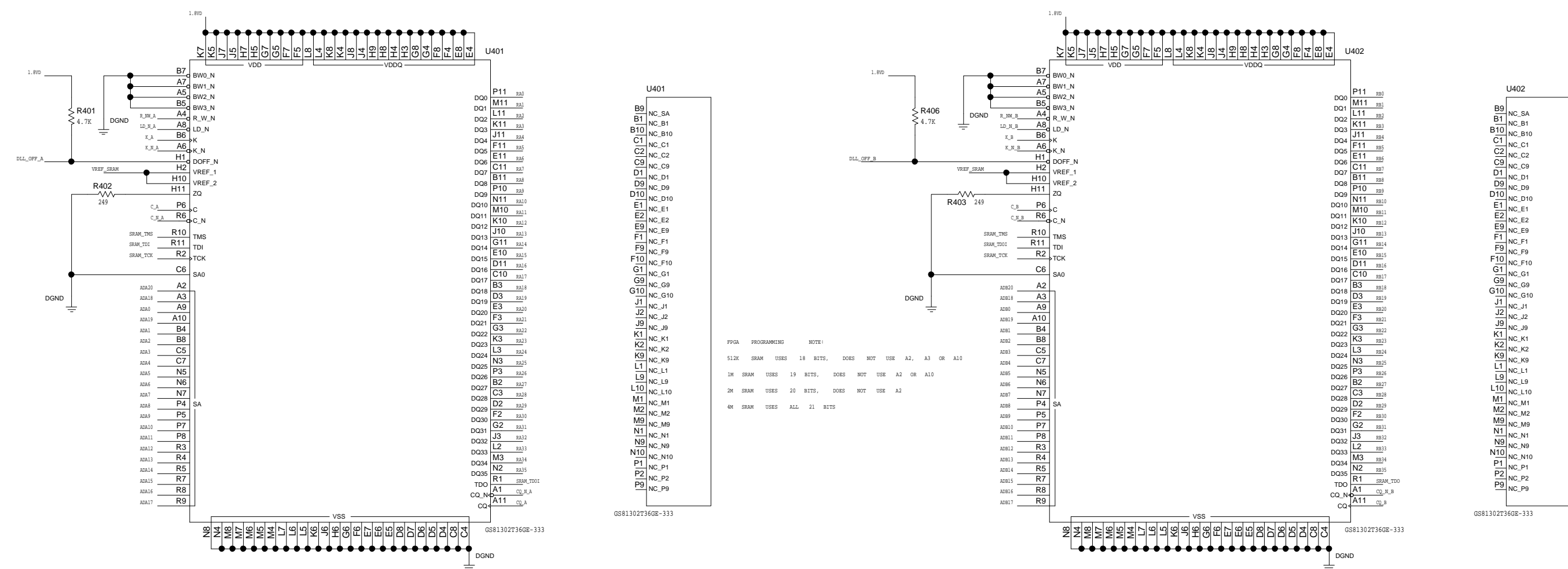
RA, RB AND AD LINES CAN BE MOVED WITHIN BANKS TO HELP ROUTING
 ASK ENGINEER BEFORE MOVING ANY OTHER LINES



	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 3 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

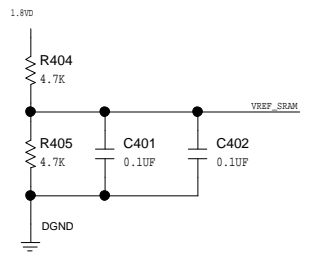
SRAM A AND B



PGA PROGRAMMING NOTE:
 512K SRAM USES 18 BITS, DOES NOT USE A2, A3 OR A10
 1M SRAM USES 19 BITS, DOES NOT USE A2 OR A10
 2M SRAM USES 20 BITS, DOES NOT USE A2
 4M SRAM USES ALL 21 BITS



PLACE ONE SRAM CHIP ON TOP SIDE
 PLACE THE OTHER SRAM CHIP ON BOTTOM SIDE
 ADDRESS LINES ARE SHARED
 K AND K_N LINES ARE SHARED
 C AND C_N LINES ARE SHARED



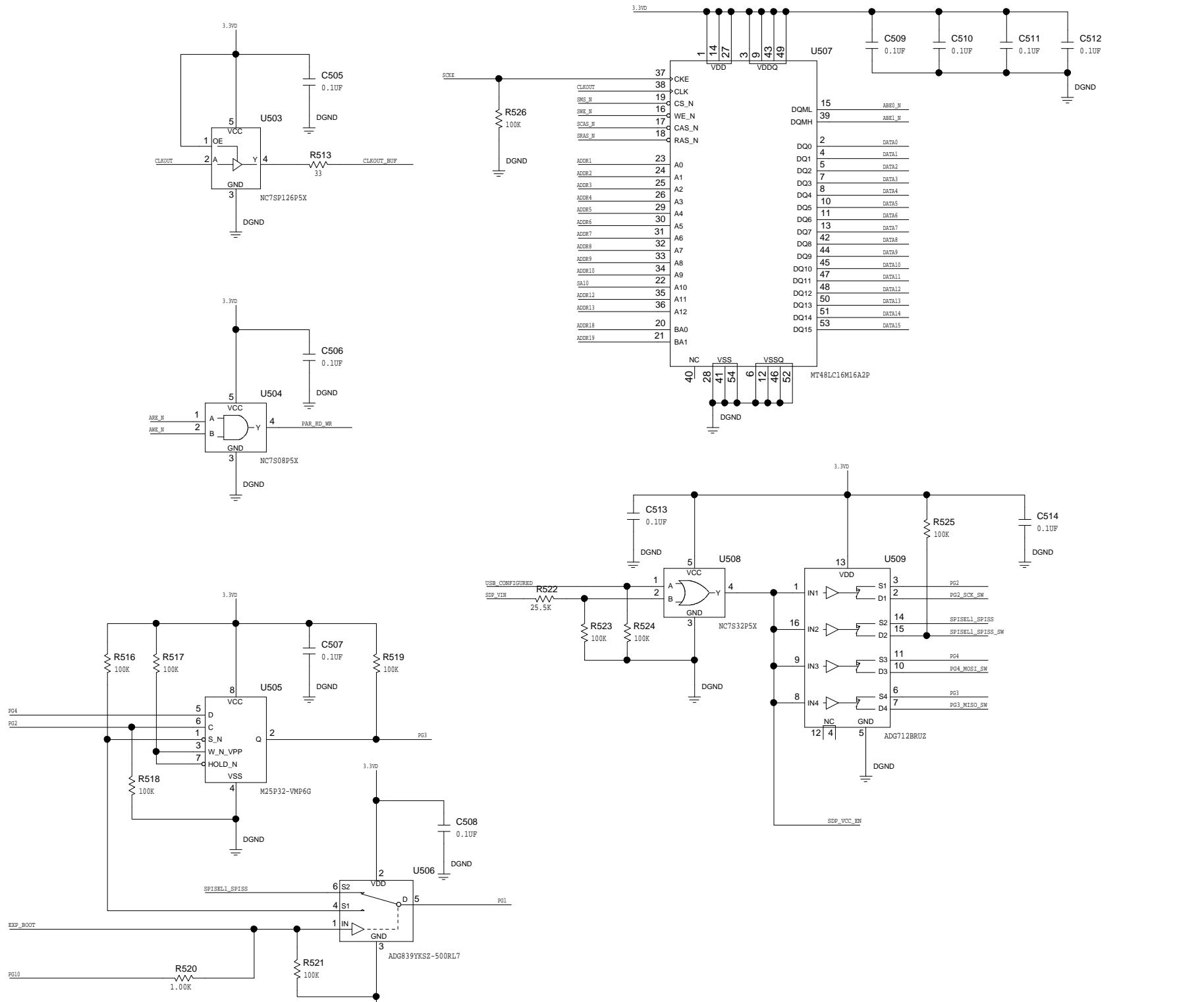
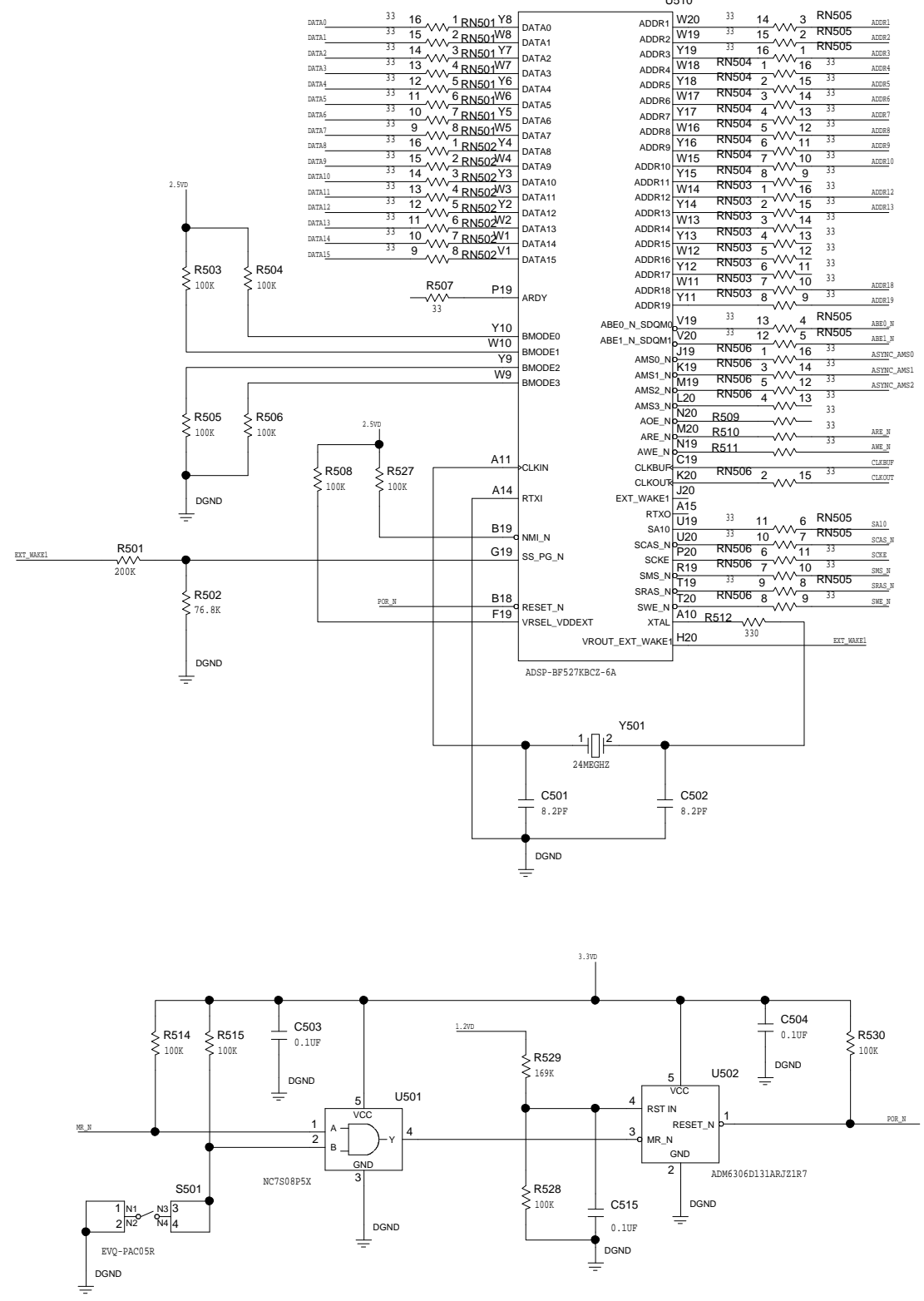
	SCHEMATIC		
	HADV6 <PRODUCT_1>		
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D	
PDT ENGINEER <PDT_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 4 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

BF SDRAM

RESISTOR ARRAY SECTIONS MAY BE REASSIGNED AS NEEDED

U510		U507					
DATA0	33 16	1 RN501 Y8	DATA0	ADDR1	W20 33 14	3 RN505	ADDR1
DATA1	33 15	2 RN501 W8	DATA1	ADDR2	W19 33 15	2 RN505	ADDR2
DATA2	33 14	3 RN501 Y7	DATA2	ADDR3	Y19 33 16	1 RN505	ADDR3
DATA3	33 13	4 RN501 W7	DATA3	ADDR4	W18 RN504 1	16 33	ADDR4
DATA4	33 12	5 RN501 Y6	DATA4	ADDR5	Y18 RN504 2	15 33	ADDR5
DATA5	33 11	6 RN501 W6	DATA5	ADDR6	W17 RN504 3	14 33	ADDR6
DATA6	33 10	7 RN501 Y5	DATA6	ADDR7	Y17 RN504 4	13 33	ADDR7
DATA7	33 9	8 RN501 W5	DATA7	ADDR8	W16 RN504 5	12 33	ADDR8
DATA8	33 8	9 RN501 Y4	DATA8	ADDR9	Y16 RN504 6	11 33	ADDR9
DATA9	33 7	10 RN501 W4	DATA9	ADDR10	W15 RN504 7	10 33	ADDR10
DATA10	33 6	11 RN501 Y3	DATA10	ADDR11	Y15 RN504 8	9 33	ADDR11
DATA11	33 5	12 RN501 W3	DATA11	ADDR12	W14 RN503 1	16 33	ADDR12
DATA12	33 4	13 RN501 Y2	DATA12	ADDR13	Y14 RN503 2	15 33	ADDR13
DATA13	33 3	14 RN501 W2	DATA13	ADDR14	W13 RN503 3	14 33	ADDR14
DATA14	33 2	15 RN501 Y1	DATA14	ADDR15	Y13 RN503 4	13 33	ADDR15
DATA15	33 1	16 RN501 W1	DATA15	ADDR16	W12 RN503 5	12 33	ADDR16
		17 RN502 V1		ADDR17	Y12 RN503 6	11 33	ADDR17
		18 RN502 V1		ADDR18	W11 RN503 7	10 33	ADDR18
		19 RN502 V1		ADDR19	Y11 RN503 8	9 33	ADDR19
		20 RN502 V1			V19 33 13	4 RN505	ABE0_N_SDQM
		21 RN502 V1			V20 33 12	5 RN505	ABE1_N_SDQM
		22 RN502 V1			J19 RN506 1	16 33	ASYNC_AMS0
		23 RN502 V1			K19 RN506 3	14 33	ASYNC_AMS1
		24 RN502 V1			M19 RN506 5	12 33	ASYNC_AMS2
		25 RN502 V1			L20 RN506 4	13 33	
		26 RN502 V1			N20 RN509		
		27 RN502 V1			M20 RN510		
		28 RN502 V1			N19 RN511		
		29 RN502 V1			C19 RN506 8	9 33	CLKREF
		30 RN502 V1			K20 RN506 2	15 33	CLKOUT
		31 RN502 V1			J20		
		32 RN502 V1			A15		
		33 RN502 V1			U19 33 11	6 RN505	SA10
		34 RN502 V1			U20 33 10	7 RN505	SCAS_N
		35 RN502 V1			P20 RN506 6	11 33	SCKE
		36 RN502 V1			R19 RN506 7	10 33	SMS_N
		37 RN502 V1			T19 33 9	8 RN505	SRAS_N
		38 RN502 V1			T20 RN506 8	9 33	SWE_N
		39 RN502 V1			A10 R512		XTAL
		40 RN502 V1			H20	330	

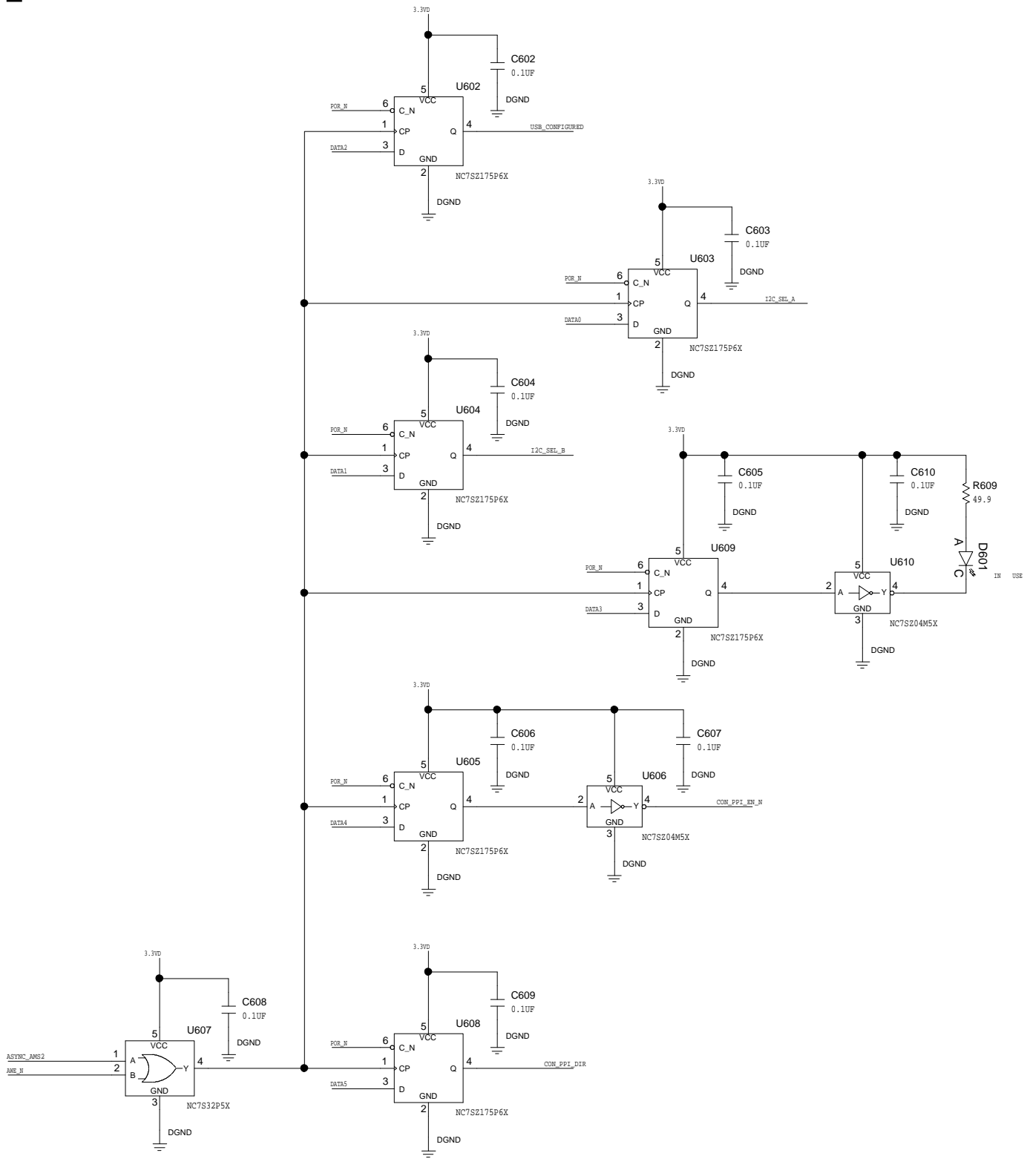
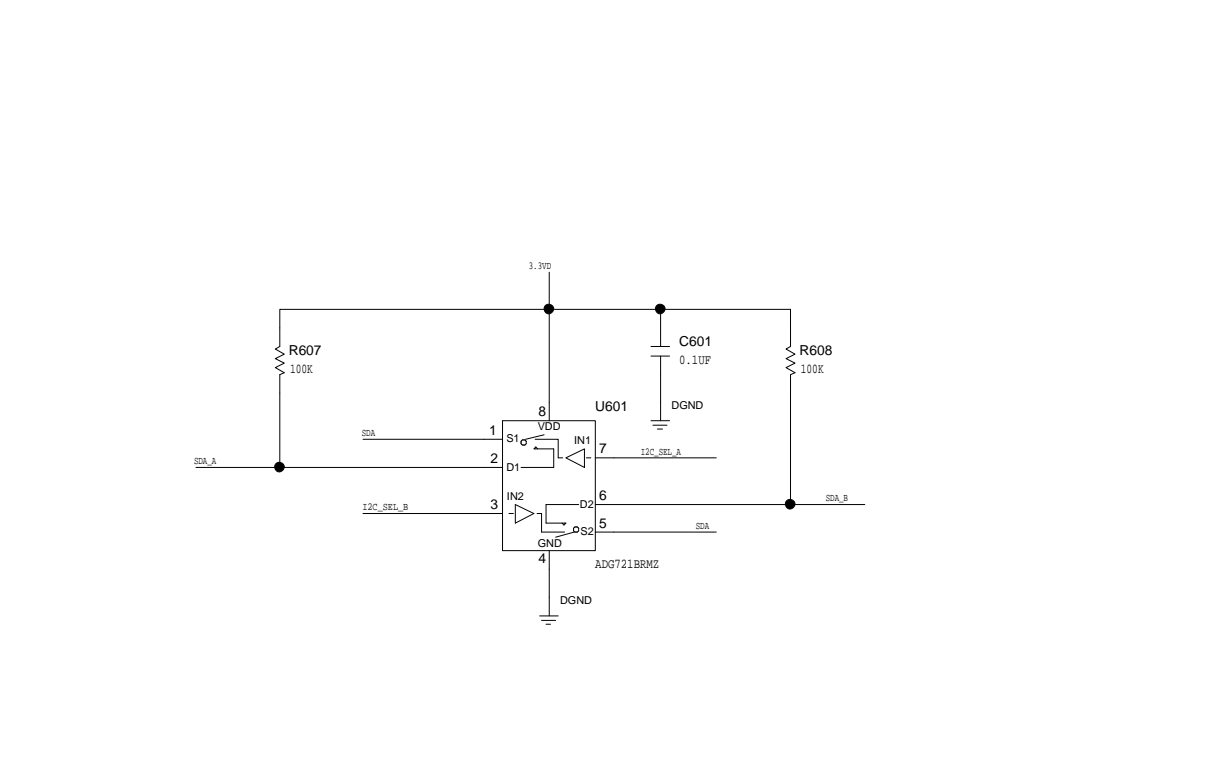
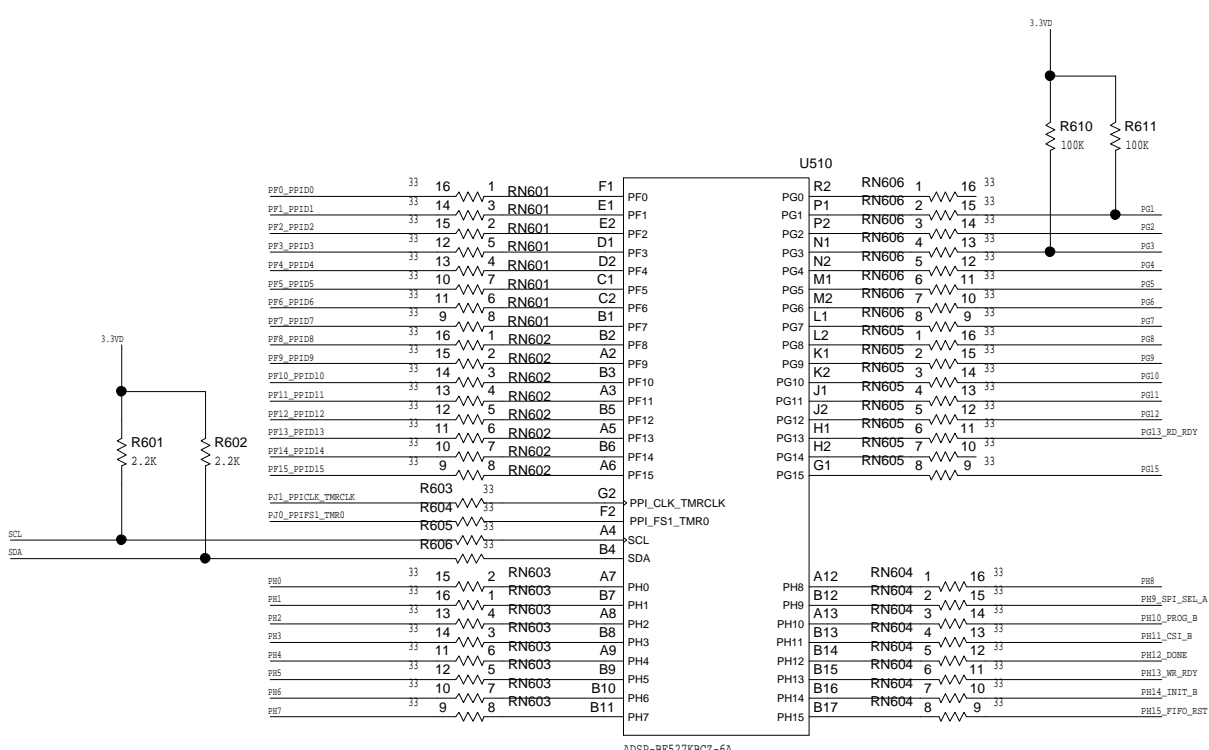


	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

SHEET 5 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

BF PPI

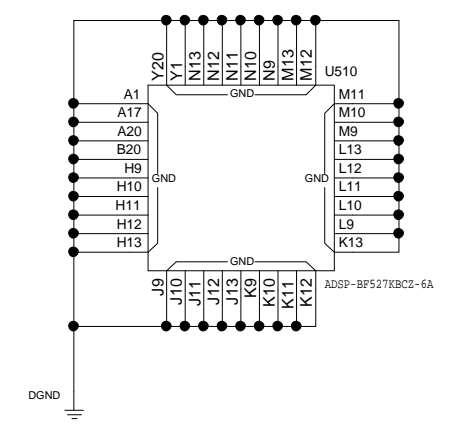
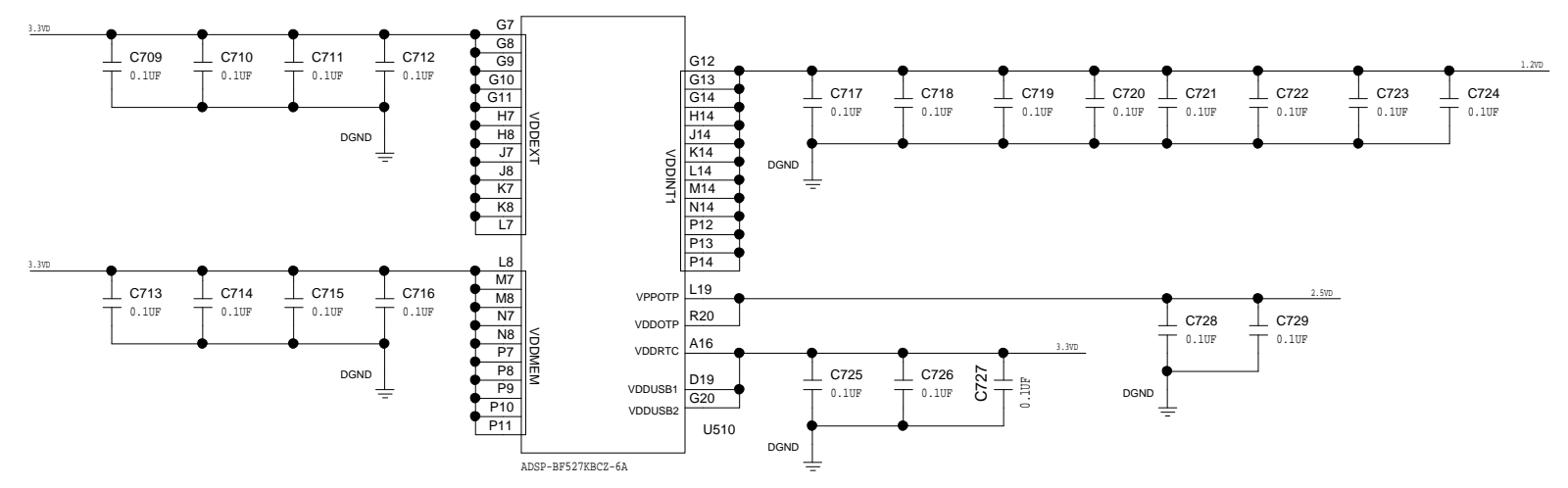
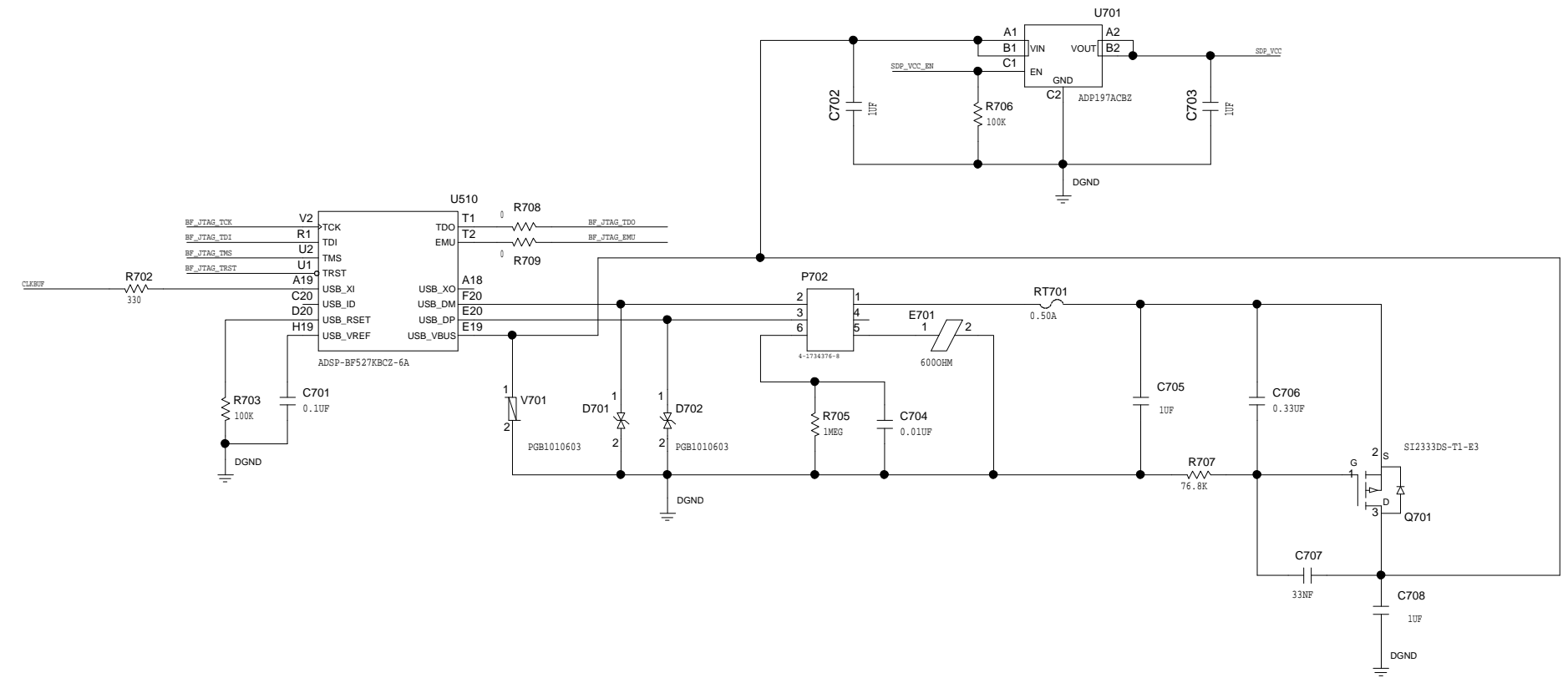
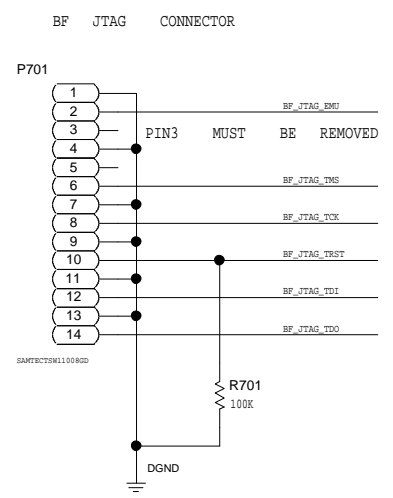


<p>ANALOG DEVICES</p> <p><small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</small></p>	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

SHEET 6 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

BF POWER, USB AND JTAG



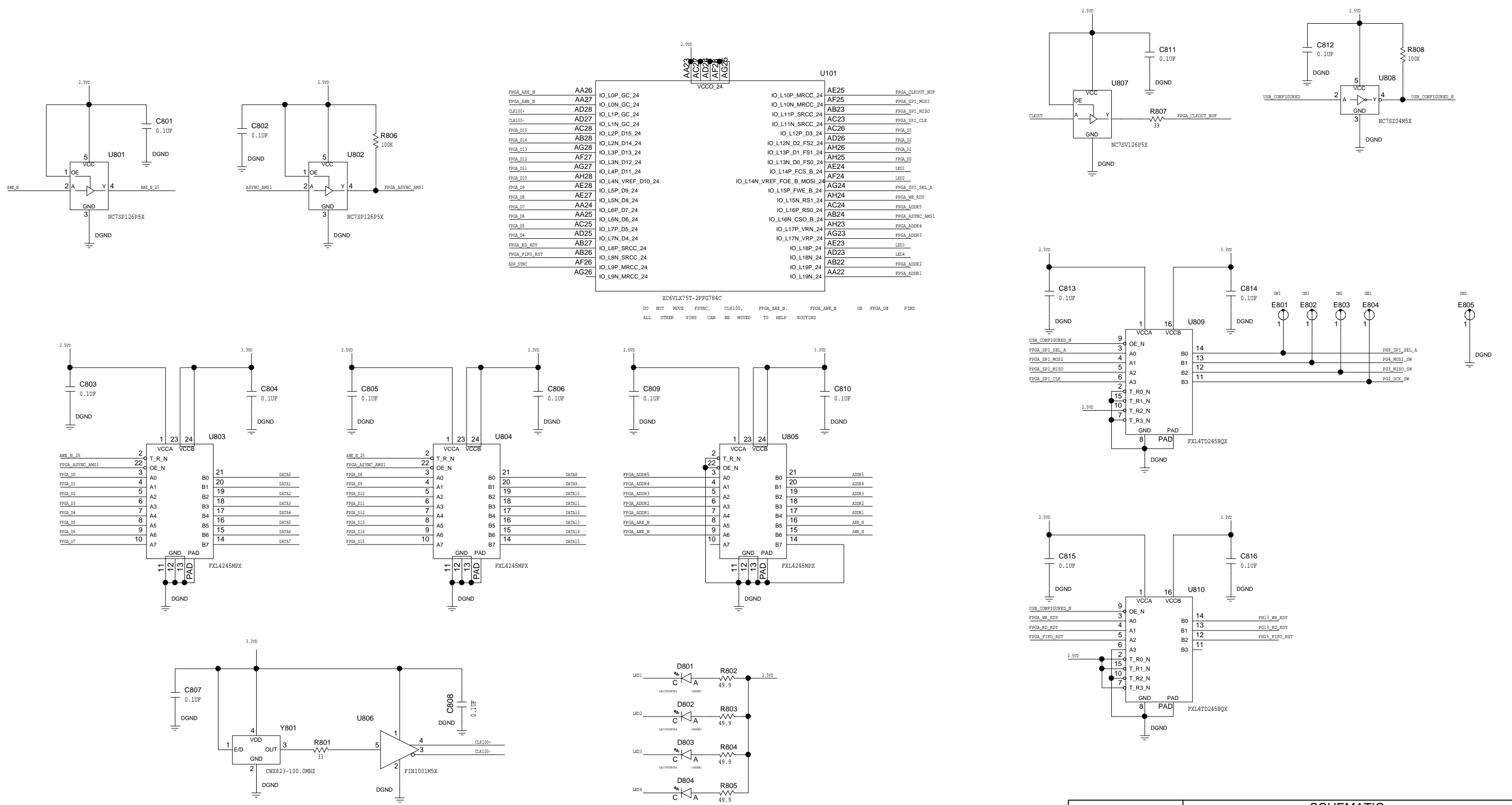
	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.

SHEET 7 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

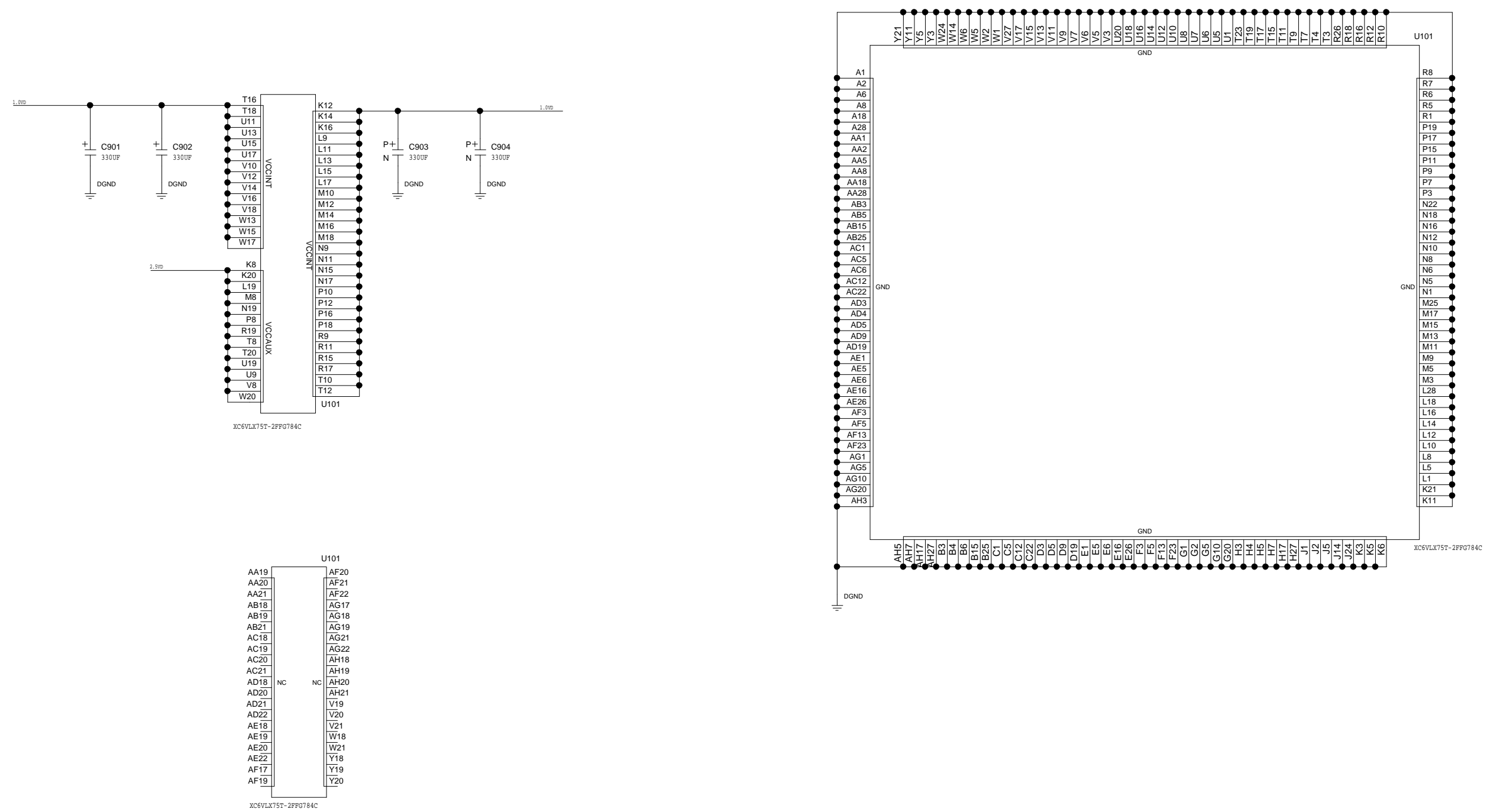
FPGA - BF INTERFACE, MISC



	SCHEMATIC		
	HADV6 <PRODUCT_1>	DRAWING NO. -	REV D
<small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IF NOT FOR REPRODUCTION OR CIRCULATION IN WHOLE OR IN PART OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES, THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.</small>	DESIGN VIEW <DESIGN_VIEW>	SIZE D	SCALE <SCALE>
PTD ENGINEER <PTD_ENGINEER>	SHEET 8 OF 17		

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

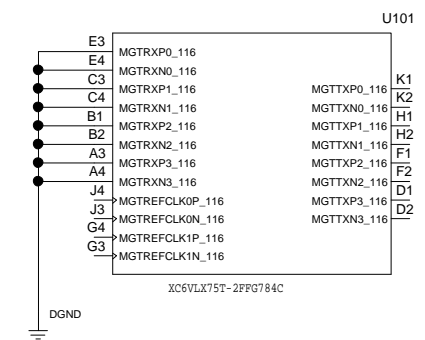
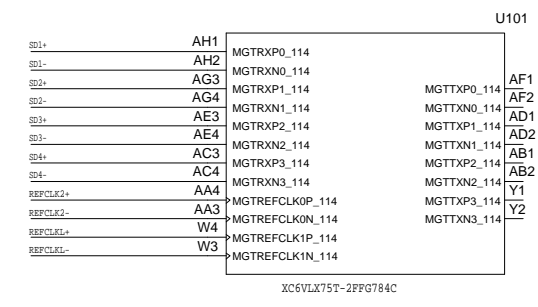
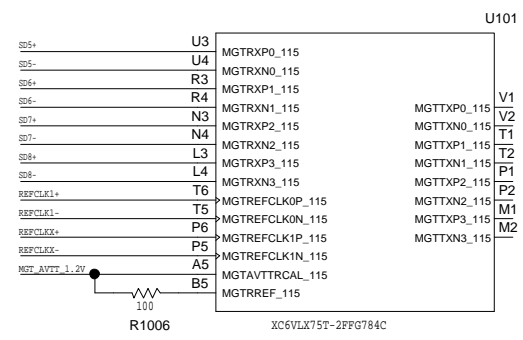
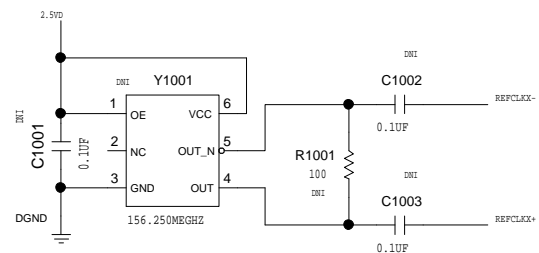
FPGA POWER AND DECOUPLING



<p>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</p>	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 9 OF 17	

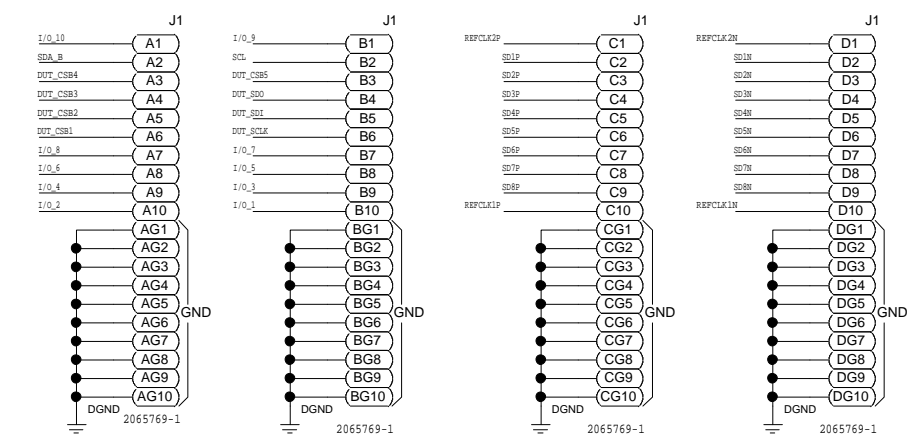
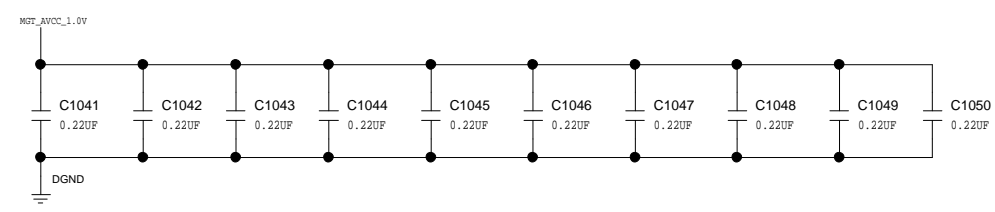
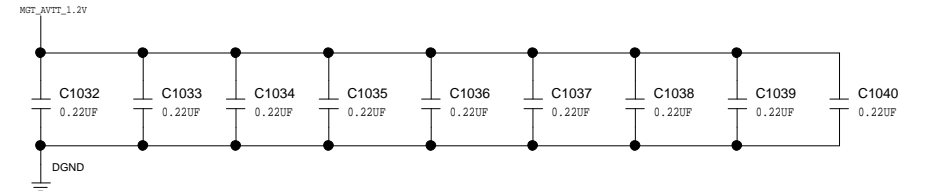
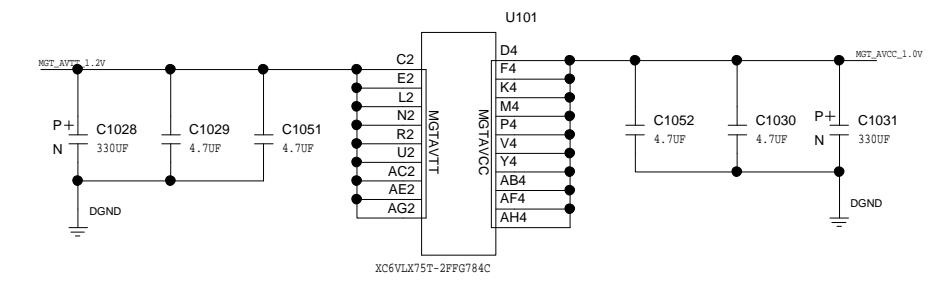
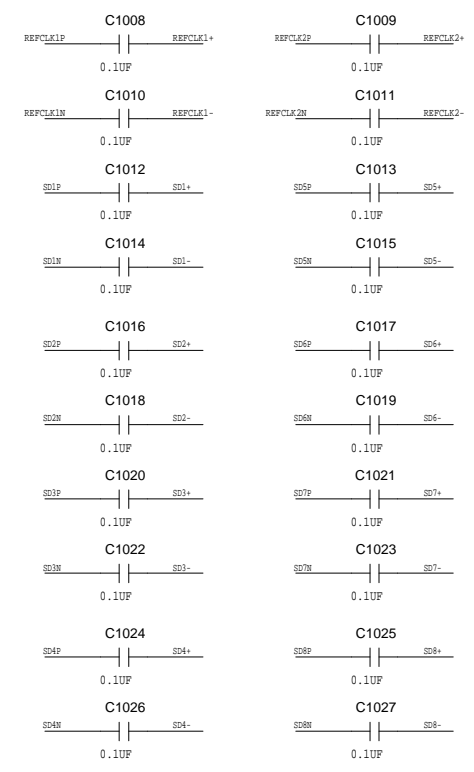
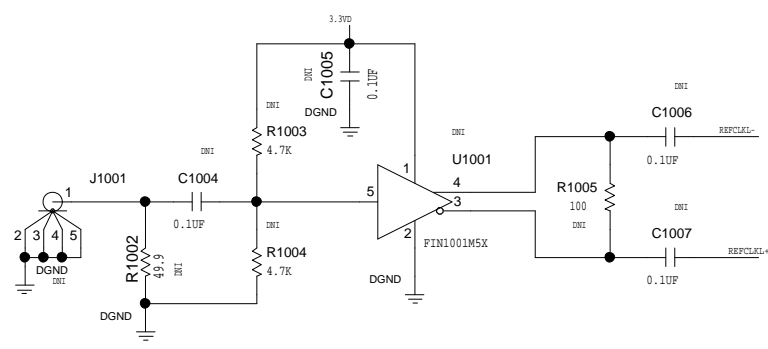
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

GTX CONNECTIONS



SD DIFF PAIRS MAY BE MOVED TO HELP ROUTING
DO NOT CROSS BANKS

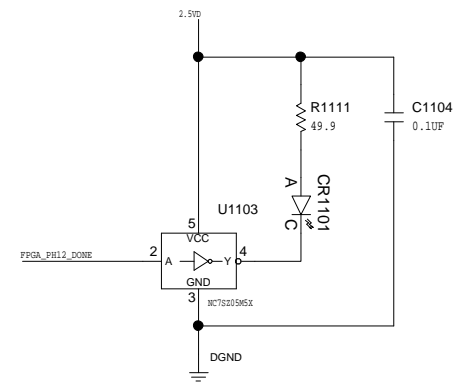
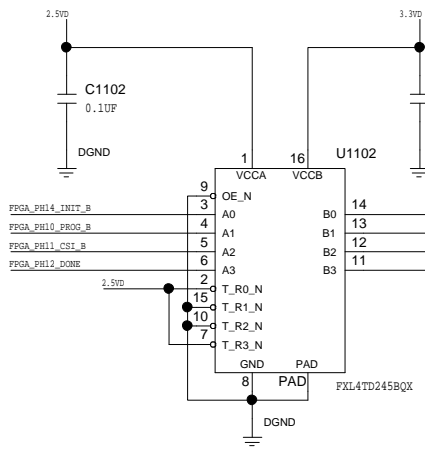
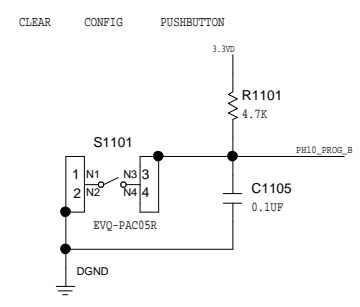
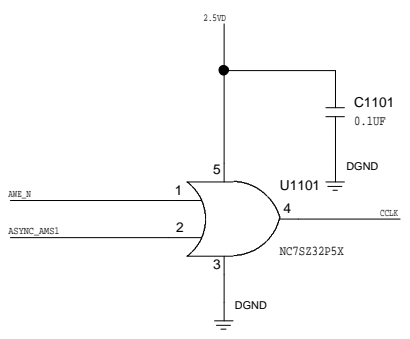
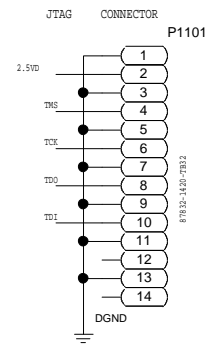
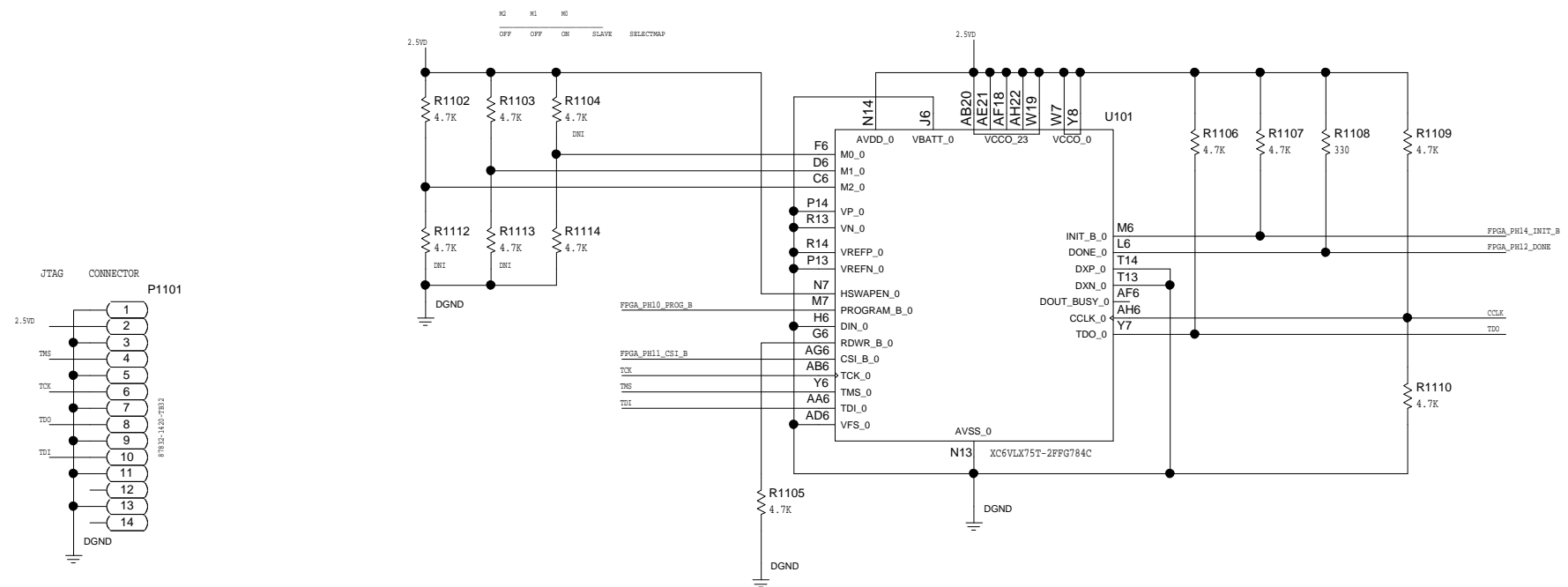
DIFF PAIR TRACE LENGTHS MUST BE MATCHED TO WITHIN 10 MILS
DIFF PAIR LANE LENGTHS MUST BE MATCHED TO WITHIN 100 MILS
TRACE LENGTHS BETWEEN R1006 AND FPGA MUST BE EQUAL IN LENGTH AND GEOMETRY



	SCHEMATIC			
	HADV6 <PRODUCT_1>	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
<small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.</small>	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 10 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FPGA CONFIGURATION

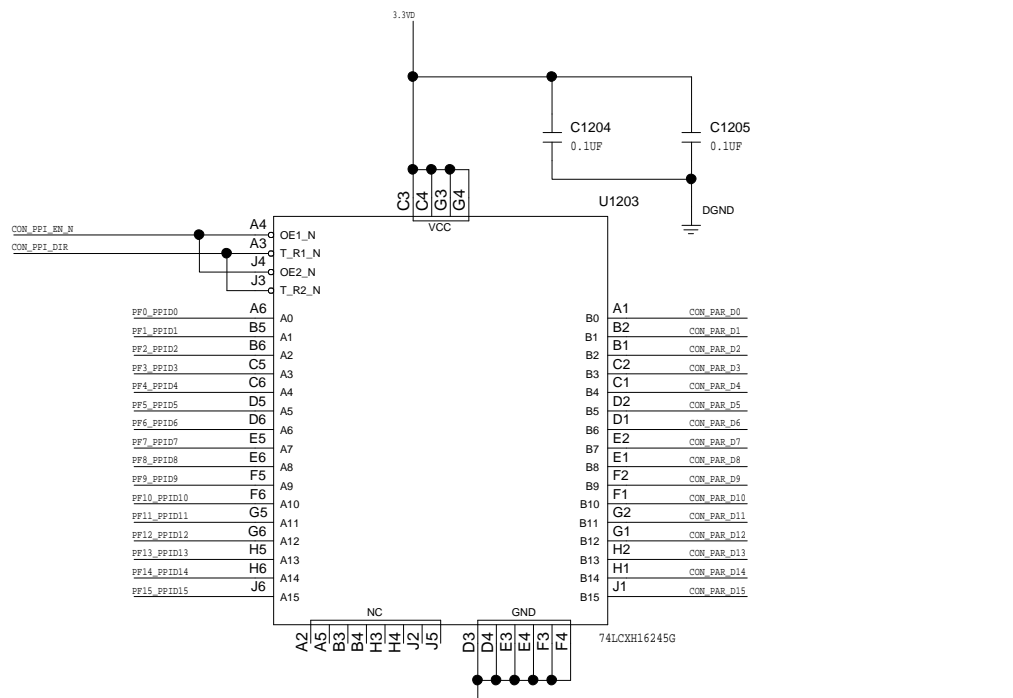
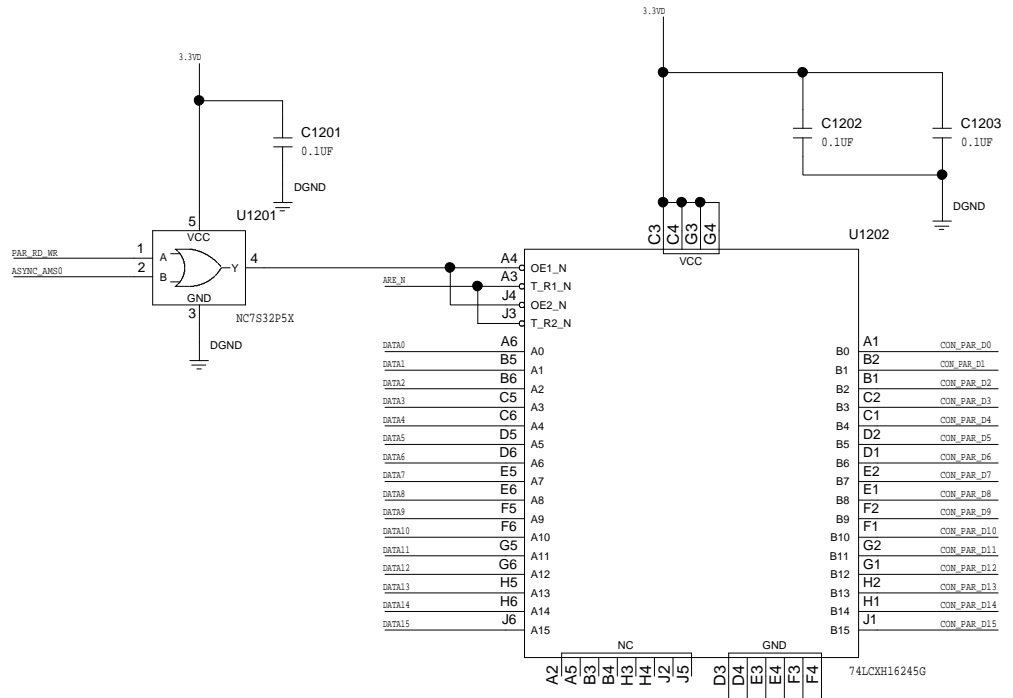
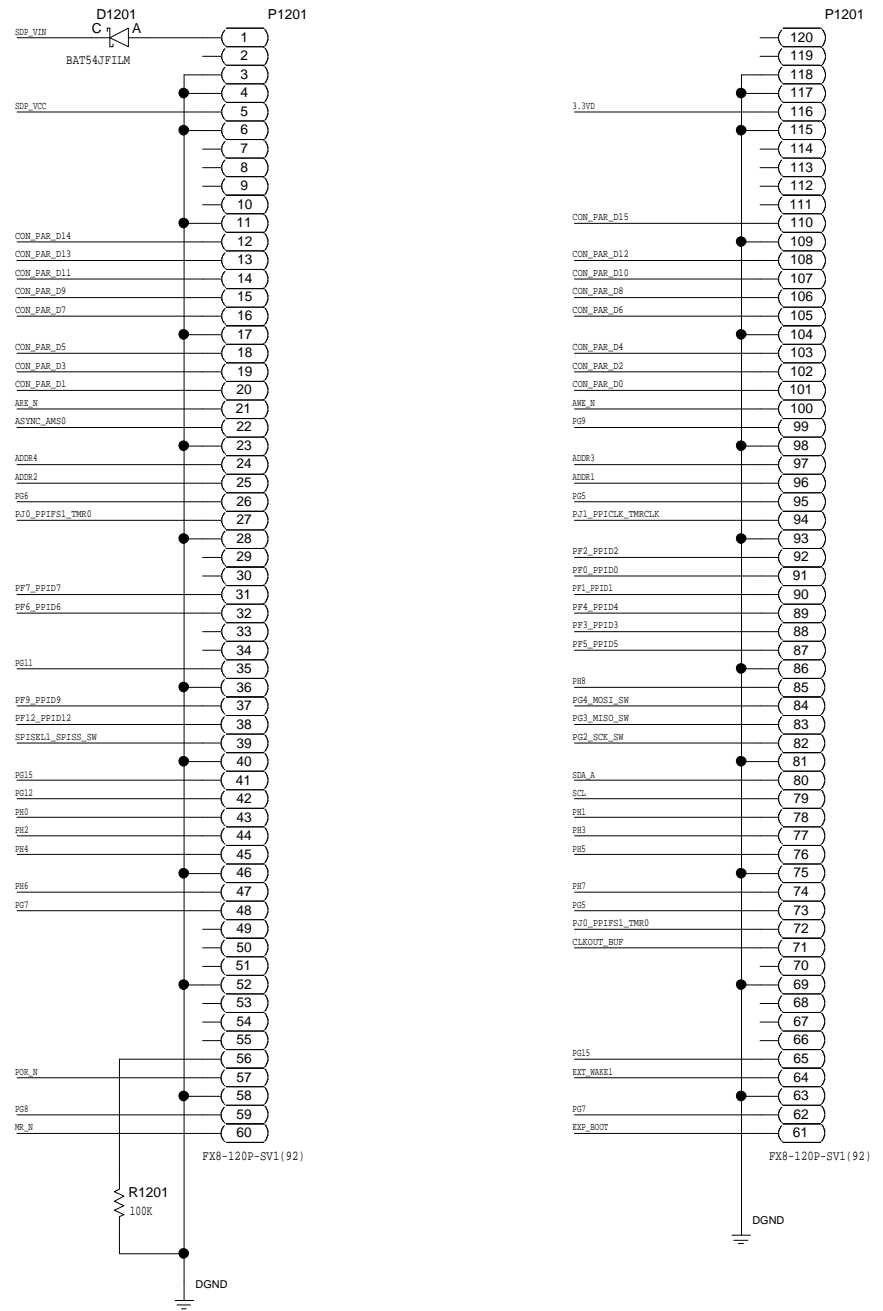


	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

SHEET 11 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

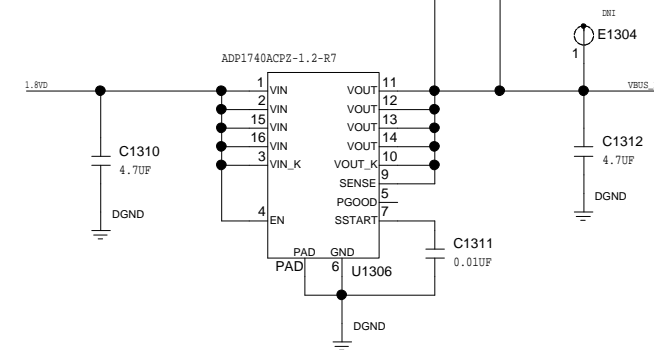
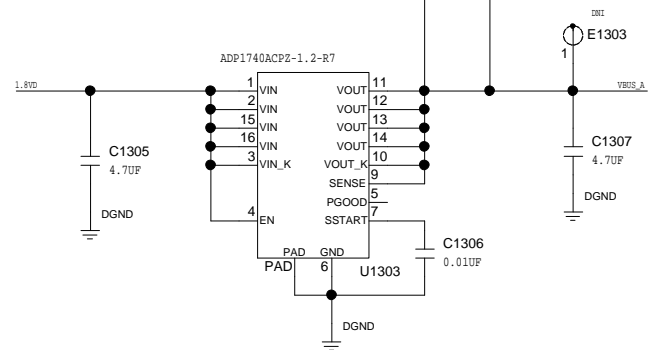
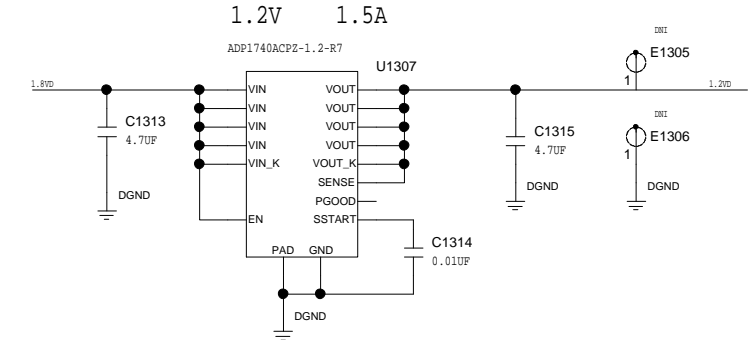
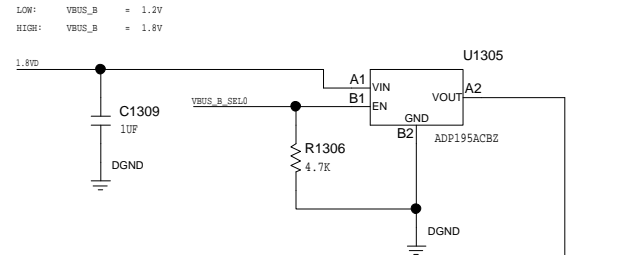
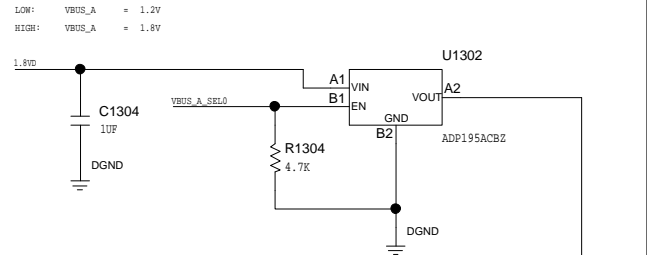
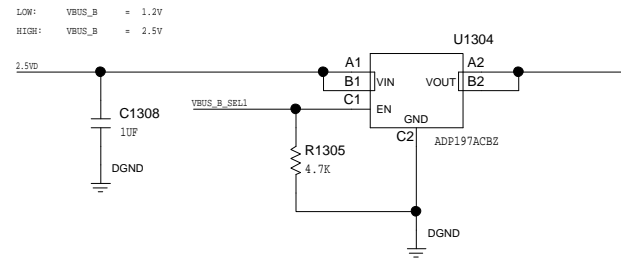
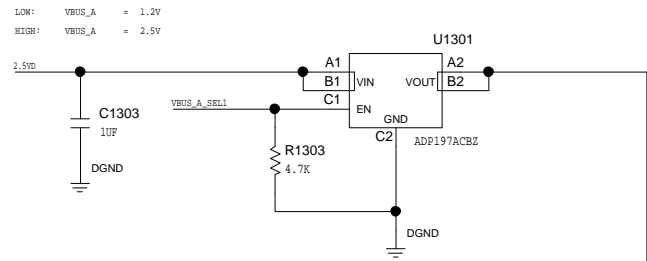
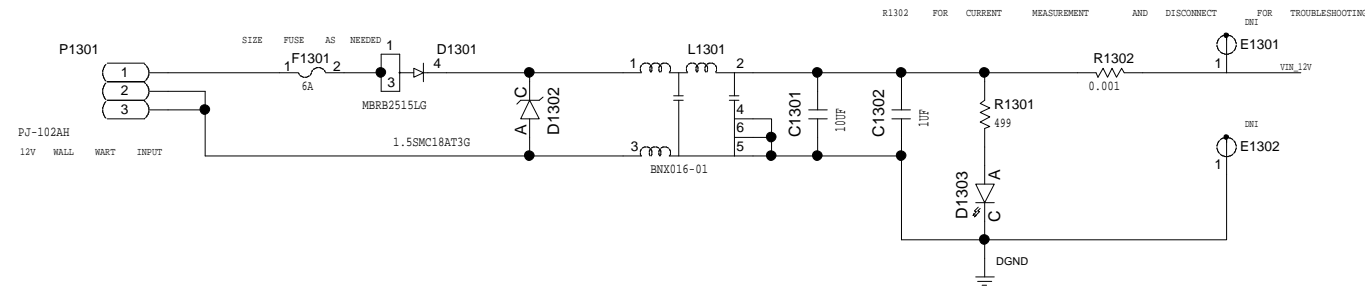
SDP CONNECTOR



<p>ANALOG DEVICES</p> <p><small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</small></p>	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 12 OF 17	

POWER SUPPLY INPUT AND CONTROLS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

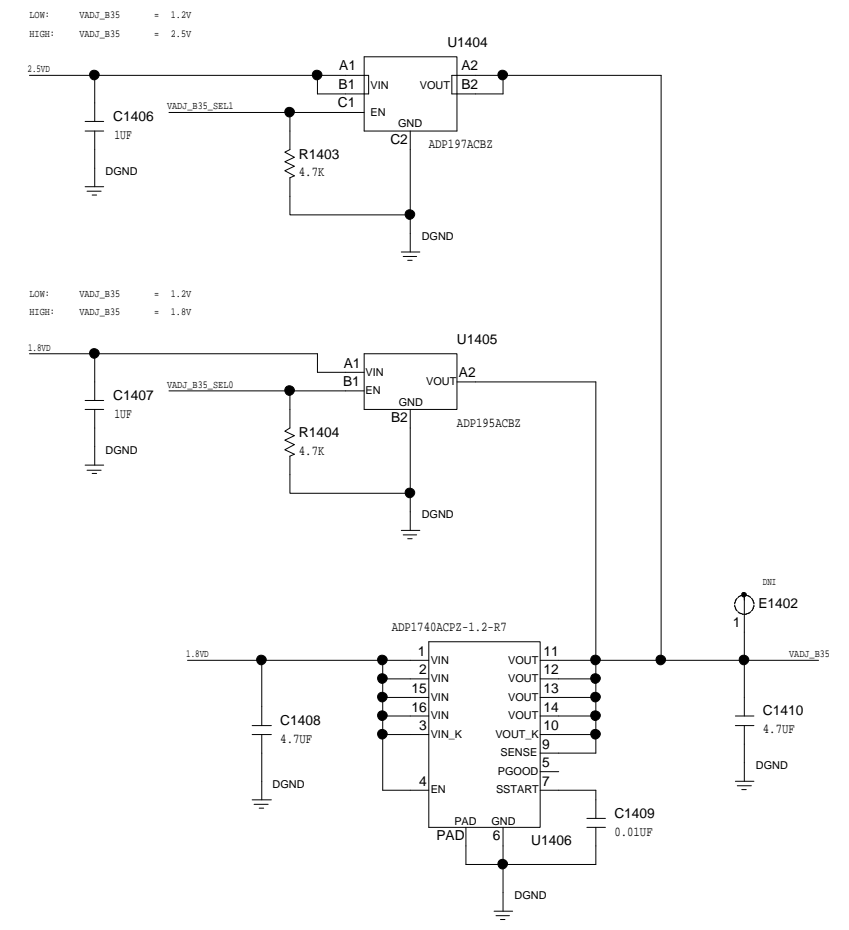
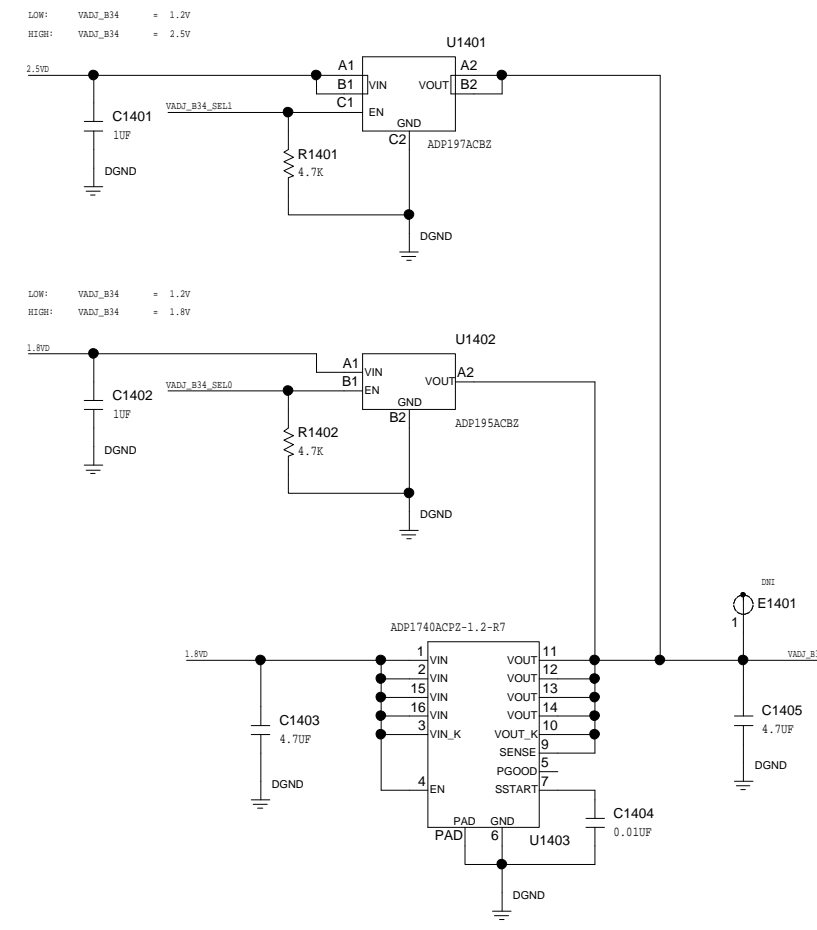


<p>ANALOG DEVICES</p> <p><small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN ANY MANNER THAT WOULD BE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.</small></p>	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

SHEET 13 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER SUPPLY CONTROLS

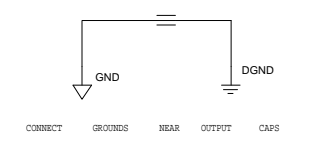
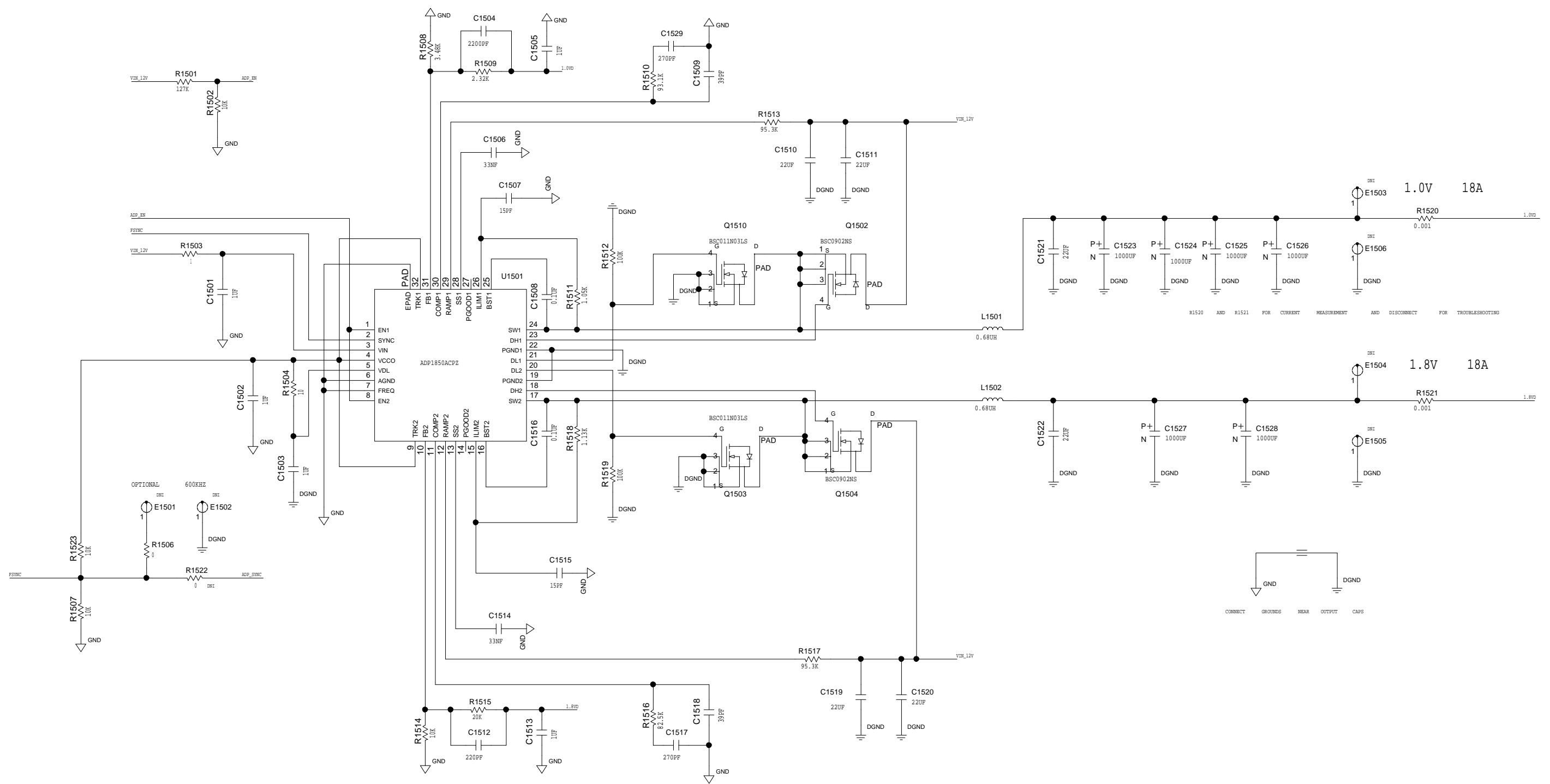


<p>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</p>	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

SHEET 14 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER SUPPLIES: 1.0VD, 1.8VD

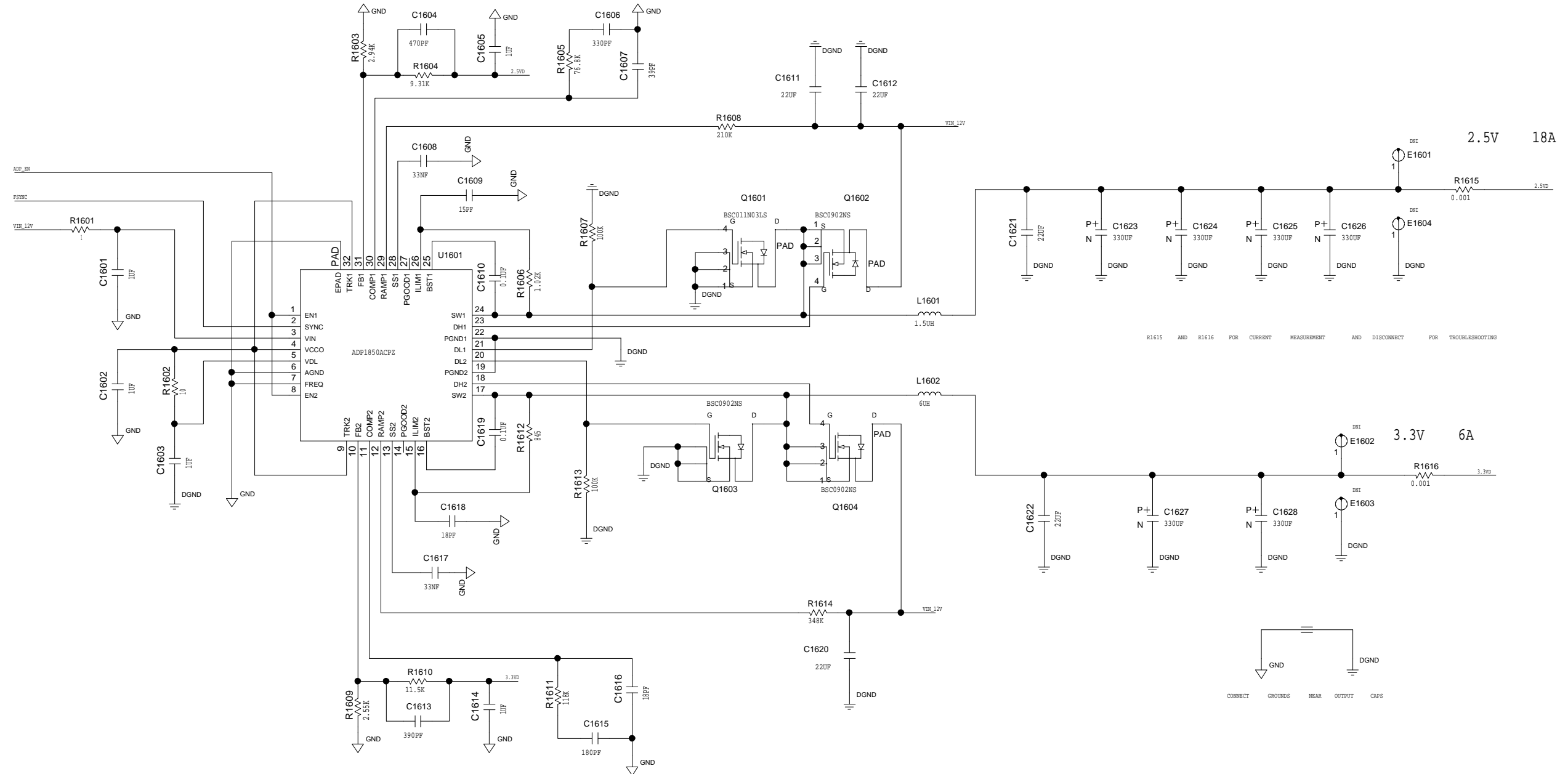


 <small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.</small>	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

SHEET 15 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER SUPPLIES: 2.5VD, 3.3VD

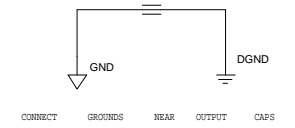
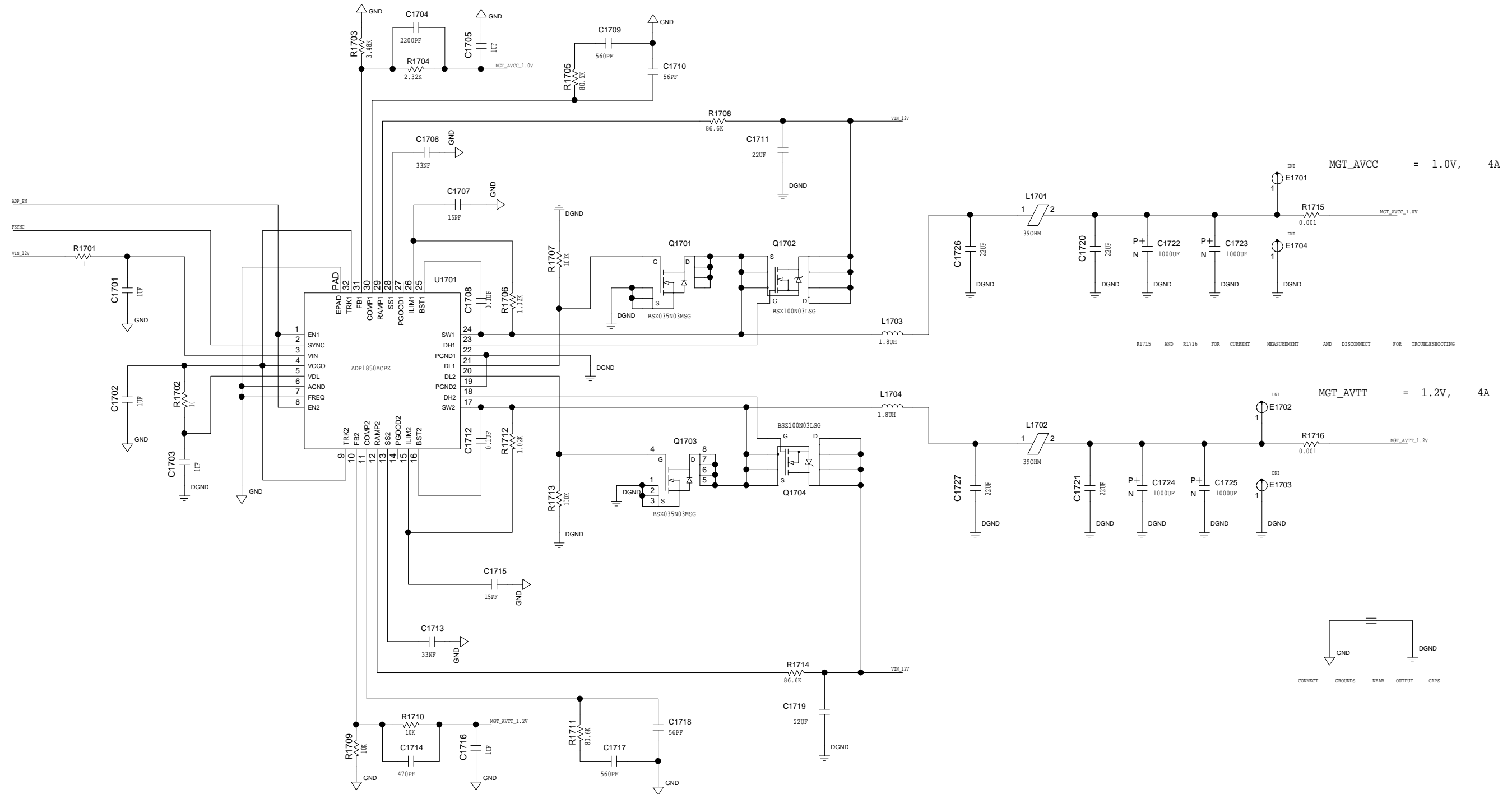


 <small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</small>	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>

SHEET 16 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

GTX POWER SUPPLIES



	SCHEMATIC		
	HADV6 <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 17 OF 17