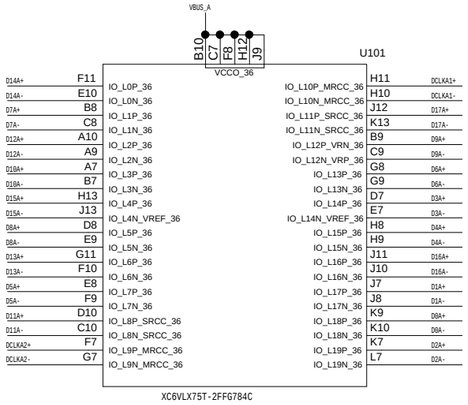
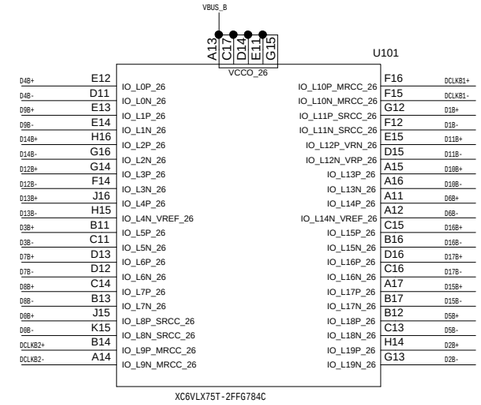
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1		APR-2011	

PARALLEL DATA BUS A AND B



DATA DIFF PAIRS CAN BE MOVED TO HELP ROUTING
DO NOT MOVE CLOCK DIFF PAIRS

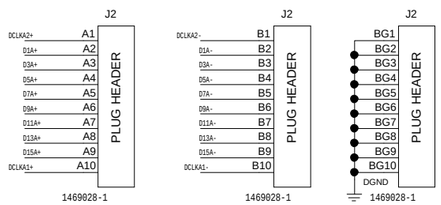


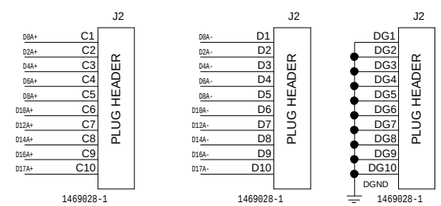
DATA DIFF PAIRS CAN BE MOVED TO HELP ROUTING
DO NOT MOVE CLOCK DIFF PAIRS

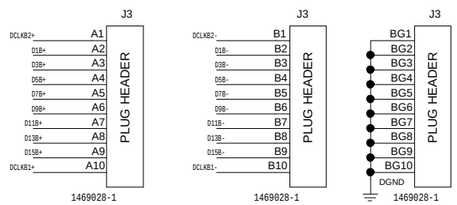
DIFF PAIR ROUTING LENGTHS MUST BE MATCHED TO WITHIN 50 MILS

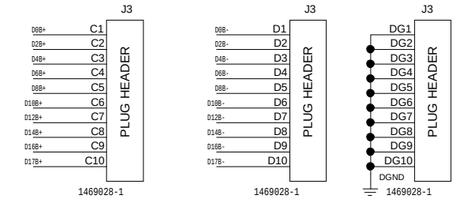
BUS ROUTING LENGTHS MUST BE MATCHED TO WITHIN 250 MILS

NOTE: J1 IS ON SHEET 10









HADV6-REVD

ANALOG DEVICES

SCHEMATIC

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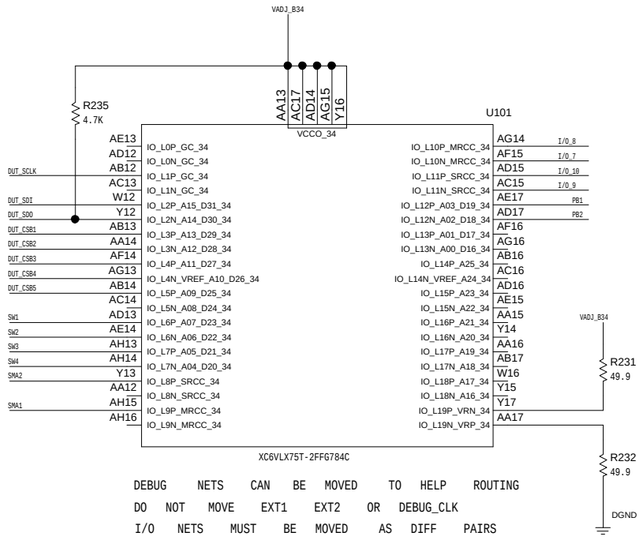
HADV6
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	.	D

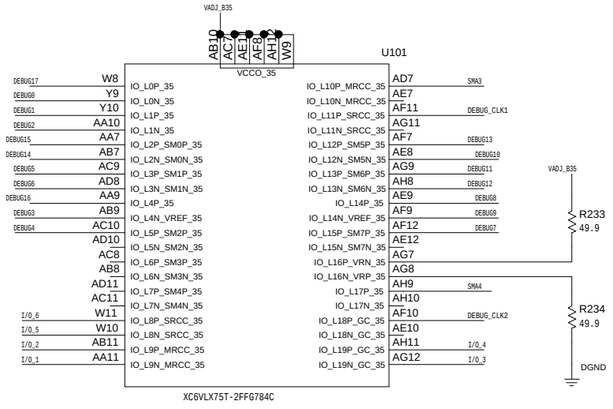
PTD ENGINEER	SIZE	SCALE	SHEET
<PTD_ENGINEER>	D	<SCALE>	1 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

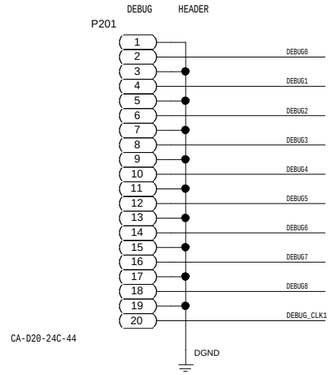
MISC. BANKS 34 AND 35



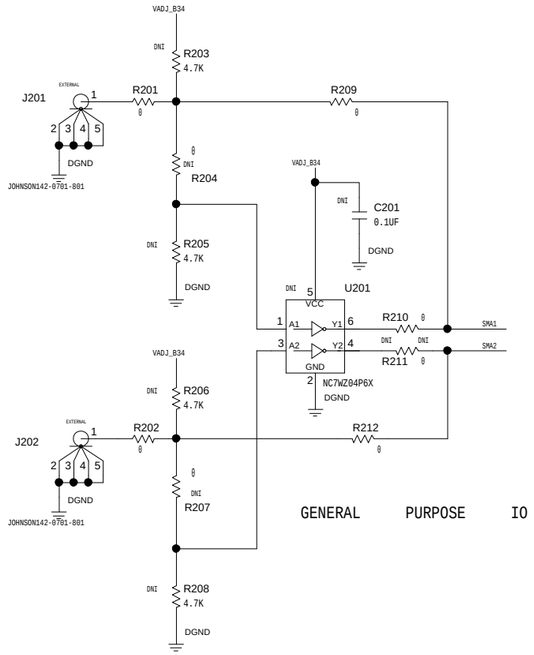
DEBUG NETS CAN BE MOVED TO HELP ROUTING
DO NOT MOVE EXT1 EXT2 OR DEBUG_CLK
I/O NETS MUST BE MOVED AS DIFF PAIRS



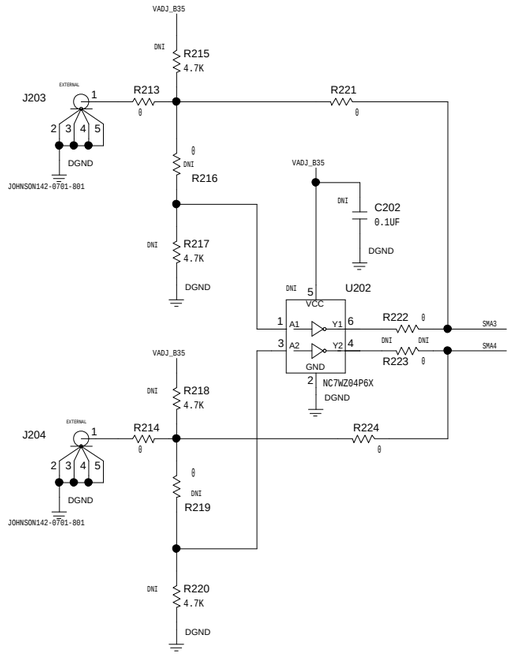
NETS CAN BE MOVED TO HELP ROUTING
I/O NETS MUST BE MOVED AS DIFF PAIRS

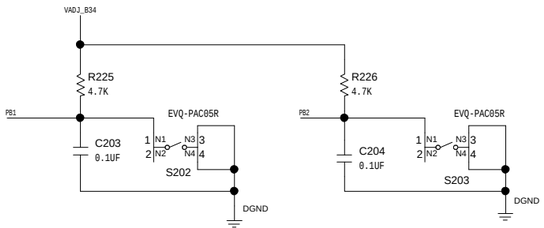


CA-D20-24C-44

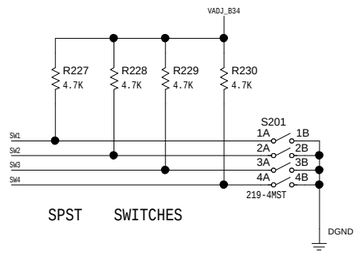


GENERAL PURPOSE IO

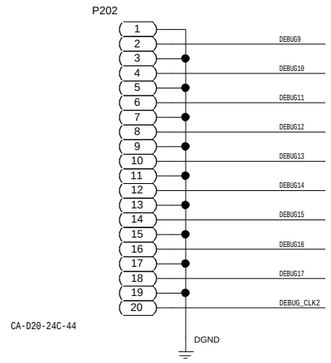




PUSH BUTTON SWITCHES



SPST SWITCHES



CA-D20-24C-44

ANALOG DEVICES	SCHEMATIC	
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	HADV6 <PRODUCT_1>	
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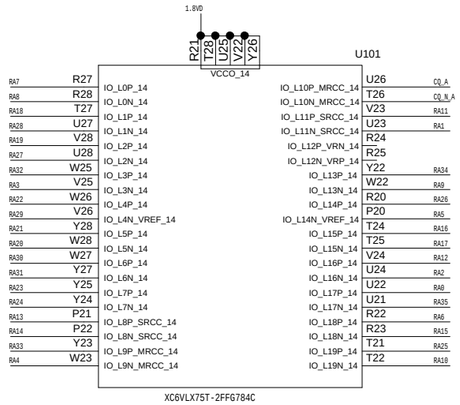
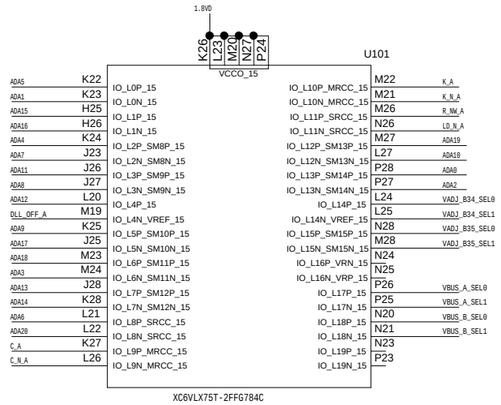
	PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE> SHEET 2 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

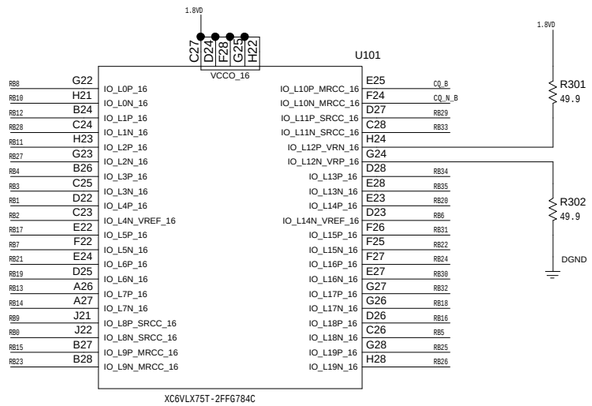
FPGA - SRAM INTERFACE AND BANK CONTROLS

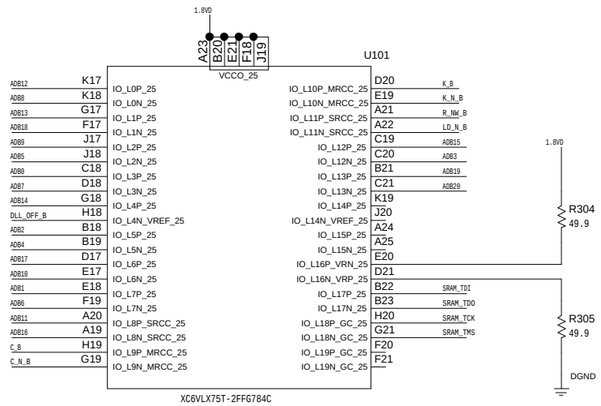




RA, RB AND AD LINES CAN BE MOVED WITHIN BANKS TO HELP ROUTING

ASK ENGINEER BEFORE MOVING ANY OTHER LINES





ANALOG DEVICES	SCHEMATIC	
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	HADV6 <PRODUCT_1>	
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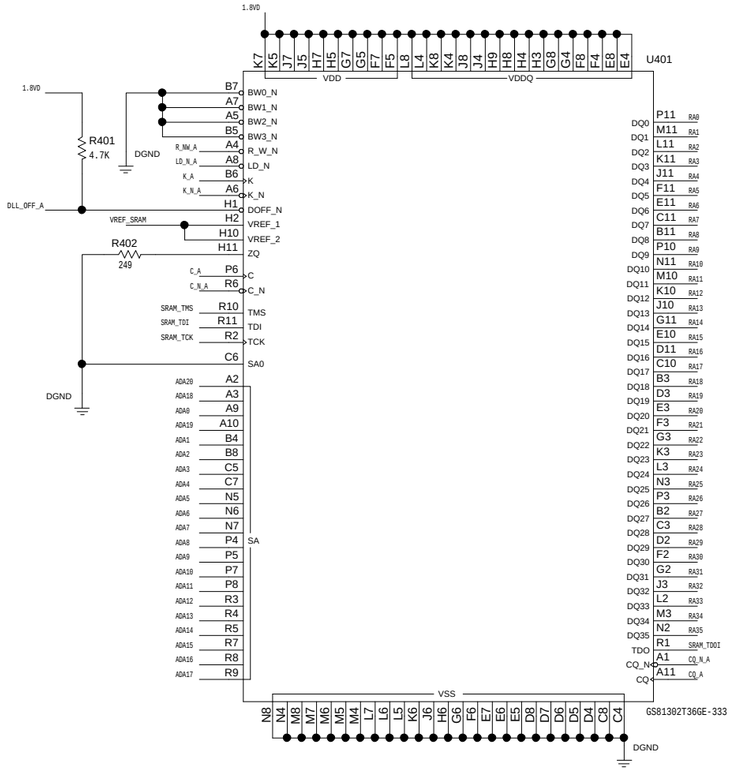
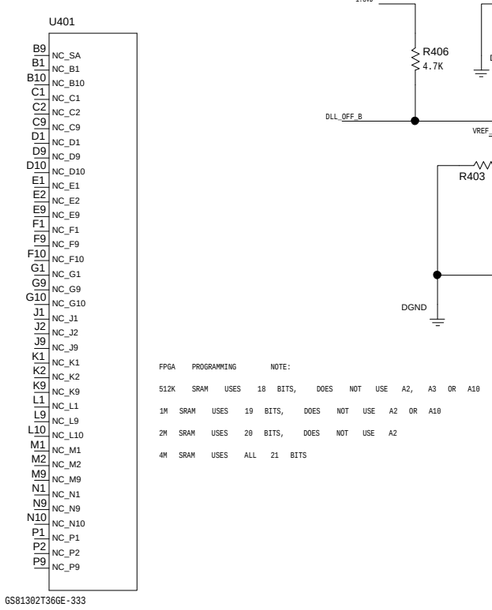
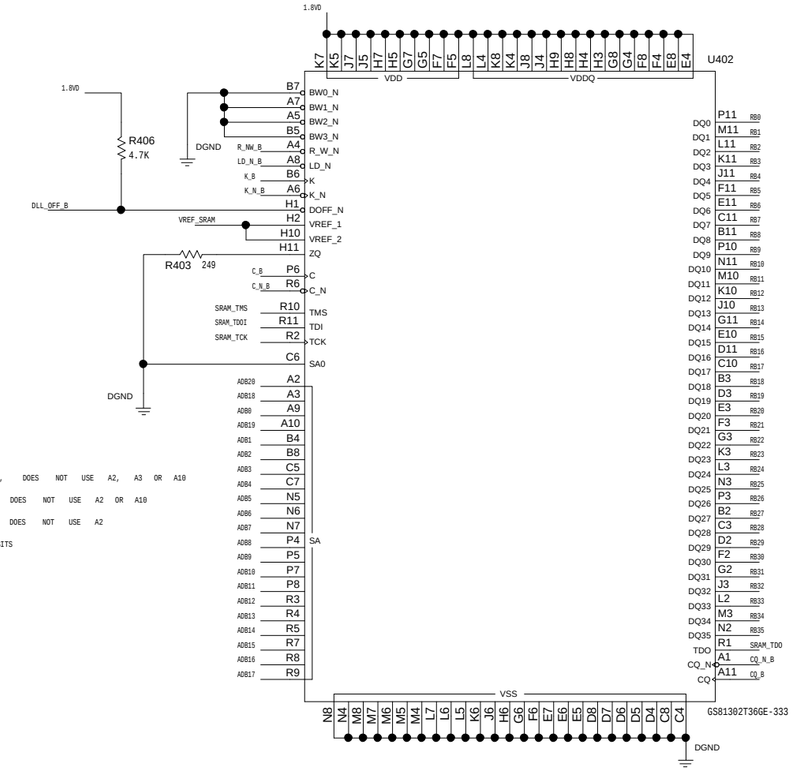
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE> / SHEET 3 OF 17

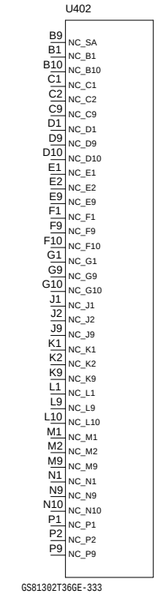
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

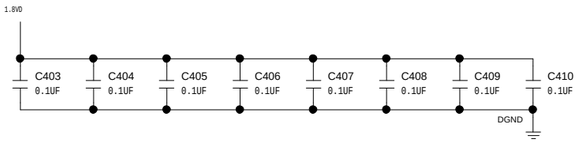
SRAM A AND B

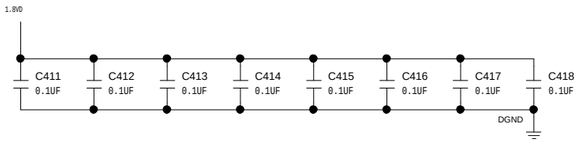


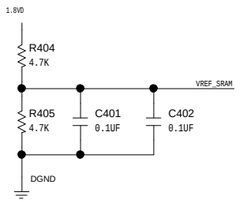












PLACE ONE SRAM CHIP ON TOP SIDE

PLACE THE OTHER SRAM CHIP ON BOTTOM SIDE

ADDRESS LINES ARE SHARED

K AND K_N LINES ARE SHARED

C AND C_N LINES ARE SHARED

ANALOG DEVICES

SCHEMATIC

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HADV6

<PRODUCT_1>

DESIGN VIEW <DESIGN_VIEW>

DRAWING NO. .

REV D

PTD ENGINEER <PTD_ENGINEER>

SIZE D

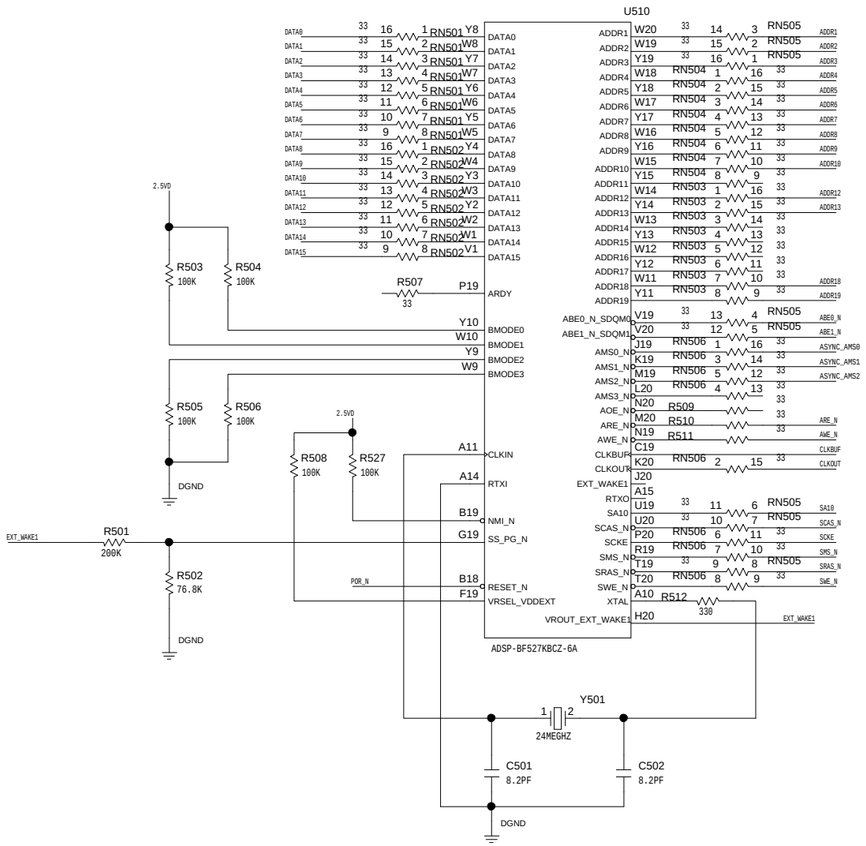
SCALE <SCALE>

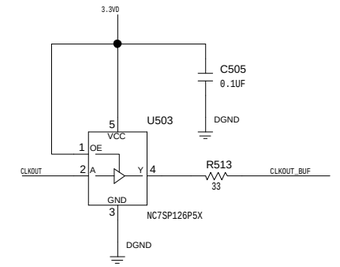
SHEET 4 OF 17

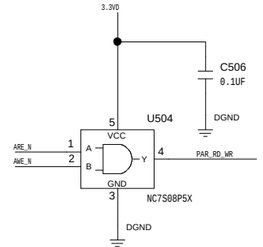
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

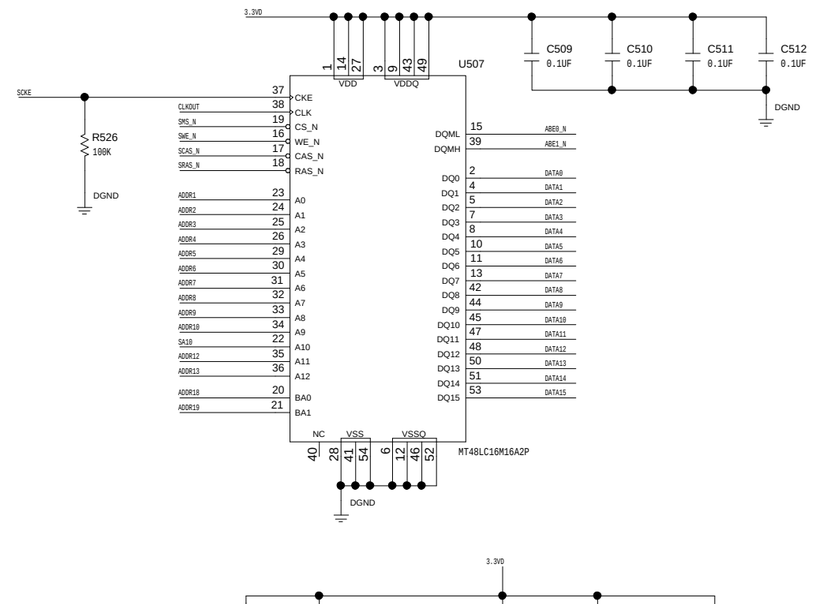
BF SDRAM

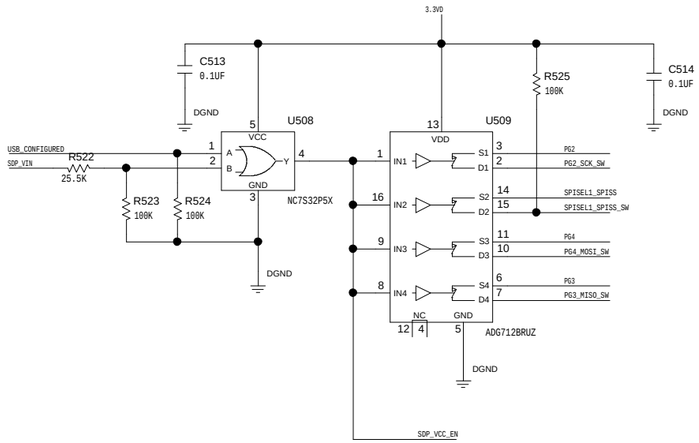
RESISTOR ARRAY SECTIONS MAY BE REASSIGNED AS NEEDED

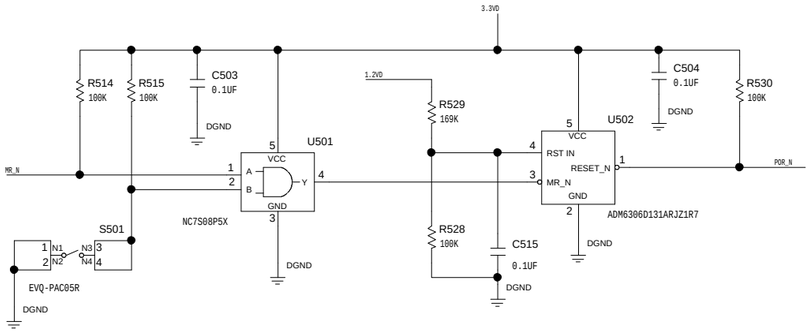


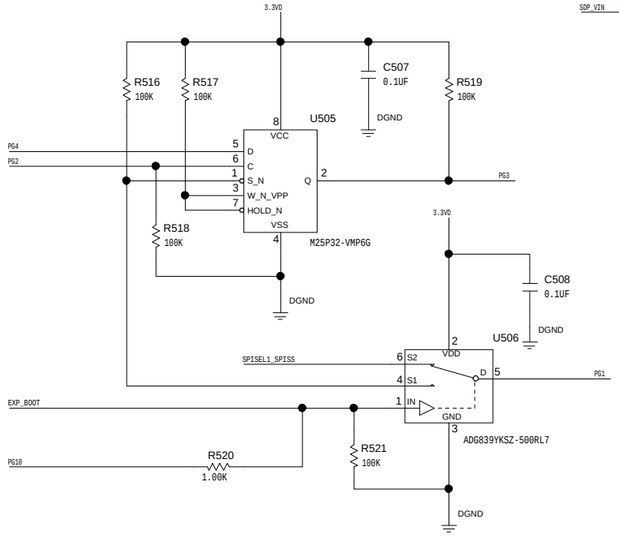












ANALOG DEVICES	SCHEMATIC
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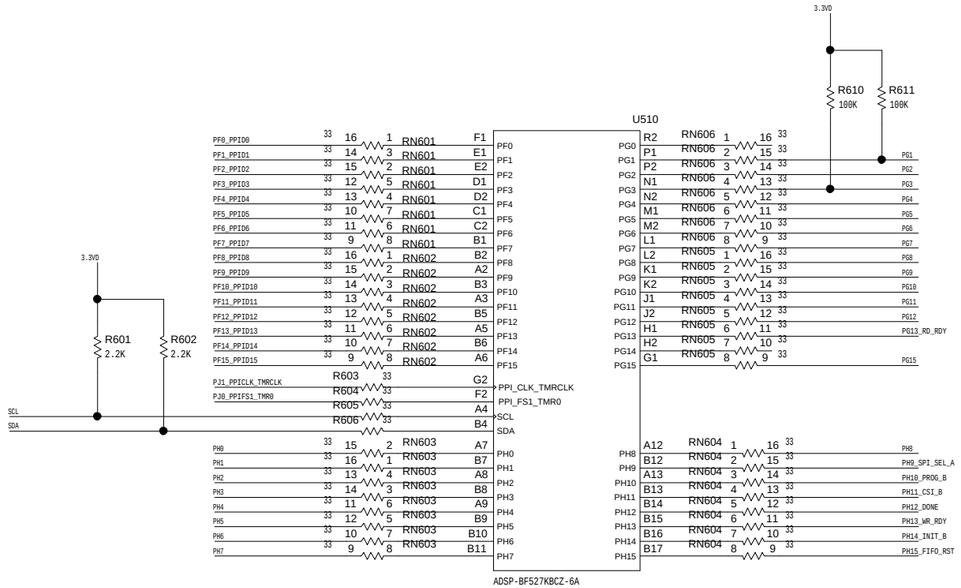
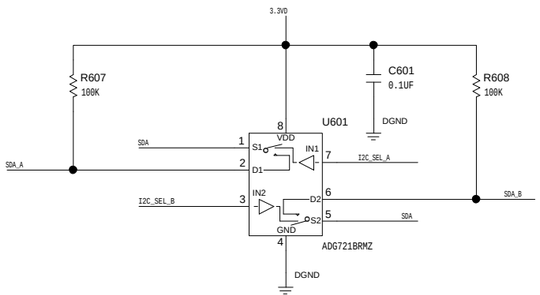
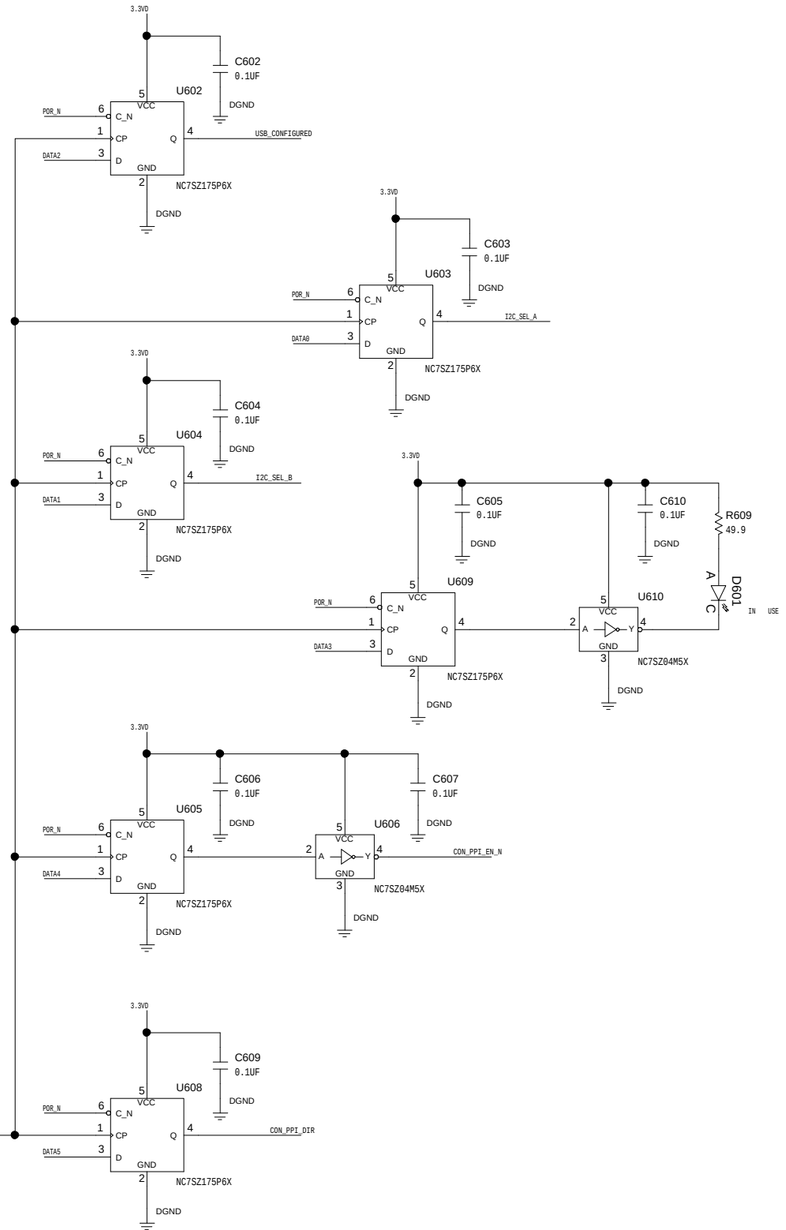
	<PRODUCT_1>
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. . / REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE> / SHEET 5 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

BF PPI







ANALOG DEVICES	SCHEMATIC		
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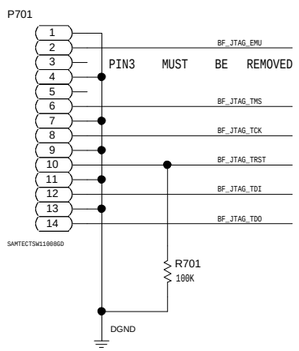
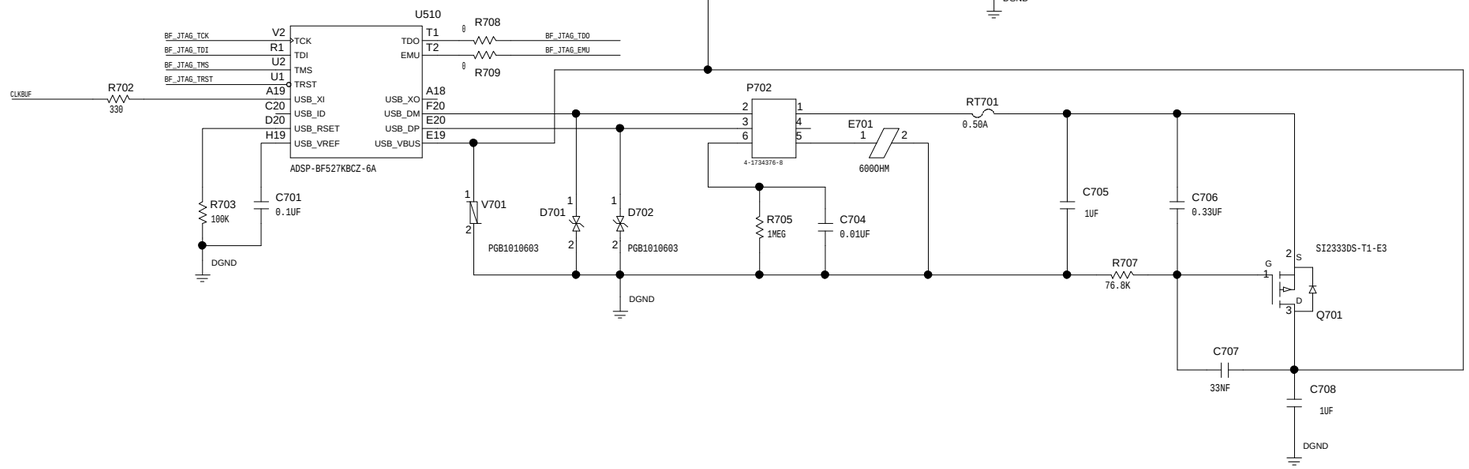
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. .	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 6 OF 17

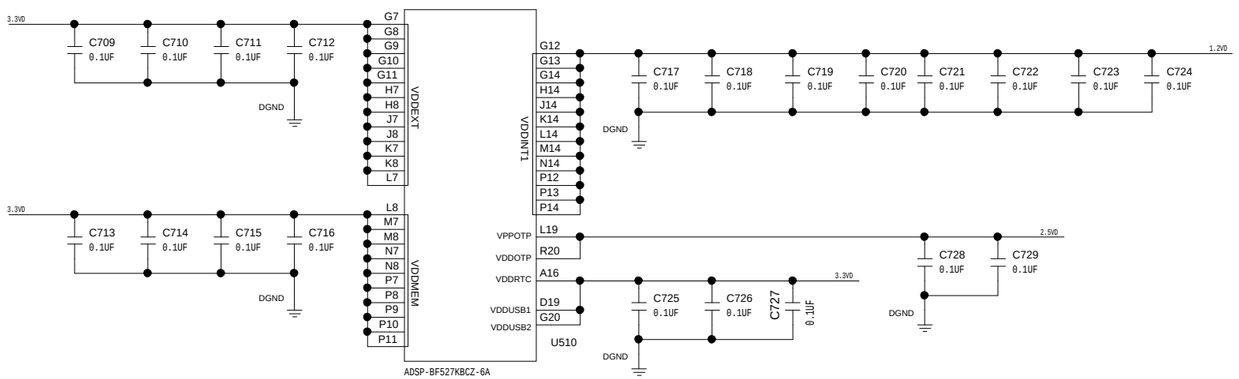
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

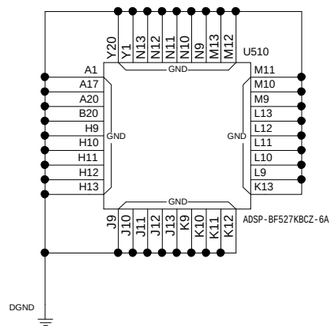
BF POWER,USB AND JTAG

BF JTAG CONNECTOR









ANALOG DEVICES	SCHEMATIC
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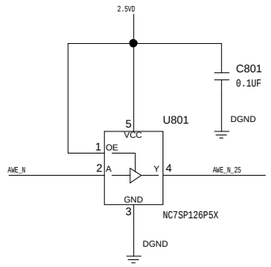
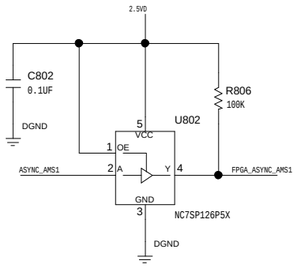
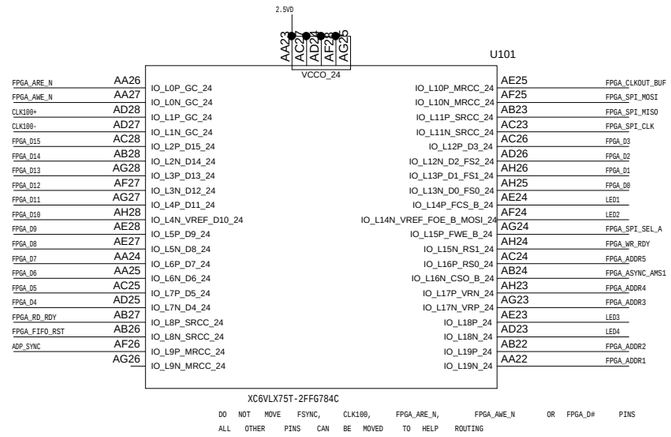
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. . REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE> SHEET 7 OF 17

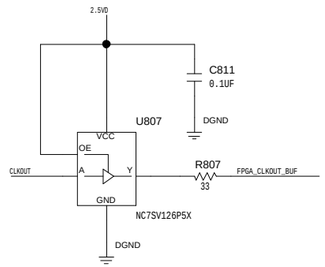
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

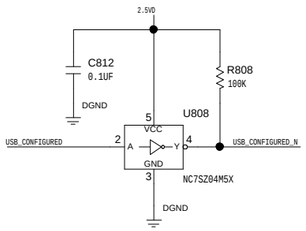
FPGA - BF INTERFACE, MISC

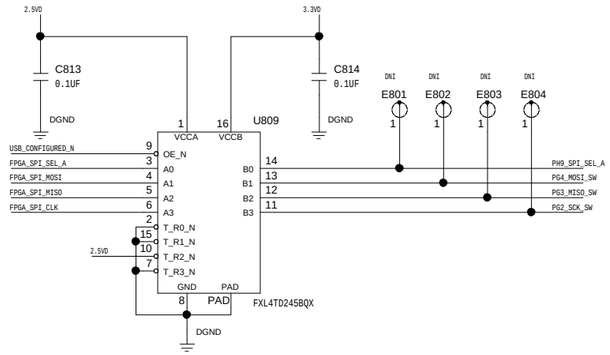


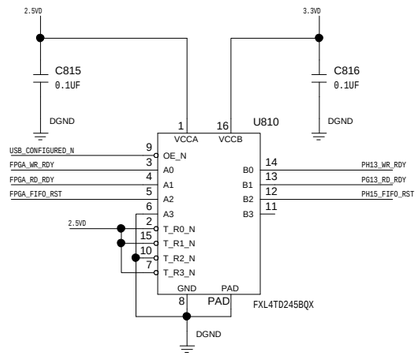


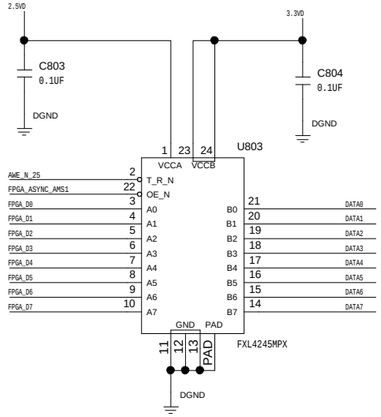


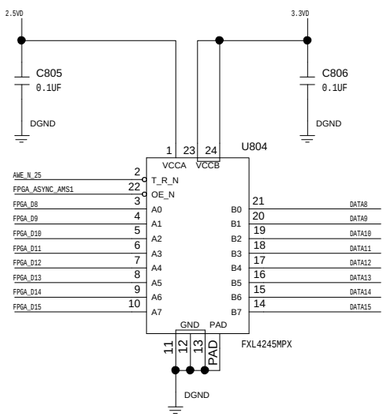


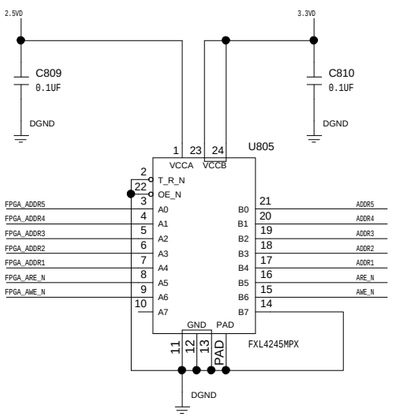


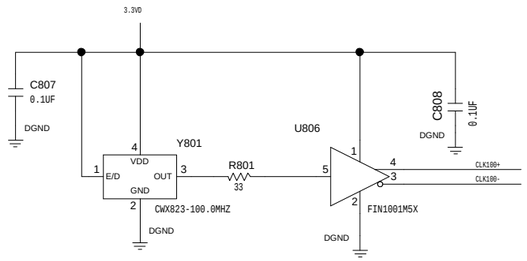


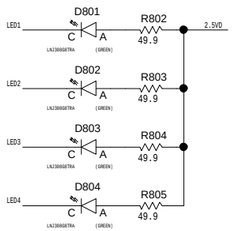












ANALOG DEVICES	SCHEMATIC		
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	HADV6 <PRODUCT_1>		
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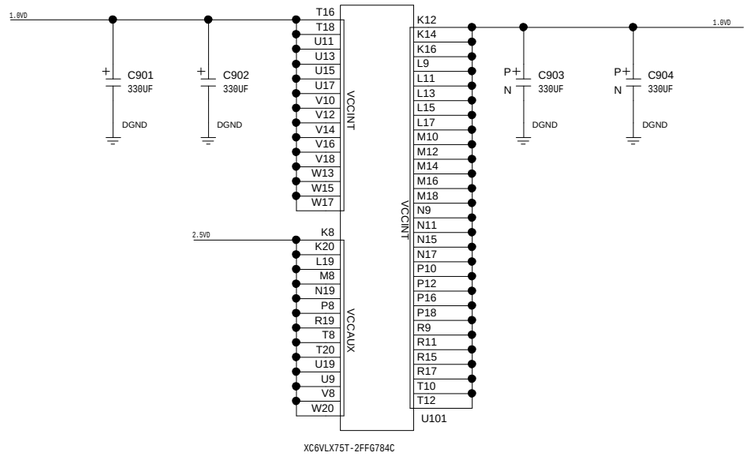
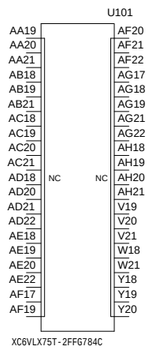
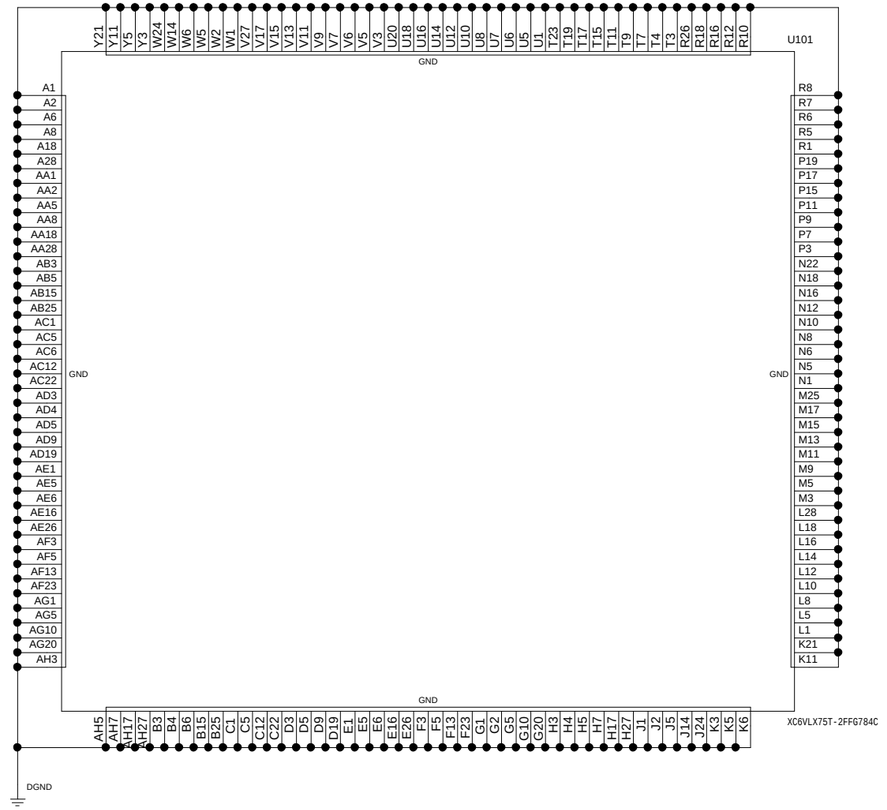
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 8 OF 17

FPGA POWER AND DECOUPLING

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED







ANALOG DEVICES

SCHEMATIC

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HADV6

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REV 0

PTD ENGINEER <PTD_ENGINEER>

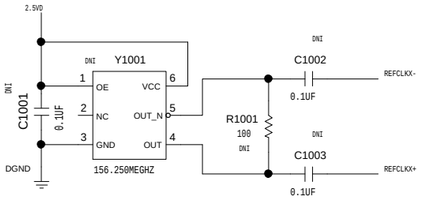
SIZE D

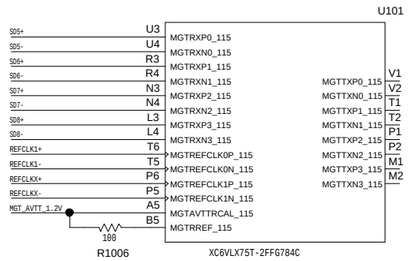
SCALE <SCALE>

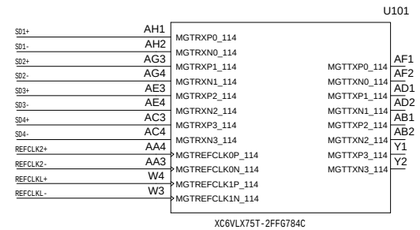
SHEET 9 OF 17

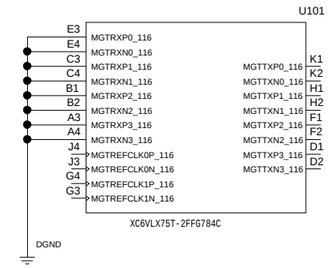
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

GTX CONNECTIONS









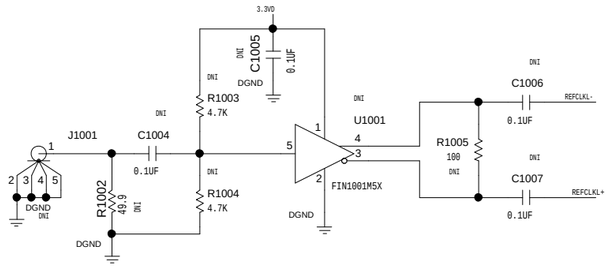
SD DIFF PAIRS MAY BE MOVED TO HELP ROUTING

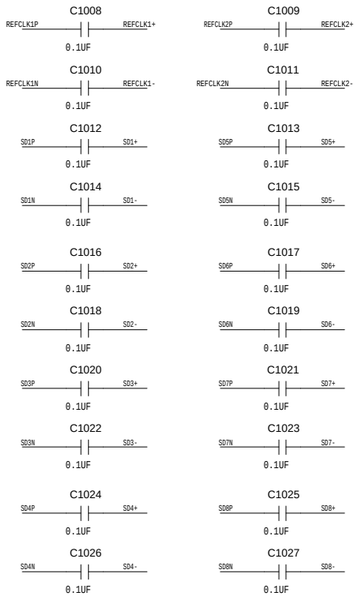
DO NOT CROSS BANKS

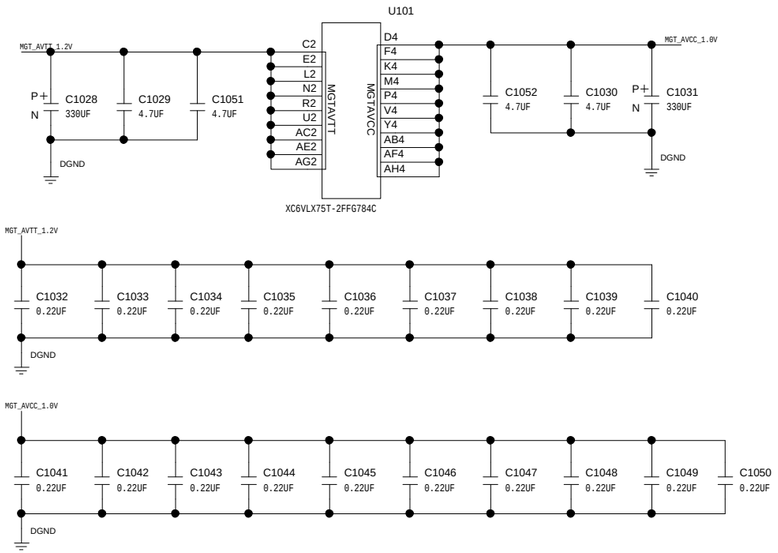
DIFF PAIR TRACE LENGTHS MUST BE MATCHED TO WITHIN 10 MILS

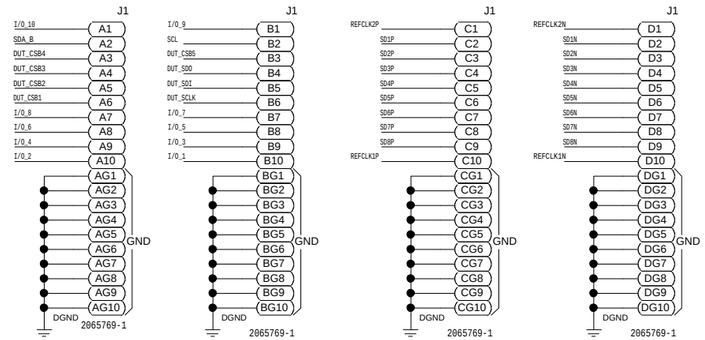
DIFF PAIR LANE LENGTHS MUST BE MATCHED TO WITHIN 100 MILS

TRACE LENGTHS BETWEEN R1006 AND FPGA MUST BE EQUAL IN LENGTH AND GEOMETRY









ANALOG DEVICES	SCHEMATIC	
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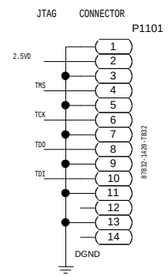
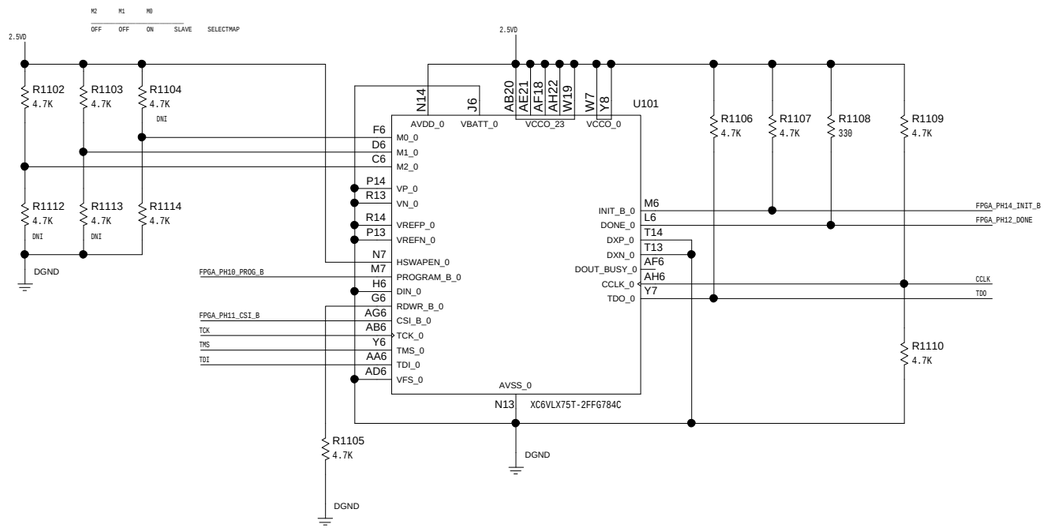
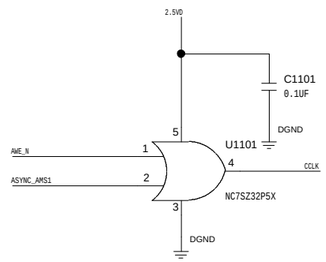
	PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE> SHEET 10 OF 17

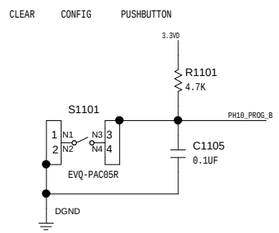
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

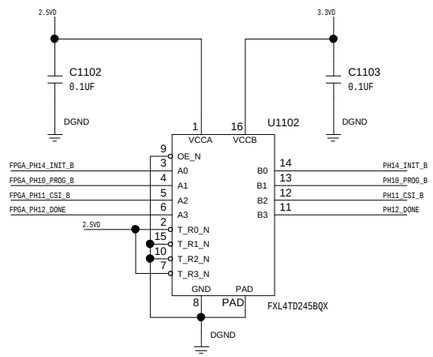
FPGA CONFIGURATION

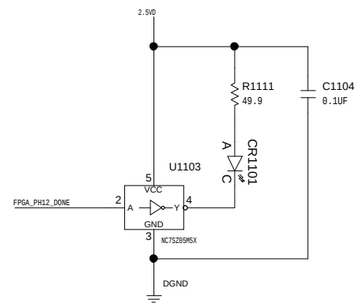












ANALOG DEVICES	SCHEMATIC
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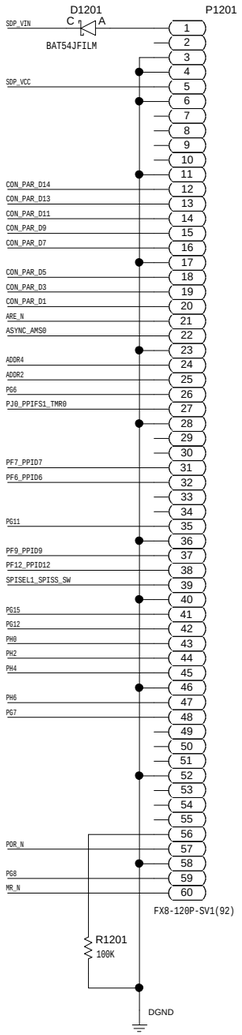
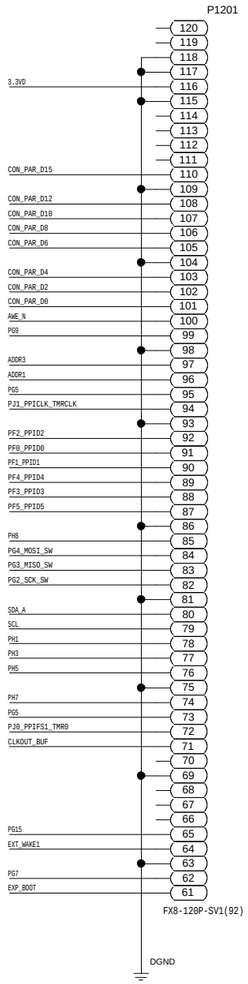
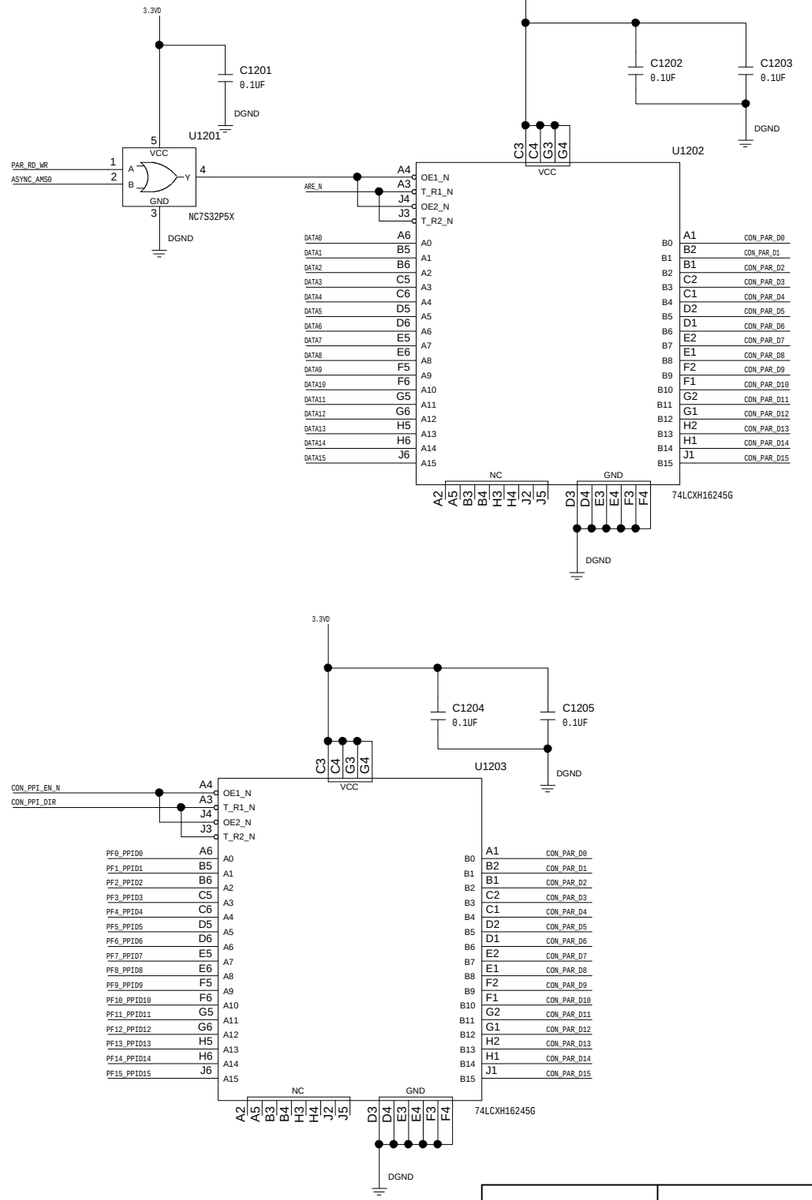
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

SDP CONNECTOR







ANALOG DEVICES

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DRAWING NO.
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PTD ENGINEER
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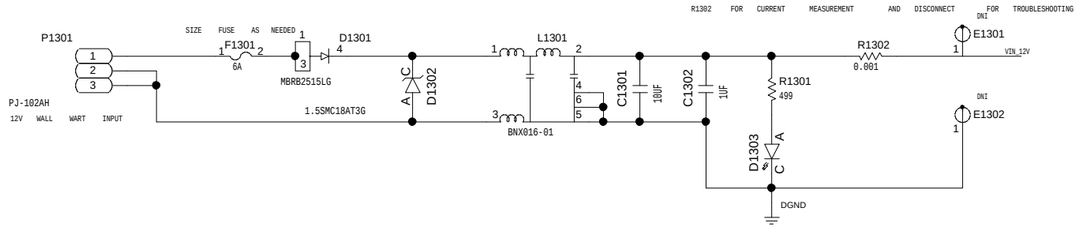
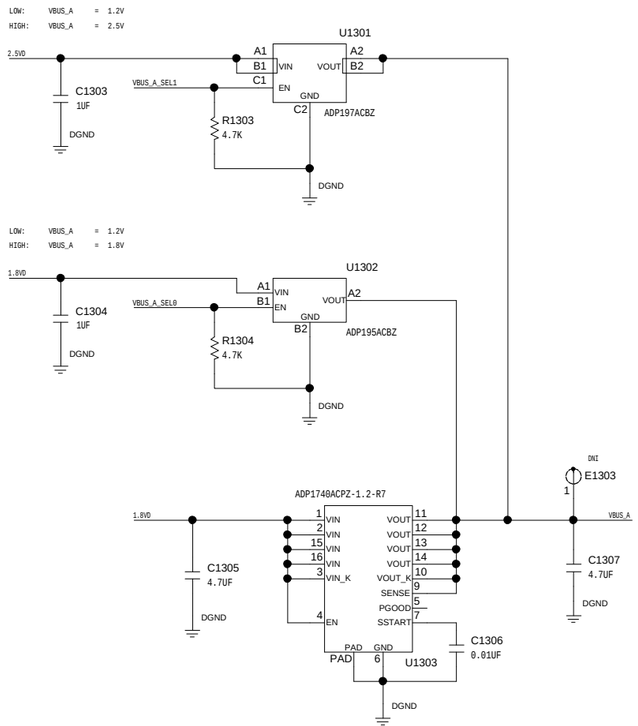
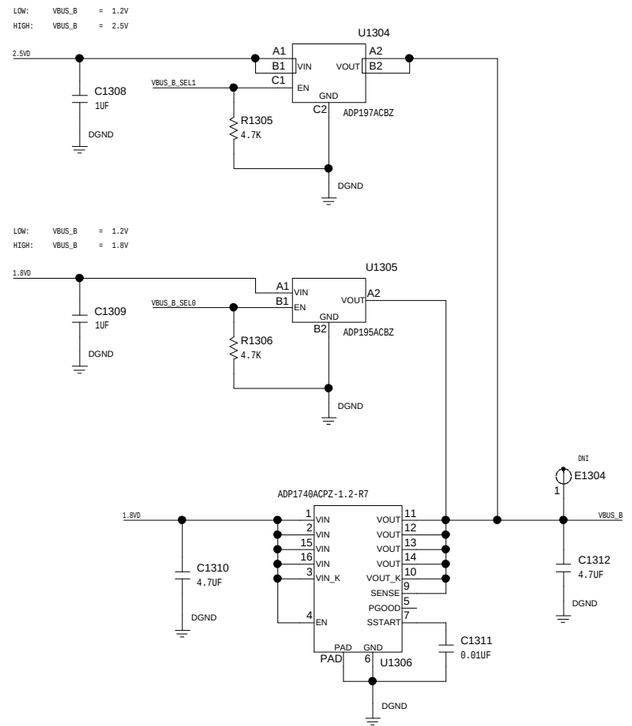
SHEET 12 OF 17

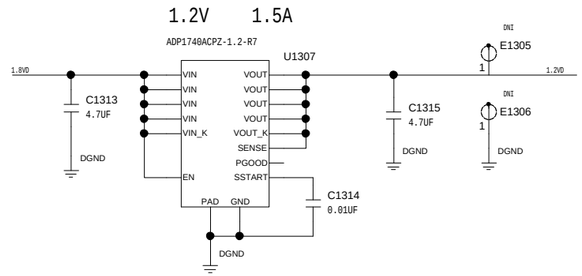
POWER SUPPLY INPUT AND CONTROLS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED









ANALOG DEVICES	SCHEMATIC
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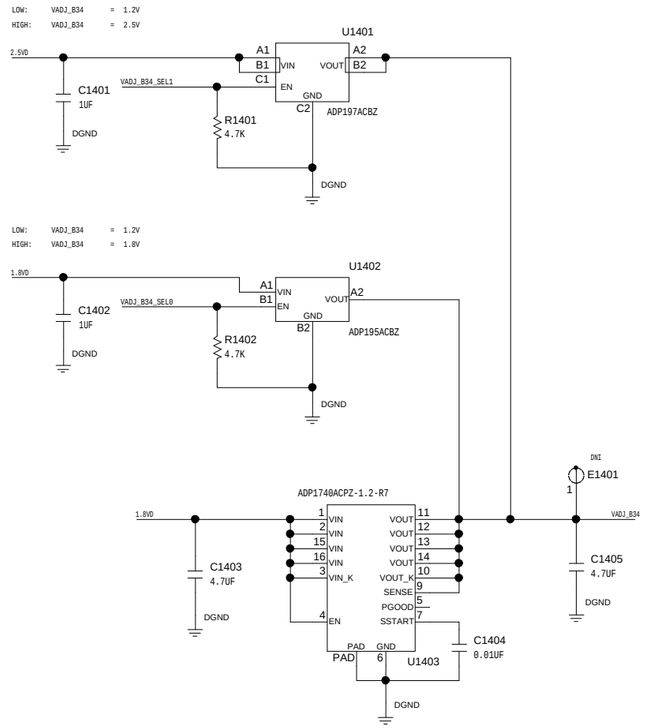
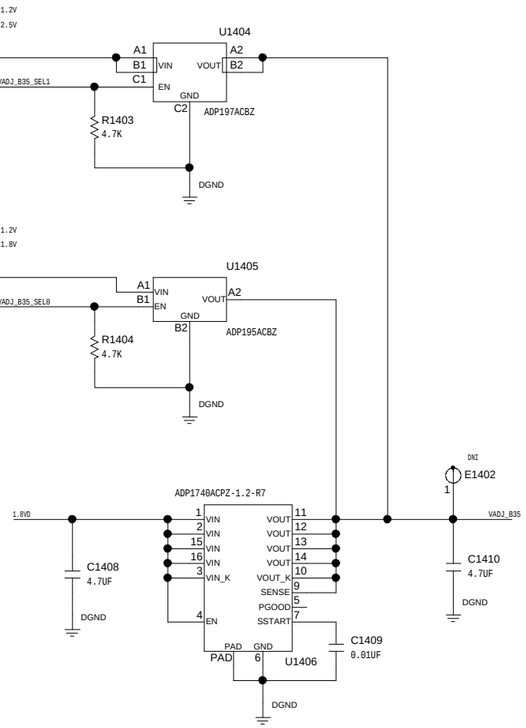
PTD ENGINEER: <PTD_ENGINEER>	SIZE: D SCALE: <SCALE> SHEET 13 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER SUPPLY CONTROLS





ANALOG DEVICES

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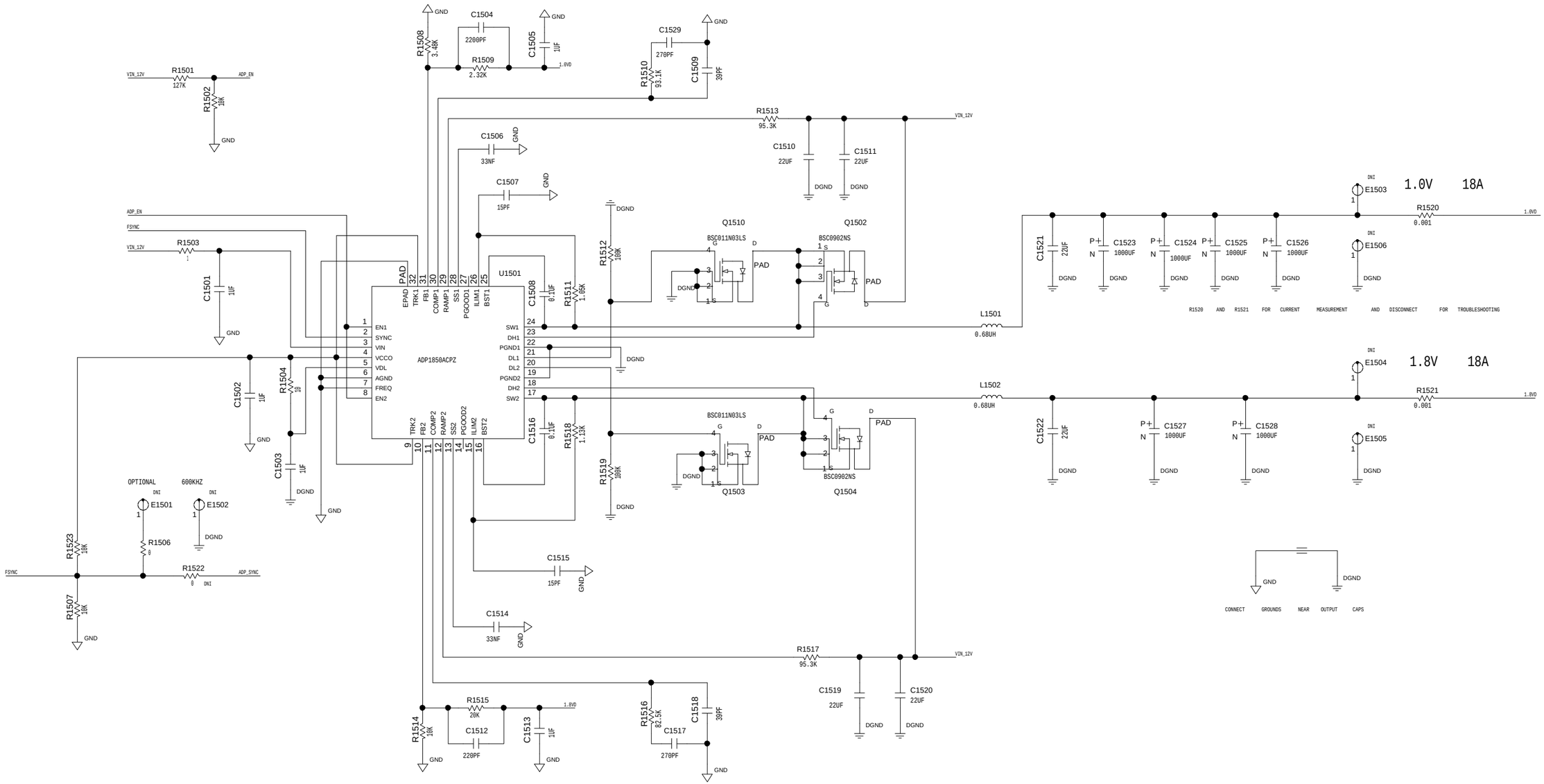
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. .	REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 14 OF 17

POWER SUPPLIES: 1.0VD, 1.8VD

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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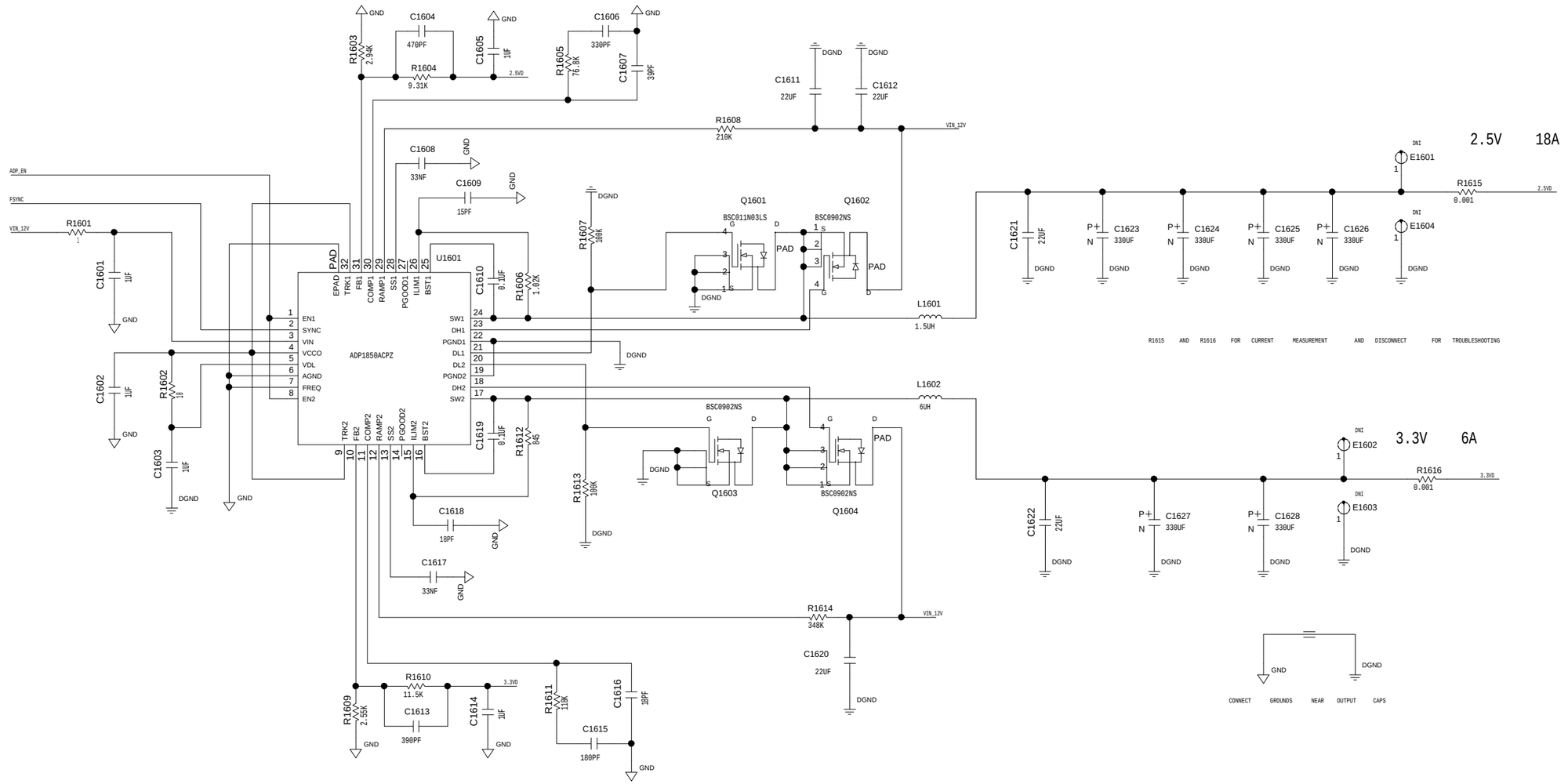
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 15 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER SUPPLIES: 2.5VD, 3.3VD



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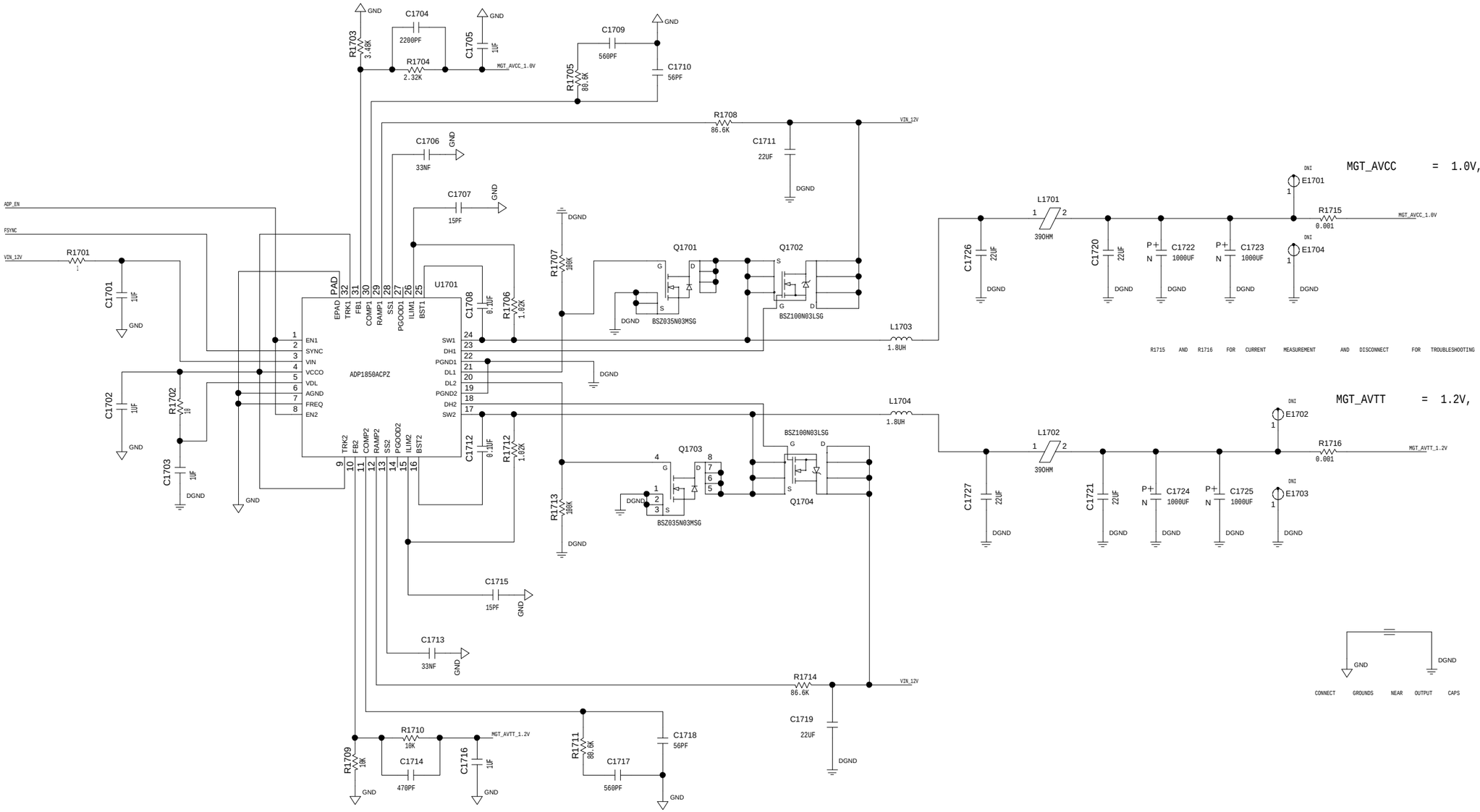
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 16 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

GTX POWER SUPPLIES



MGT_AVCC = 1.0V, 4A

R1715 AND R1716 FOR CURRENT MEASUREMENT AND DISCONNECT FOR TROUBLESHOOTING

MGT_AVTT = 1.2V, 4A

GND DGND

CONNECT GROUNDS NEAR OUTPUT CAPS

ANALOG DEVICES

SCHEMATIC

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<PRODUCT_1>

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. .	REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 17 OF 17