This version (13 May 2019 22:41) was *approved* by Tony Meyers [https://ez.analog.com/members/TonyM].
The Previously approved version (/resources/eval/hmcad15xx?rev=1557779915) (13 May 2019 22:38) is available.

EVAL01-HMCAD15xx User Guide

High Speed, Low Power, Analog-to-Digital Converter Evaluation Kit

Features

* Full featured evaluation board for the HMCAD1511, and HMCAD1520 ADCs

* Simple USB (Universal Serial Bus) computer interface

* Single-ended SMA connectors for clock inputs and analog inputs

* ADC obtains power from Xilinx SP-601 FMC connector

Evaluation Kit Contents

* Eval01-HMCAD1511/EVAL01-HMCAD1520 EZ-Board®

* SP-601 Xilinx development board with EasyStack

* EasySuite software and User Manual: https://www.analog.com/en/design-center/evaluation-hardware-and-software/a-d-converter-evaluation-software.html [https://www.analog.com/en/design-center/evaluation-hardware-and-software/a-d-converter-evaluation-software.html]

Equipment Needed

* Clock source

* Signal source

* PC capable of running EasySuite software

General Description

This user guide describes the physical components of the EVAL01-HMCAD1511/EVAL01-HMCAD1520 EZ-Boards®. These boards are a part of the EKIT01-HMCAD1511/EKIT01-HMCAD1520 evaluation kits. The kits consist of an EZ-Board field-programmable gate array (FPGA) mezzanine card (FMC) daughter board, a Xilinx® FMC SP601 development mother board, and the EasySuite software. Refer to the EasySuite software user guide for installation of the EasySuite software. The EasyStack firmware is loaded on the Xilinx development board, which enables configuration of the analog-to-digital converter (ADC) and capturing of data from the ADC. The EKIT01-HMCAD1511/EKIT01-HMCAD1520 features power monitoring and supply voltage adjustment.

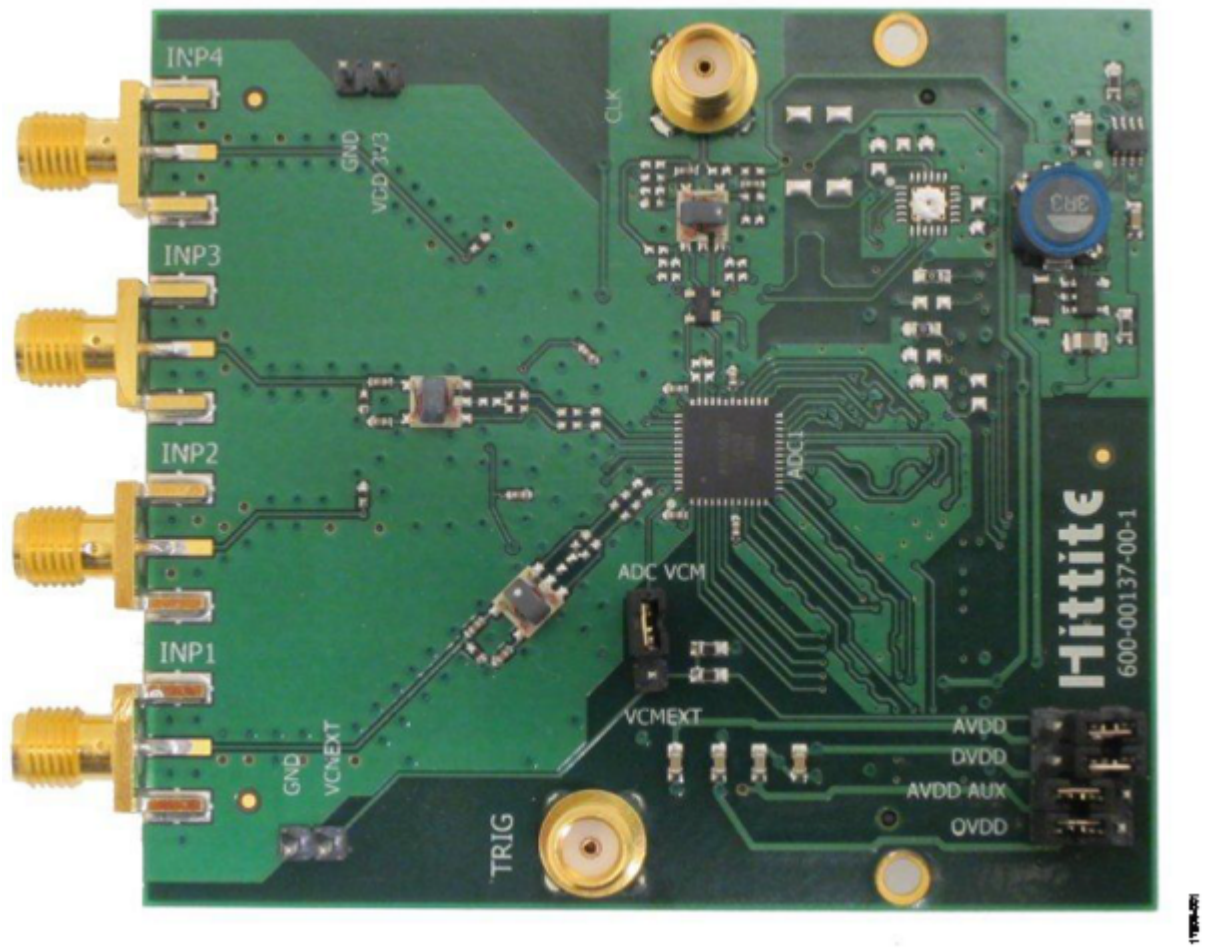

Figure 1. EVAL01-HMCAD15XX Hittite EasyBoard(TM)

Analog Inputs

Signal Quality

The quality of the input signal is the most important criterion to obtain accurate measurement results. The user must also take the following into consideration:

- Select a signal source with low noise and low phase noise, such as the Agilent E8663.
- Apply a bandpass filter between the signal source and the EZ-Board RF input (INP1 through INP4). A bandpass filter is required to obtain sufficiently low white noise levels and to reduce harmonic components from the signal source. The TTE filter series Q56T or KC4T is recommended. Ensure that large magnetic cores are used in the filters to avoid nonlinearity due to core saturation. Alternative vendors are K (kelvin (unit of temperature, not degrees))&L Microwave and Allen Avionics. The input signal can be checked with a spectrum analyzer after filtering to ensure that noise and harmonic levels are significantly better than the theoretical contribution from the ADC

Analog Input Network

The input network of the EZ-Board is configured with an ac-coupled balun. This balun converts the single-ended input to a differential input for the ADC (see Figure 3).

Clock Generation

The clock inputs on the HMCAD15XX ADCs accept CMOS, LVDS, LVPECL and sine wave inputs. Connect a clock source to the SMA connector named CLK. The EasyBoard clock network is an AC coupled balun configuration with a 20MHz lower frequency limit. The network will accept a single ended sine wave or square wave input.

For best possible performance it is very important that the clock source have low jitter. Poor jitter performance will directly result in reduced SNR. The SNR contribution from jitter is given by equation (1) assuming a full scale input signal at frequency, FIN, and TRMS-jitter, measured in second Root-Mean-Square.

$$SNR = -20 \times \log\left(2\pi \times F_{IN} \times T_{RMS}\right)$$

One can see that a 1ps clock jitter with a 25 MHz (megahertz) full scale input results in an additional SNR component of 76 dBc (decibels relative to the carrier). Because of this the clock signal should be treated with the same care as the analog inputs to the ADC.

Trig Input

This connector is directly routed to a general input/output pin on the FPGA. It can be used to apply an external trigger.

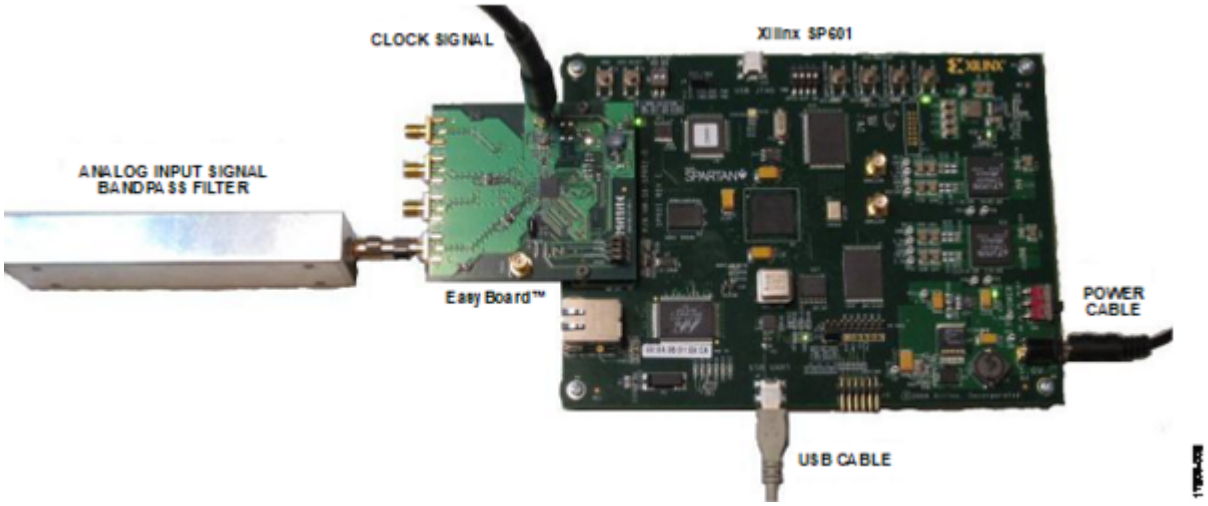

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Figure 2. Hardware Configuration (click on enlarge)

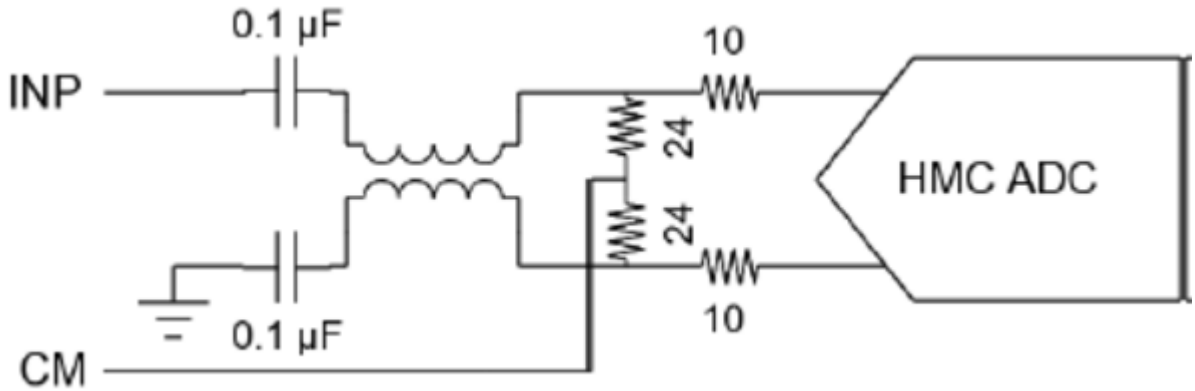

Figure 3. Default Analog Input Network

Jumpers and Connectors

Power Domains

JP4 and JP5 in lower right corner (see Figure 9) must be set to enable power for all power domains to the converter. One jumper must be present on each row, either to the right or the left. Setting the jumper to the right includes that power domain in the built-in current measurement feature. Setting the jumper to the left bypasses the current measurement for that domain.

All the power domains are on the 1.8 V (volt) power supply. The domains are separated on the board so that it is possible to measure the current consumption individually for each power domain on the chip. The domains are as follows:

- AVDD is the analog power domain and includes all power consumption in the ADC cores.
- DVDD is the digital power domain and includes power consumption in the digital block and the low voltage differential signaling (LVDS) input/output drivers.
- AVDD_AUX is the power domain for the reference circuit.
- OVDD is the domain for the input/output ring on the pads inside the chip. OVDD effectively only drives the configuration serial peripheral interface (SPI (Serial Peripheral Interface)) signals.

Common Mode

JP1 in Figure 9 selects the source for common mode drive. The source is the common mode level for the differential input signals. If the jumper is placed in the top position, the common mode is driven by the common mode output of the ADC. The drive strength of this output is programmable from the configuration software. See the HMCAD1511/ HMCAD1520 data sheet for details regarding the drive strength. If the jumper is placed in the lower position, the common mode is set by two on-board 51 Ω resistors between the 1.8 V (volt) supply and ground. It is possible to override this common mode externally by connecting a voltage source to the terminal port JP2 in the lower left corner.

3.3 V Supply Outlet

Terminal JP5 provides a 3.3 V (volt) supply outlet. This supply originates from the power converters on the mother board such as the SP601. It can drive a load up to 5 A. JP5 can be used as a power supply for an external crystal oscillator, which can be used as a clock source.

FMC Connector

The FMC connector J1 is located on the backside of the board. Connect J1 with the FMC connector on the Xilinx mother board.

Special Features

Power Monitoring

U4 is a power monitoring chip. U4 can measure the current consumption and voltage level from the ADC. See the Power Domains section for details about measuring different power domains on the ADC. If all jumpers on JP4 and JP5 are placed to the right, the total power consumption of the chip is measured.

The EasySuite software controls and collects data from the monitoring chip.

If the power measurement gives unexpected results, try bypassing the OVDD domain from the power measurement circuit.

Supply Voltage Level

The supply voltage level for the ADC can be adjusted through the EasySuite software. U12 is a digital potentiometer which can adjust the supply level between 1.7 V (volt) and 2.0 V (volt). Refer to the EasySuite software user guide for an explanation of how to set the supply voltage.

Evaluation Board Schematics and Artwork

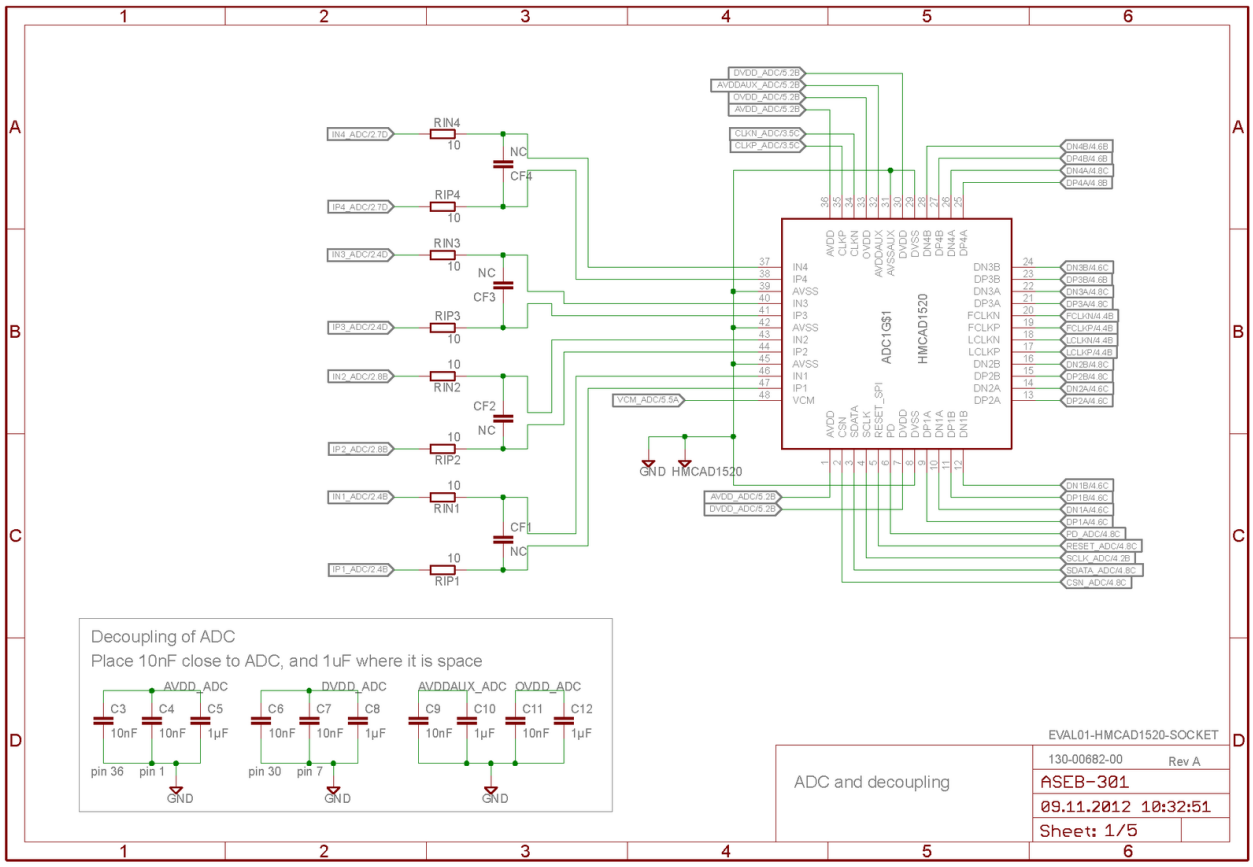

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Figure 4. Evaluation Board Schematic, ADC, and Decoupling (click to enlarge)

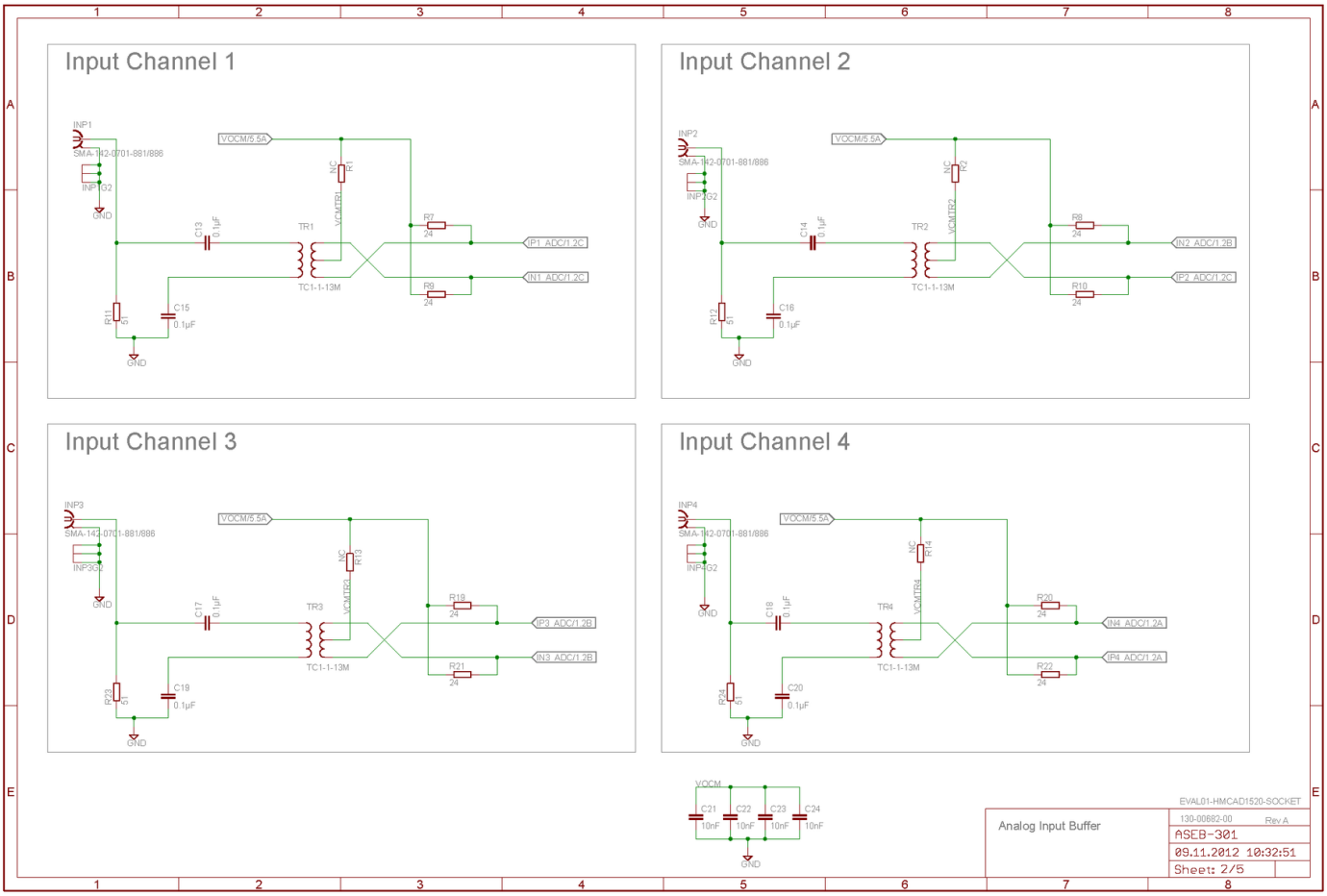

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Figure 5. Evaluation Board Schematic, Analog Input Buffer (click to enlarge)

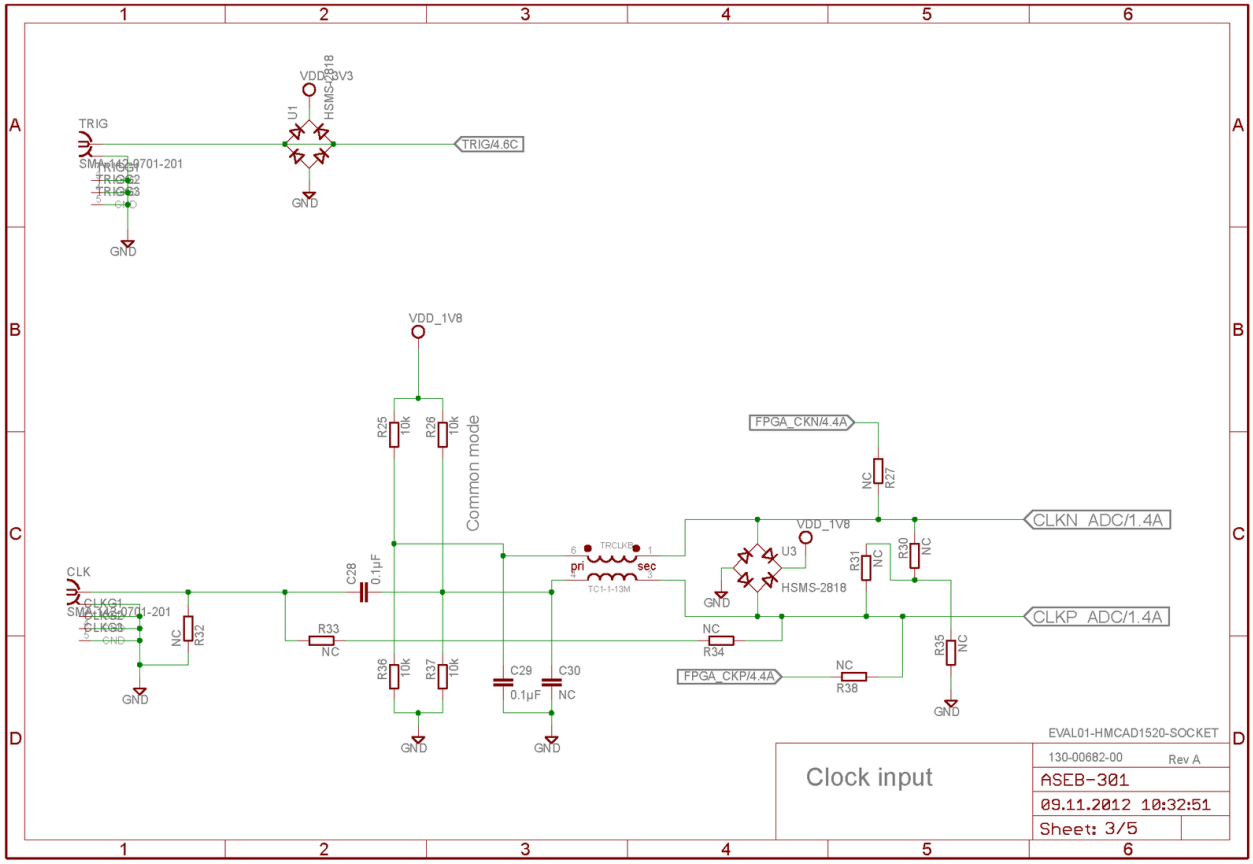

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Figure 6. Evaluation Board Schematic, Clock Input (click to enlarge)

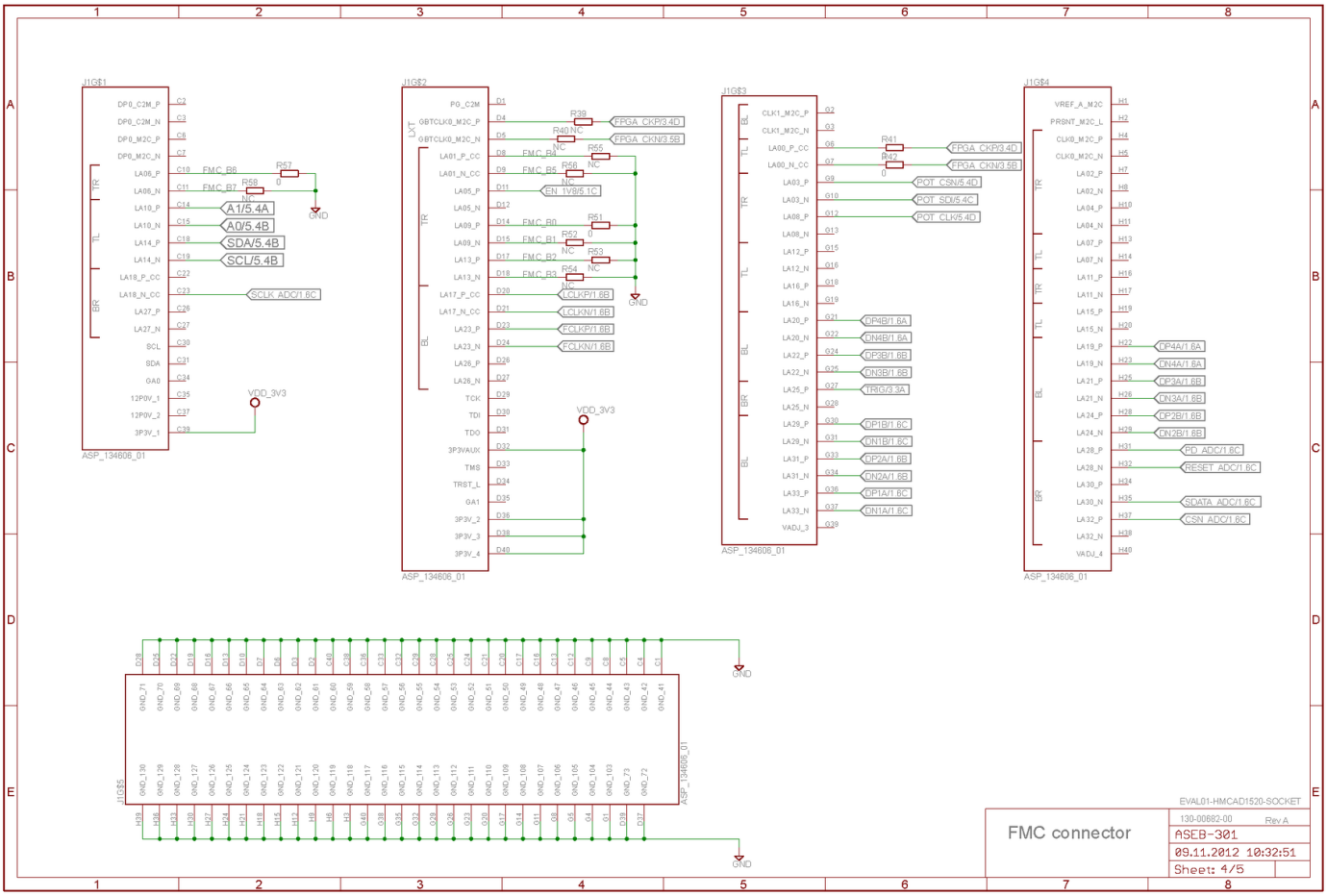

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Figure 7. Evaluation Board Schematic, FMC Connector (click to enlarge)

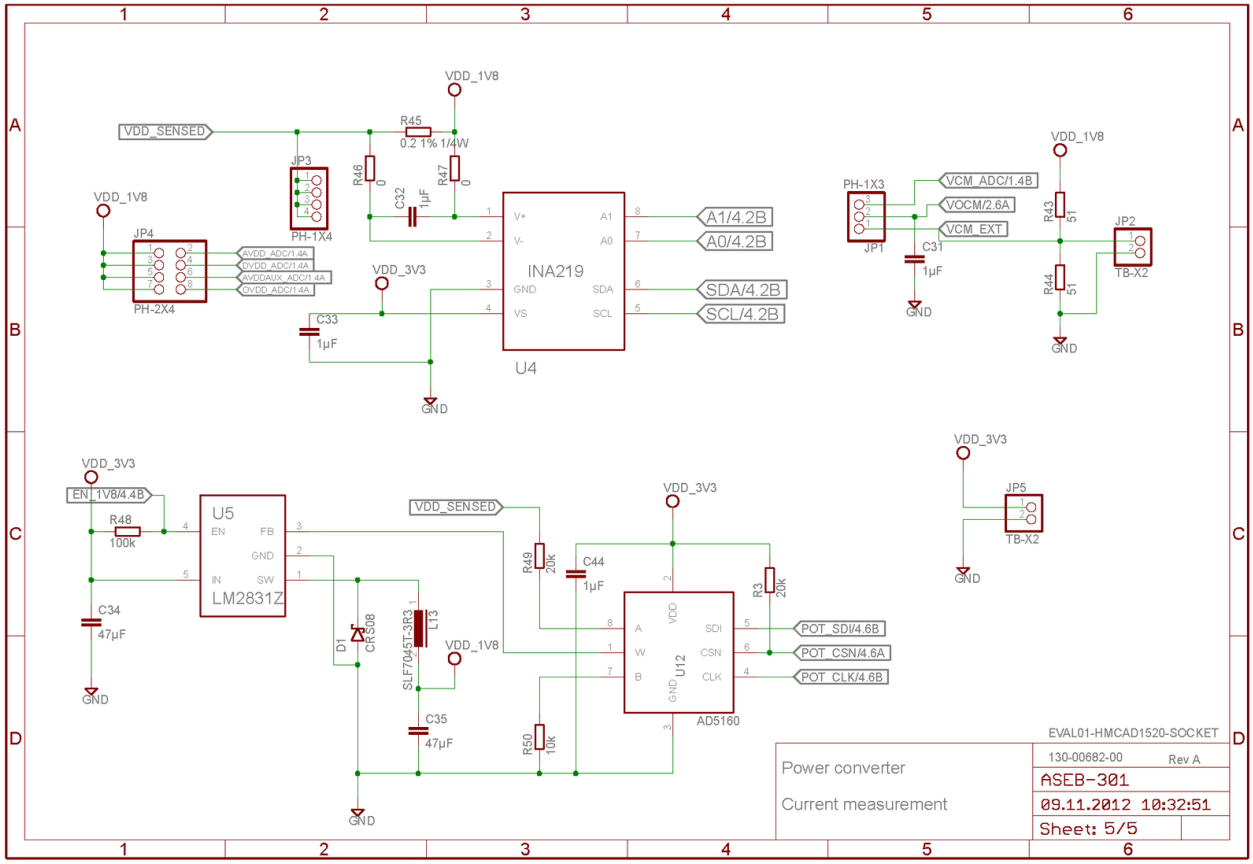

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Figure 8. Evaluation Board Schematic, Power Converter and Current Measurement (click to enlarge)

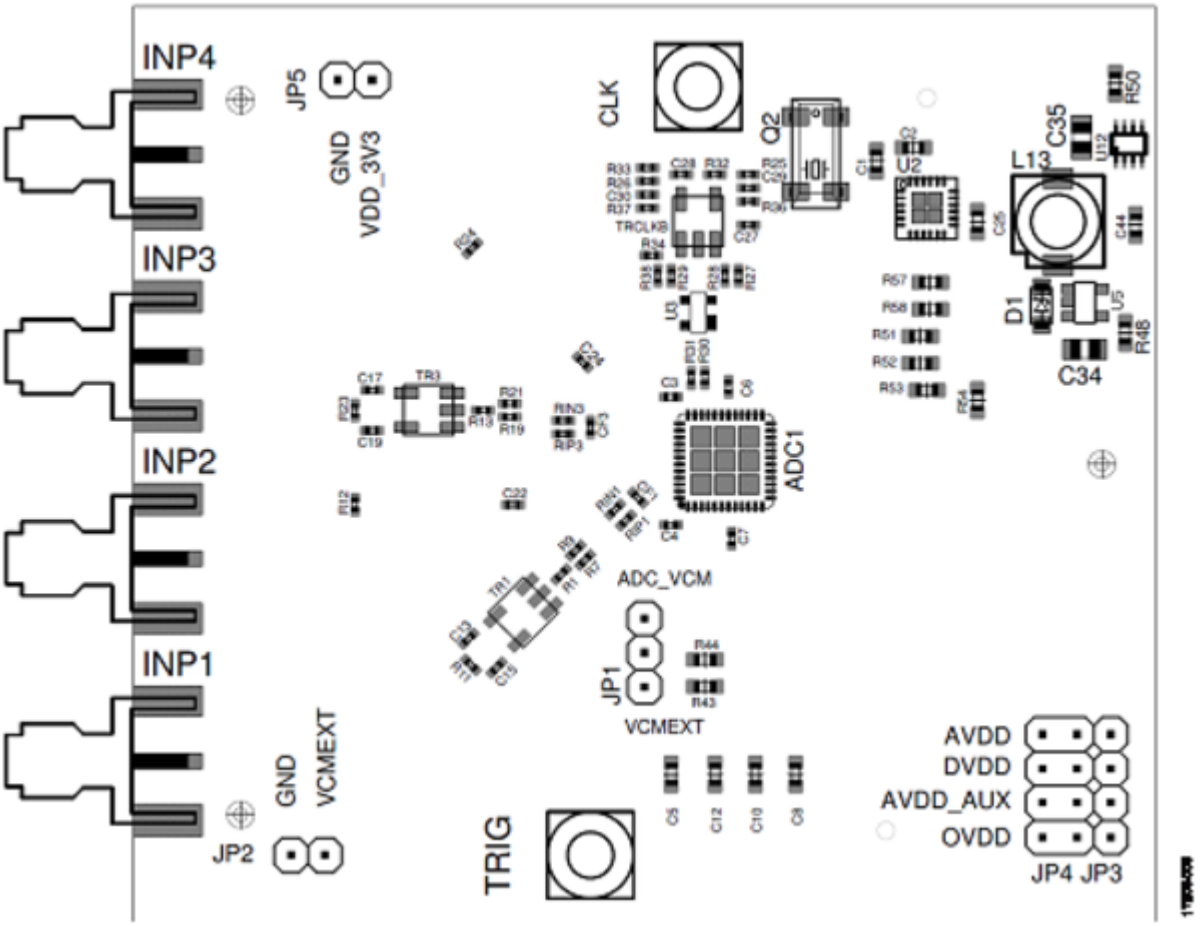

Figure 9. Component Placement, Top

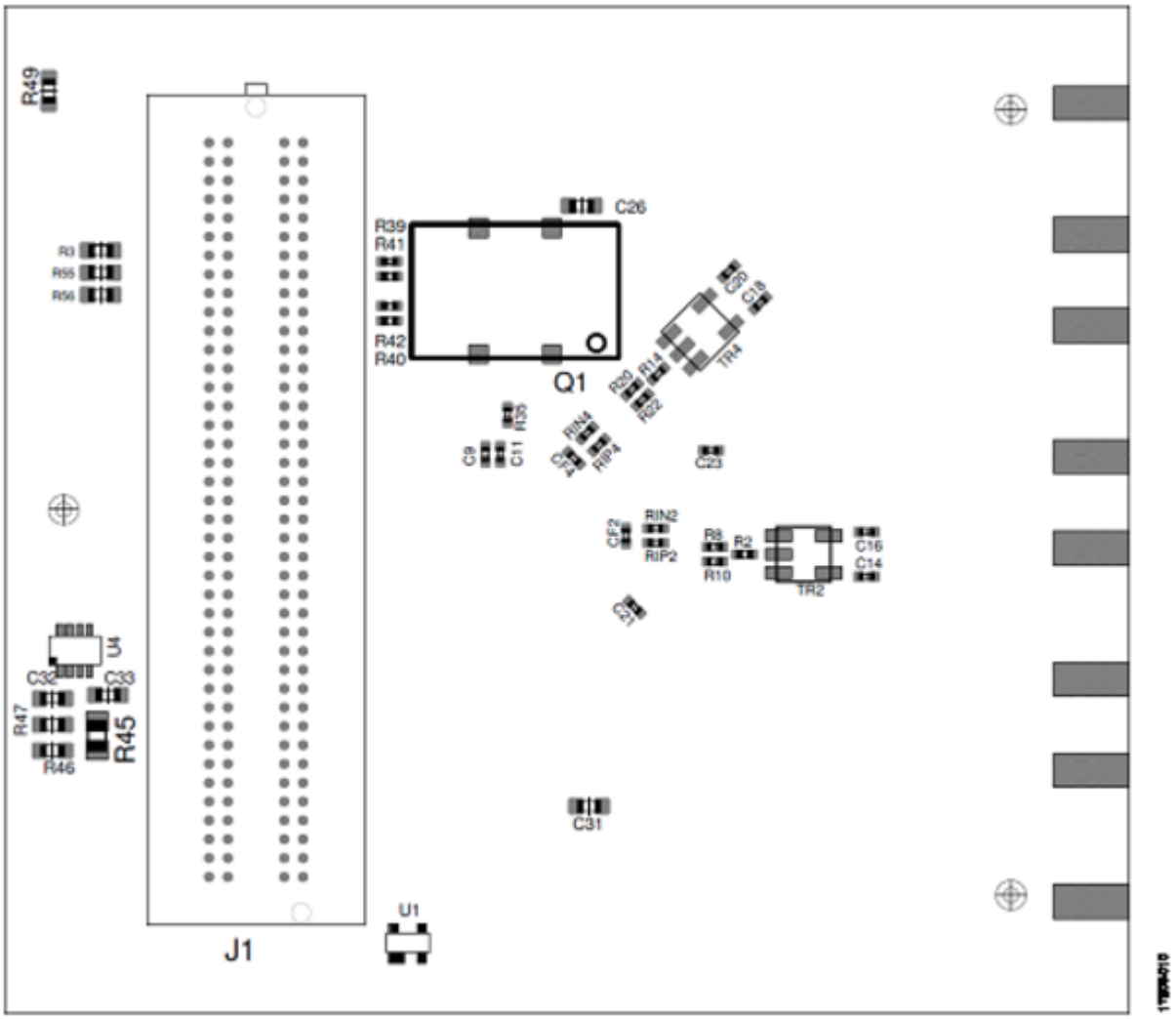

Figure 10. Component Placement, Bottom

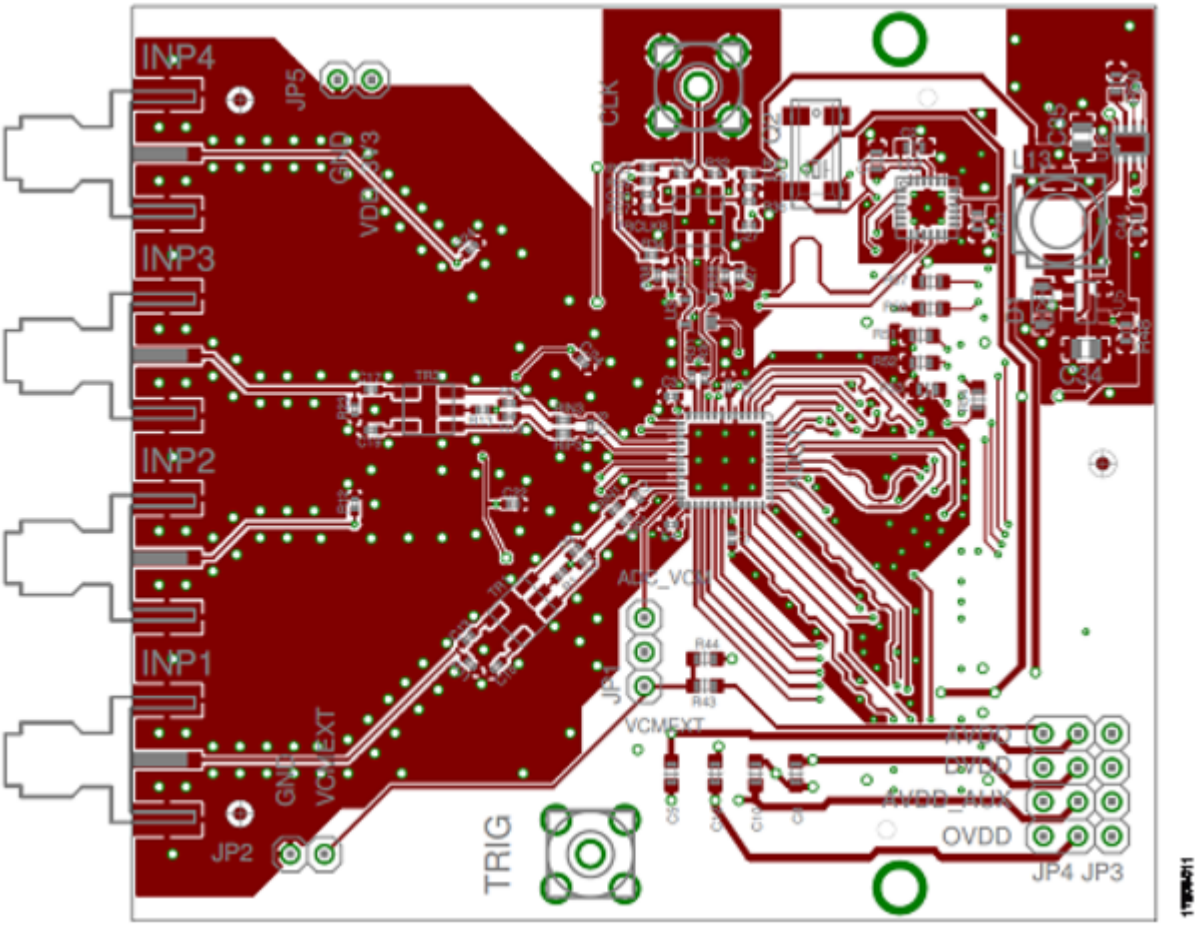

Figure 11. Top Layer

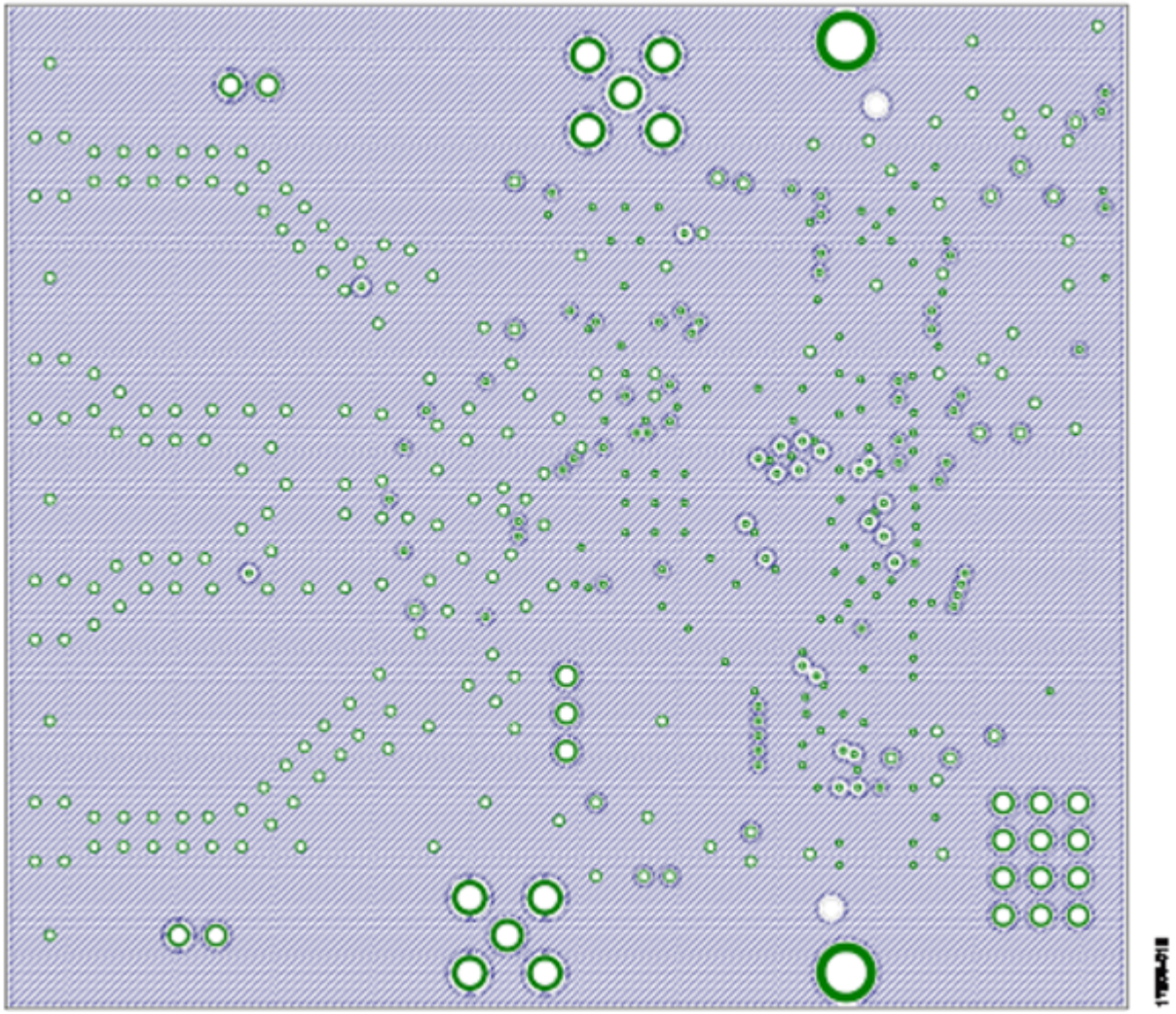

Figure 12. Inner Layer, Top

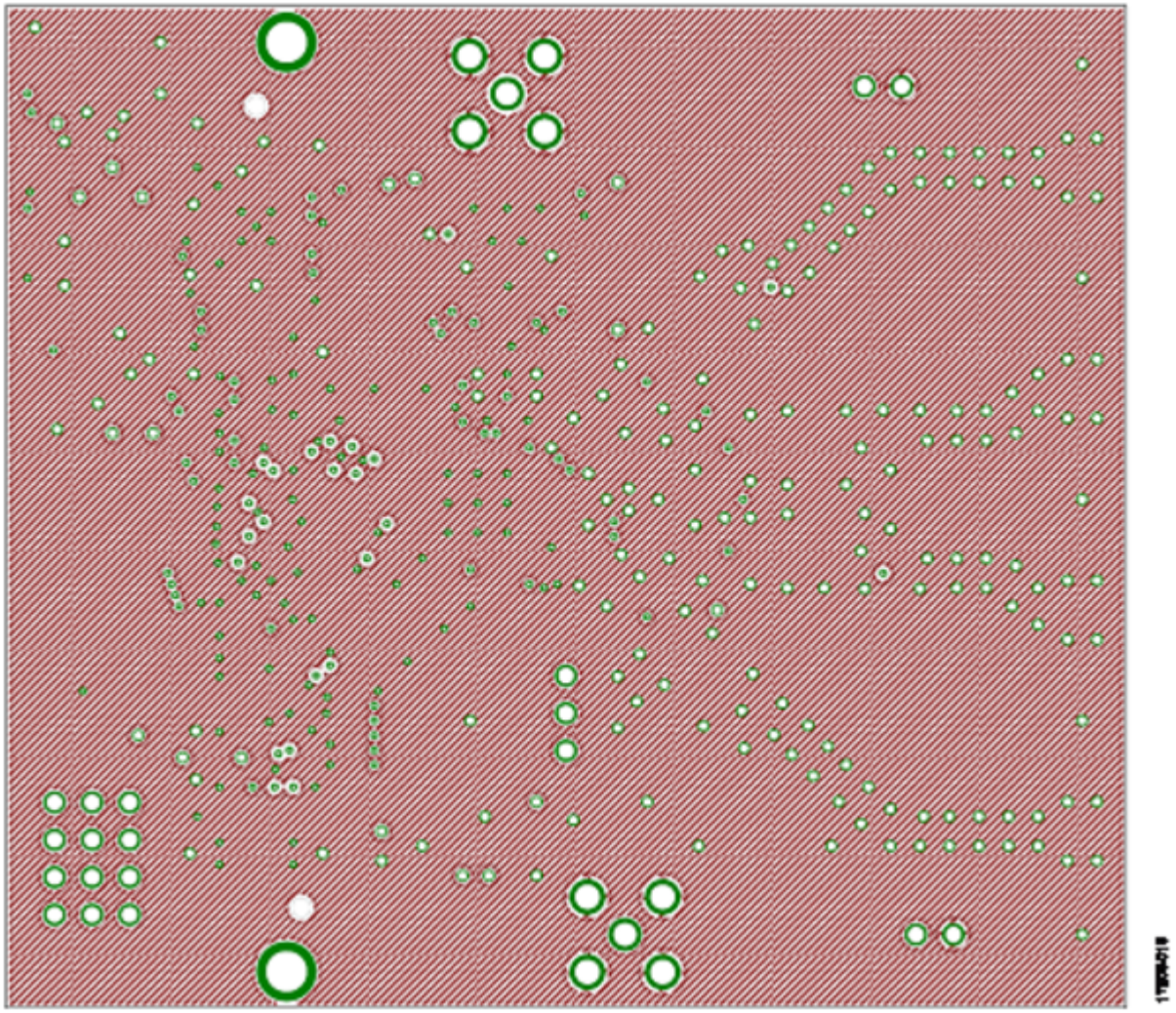

Figure 13. Inner Layer, Bottom

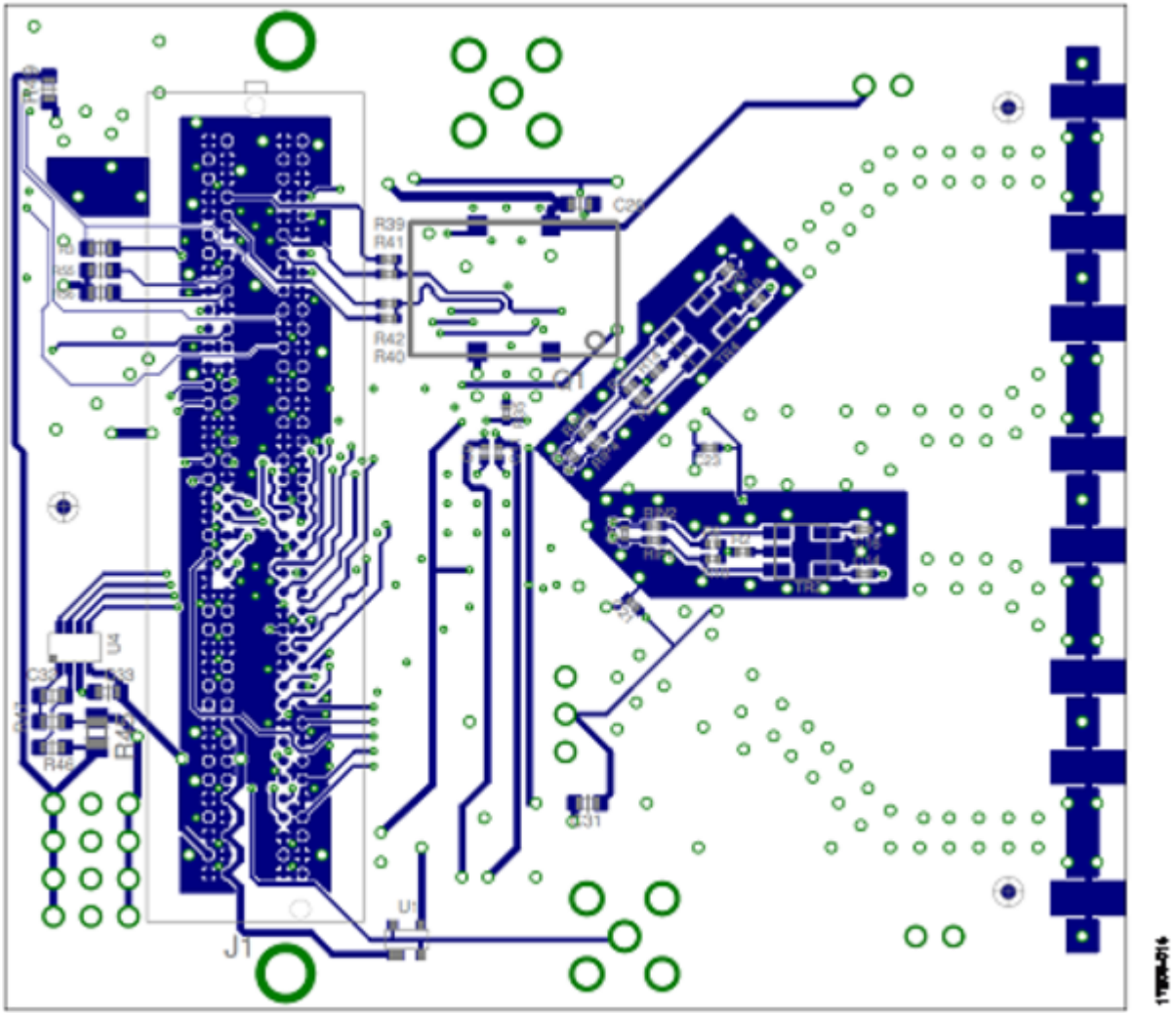

Figure 14. Bottom Layer

Ordering Information

Bill of Materials

Refence Designator	Description
ADC1	High speed multimode 12-bit/14-bit, 40 MSPS (mega/millions of samples per second) to 640 MSPS (mega/millions of samples per second) A/D converter
D1	Rectifier Schottky 30 V (volt), 1.5 A, 3-2A1A
J1	Connected single end array male 160 position
JP1	Terminal strip, single row 3-pin 0.100", TRW
JP3	Terminal strip, single row 4-pin through 0.100", TLW
JP4	Terminal strip, dual row 2×4 through 0.100", TLW
L13	Inductor shield power 3.3 µH 7045
R45	Resistor 0.20 Ω 1/4 W, 1%, 0805 SMD
R48	Resistor 100 kΩ 1/10 W, 1% 0603 SMD
R50	Resistor 10.0 kΩ 1/10 W, 1% 0603 SMD

Refence Designator	Description
U12	Integrated circuit (IC) pot digital SPI (Serial Peripheral Interface) 256 position SOT23-8
U4	IC current monitor 1% SOT23-8
U5	IC regulator buck 1.5 A SOT23-5
C34 to C35	Capacitor ceramic 47 µF, 6.3 V (volt), X5R 20% 0805
CLK, TRIG	Connected receptor straight printed circuit board (PCB) 0.155" G
JP2, JP5	Terminal strip, SGL Row 2, pin through 0.100", TLW
R3, R49	Resistor 20 kΩ 1/10 W, 1% 0603 SMD
R42 to R42	Resistor 0 Ω 1/16 W, 5% 0402 SMD
R43 to R44	Resistor 51 Ω 1/10 W, 1% 0603 SMD
U1, U3	Schottky diode, radio frequency (RF), bridge quad
INP1 to INP4	SCD, MA-F, edge launch, 0.031" board, Johnson
R11 to R12, R23 to R24	Resistor 51 Ω 1/10 W, 1% 0402 SMD
R25 to R26, R36 to R37	Resistor 10.0 k (thousands (prefix, as in kHz, kΩ, kV, kW)) Ω 1/16 W, 1% 0402 SMD
R46 to R47, R51, R53, R57	Resistor 0 Ω 1/10 W, 5% 0603 SMD
TR1 to TR4, TRCLKB	RF transformer, 50 Ω, 4.5 MHz (megahertz) to 3000 MHz (megahertz), TC!-1-13M+
C5, C8, C10, C12, C31 to C33, C44	Capacitor ceramic 1 µF, 25 V (volt), 15% X5R 0603
R7 to R10, R19 to R22	Resistor 24 Ω 1/10 W, 1% 0402 SMD
RIN1 to RIN4, RIP1 to RIP4	Resistor 10 Ω 1/10 W, 1% 0402 SMD
C13 to C20, C28 to C29	Capacitor ceramic 0.1 µF, 50 V (volt), 10% X7R 0402
C3 to C4, C6 to C7, C9, C11, C21 to C24	Capacitor ceramic 0.01 µF, 50 V (volt), 10% X7R 0402
C1 to C2, C25 to C27, C30, CF1 to CF4, Q1 to Q2, R1 to R2, R13 to R14, R27 to R35, R38 to R40, R52, R54 to R56, R58, U2	Do not populate components

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