

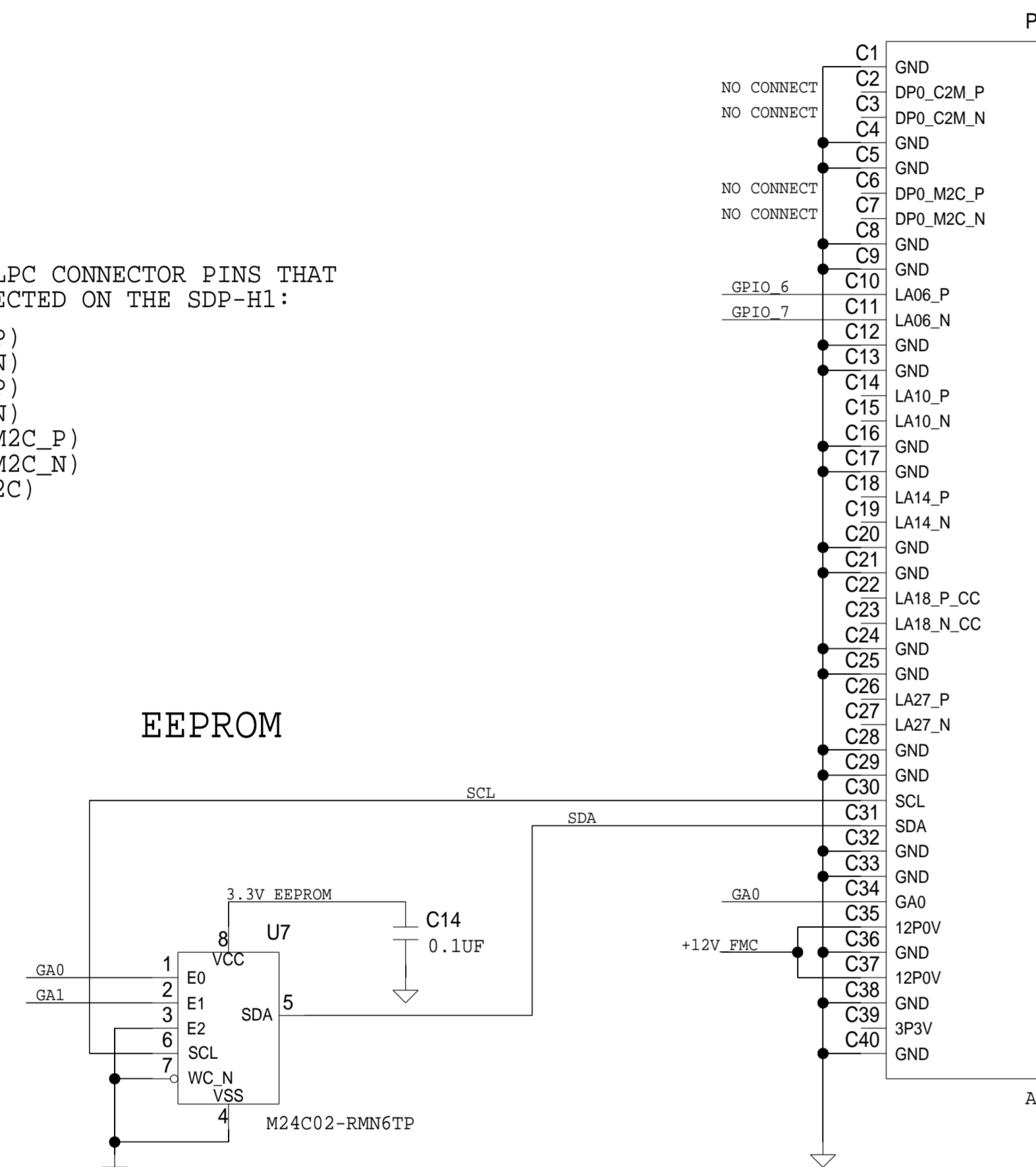


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# FPGA FMC CONNECTIONS

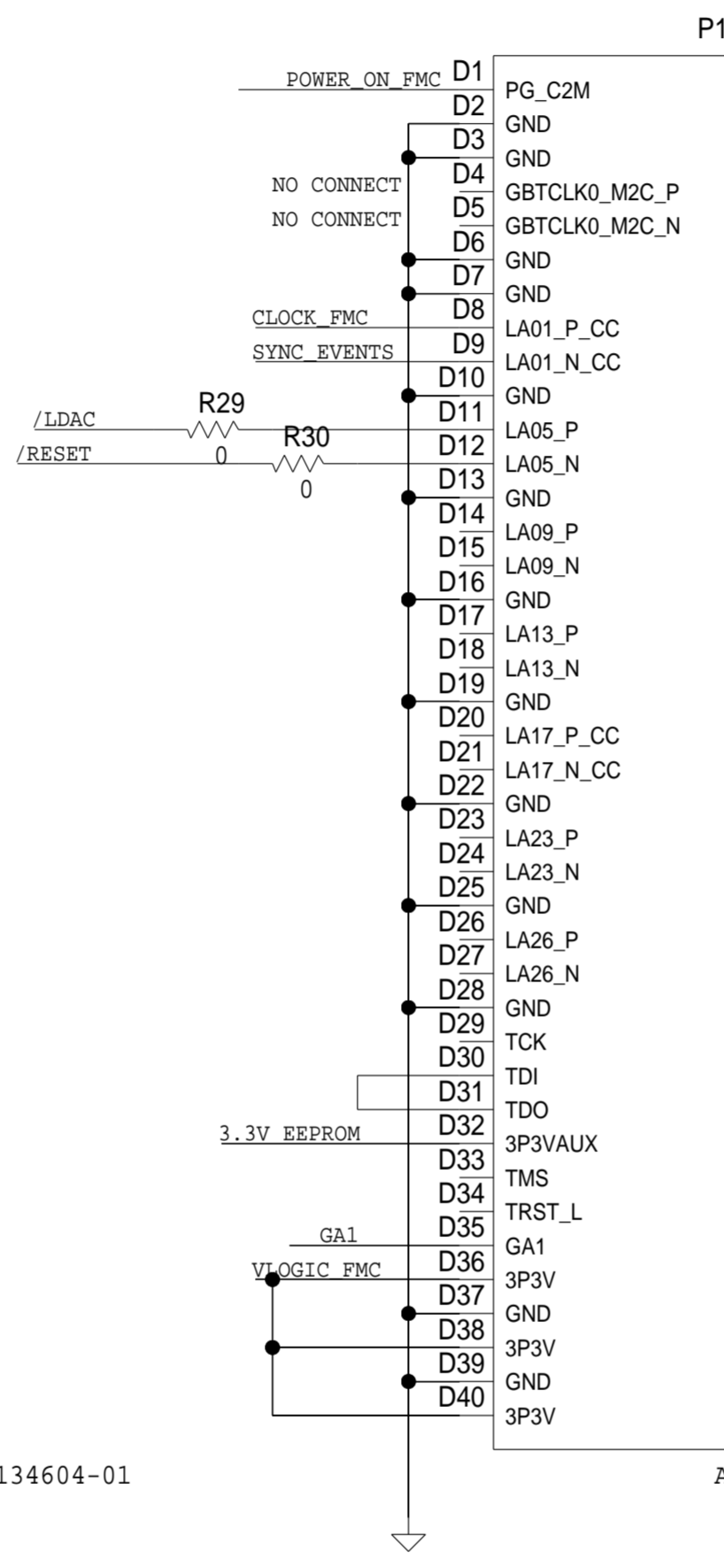
LIST OF FMC-LPC CONNECTOR PINS THAT ARE NOT CONNECTED ON THE SDP-H1:

- C2 (DP0\_C2M\_P)
- C3 (DP0\_C2M\_N)
- C6 (DP0\_M2C\_P)
- C7 (DP0\_M2C\_N)
- D4 (GBTCLK0\_M2C\_P)
- D5 (GBTCLK0\_M2C\_N)
- H1 (VREF\_A\_M2C)



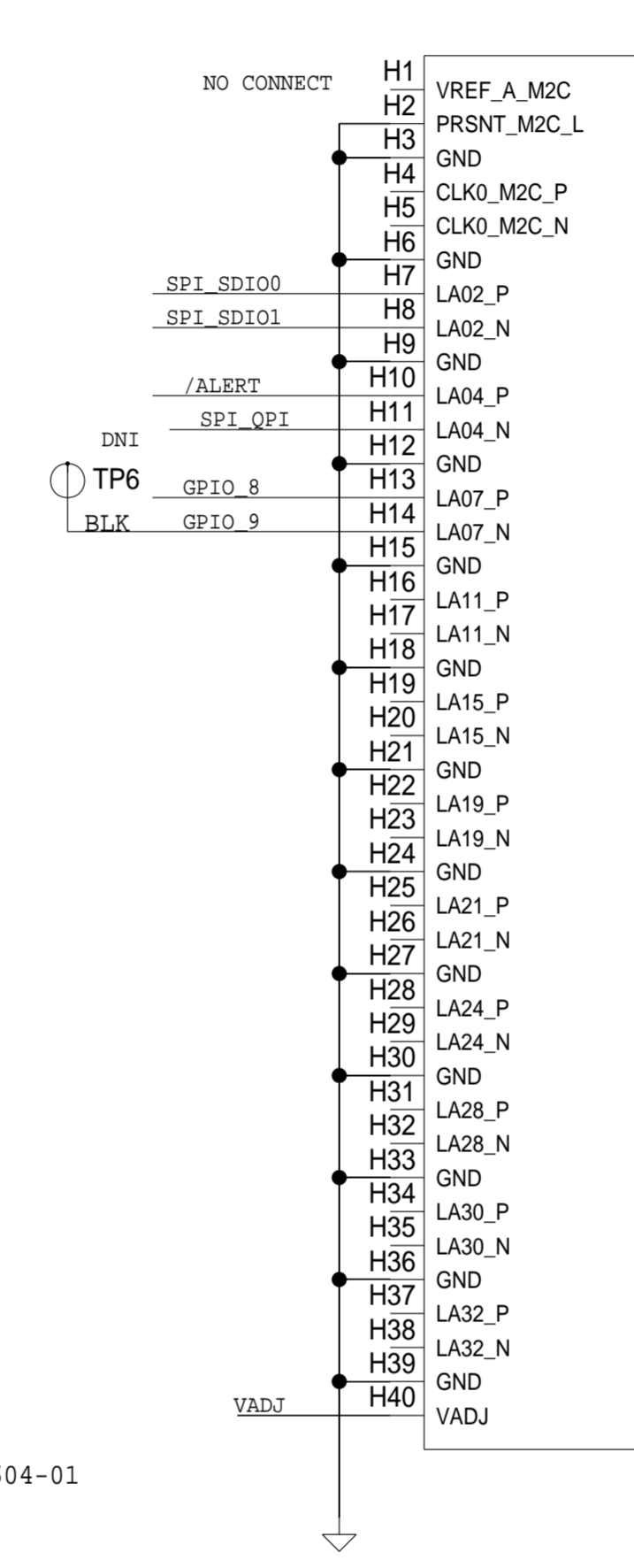
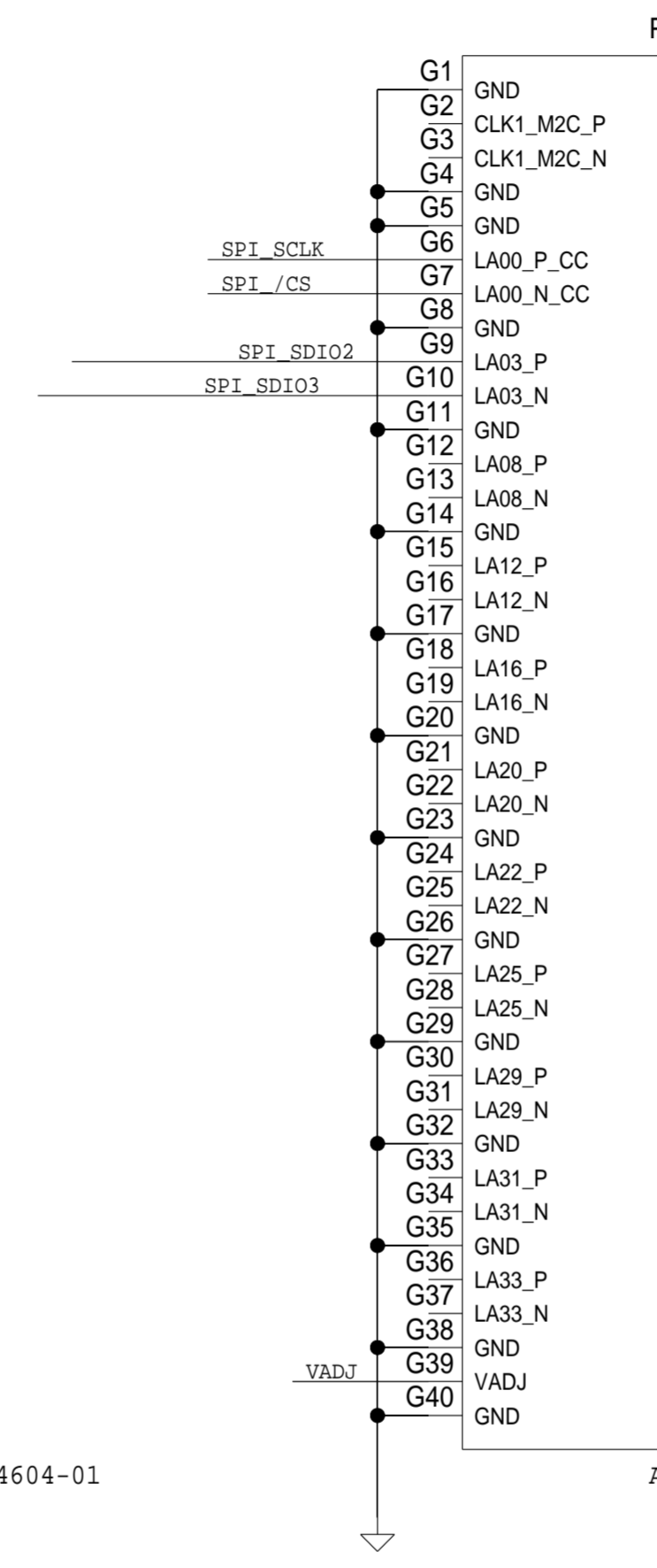
EEPROM REQUIRED IN VITA57.1 STANDARD.  
I2C LINE PULL-UP RESISTORS ON FPGA BOARD.  
I2C ADDRESS SET BY CONTROLLER BOARD.

MISSING THE CLOCK, AND INTERRUPTION



IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN

POWER SUPPLIES:  
12P0V. 1A MAX CURRENT LIMIT  
3P3V. 3A MAX CURRENT LIMIT  
VADJ. 2A MAX CURRENT LIMIT. 1.2V TO 3.3V.

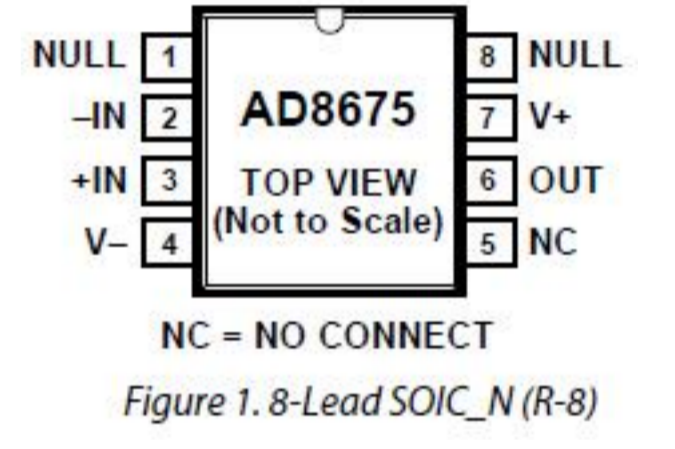
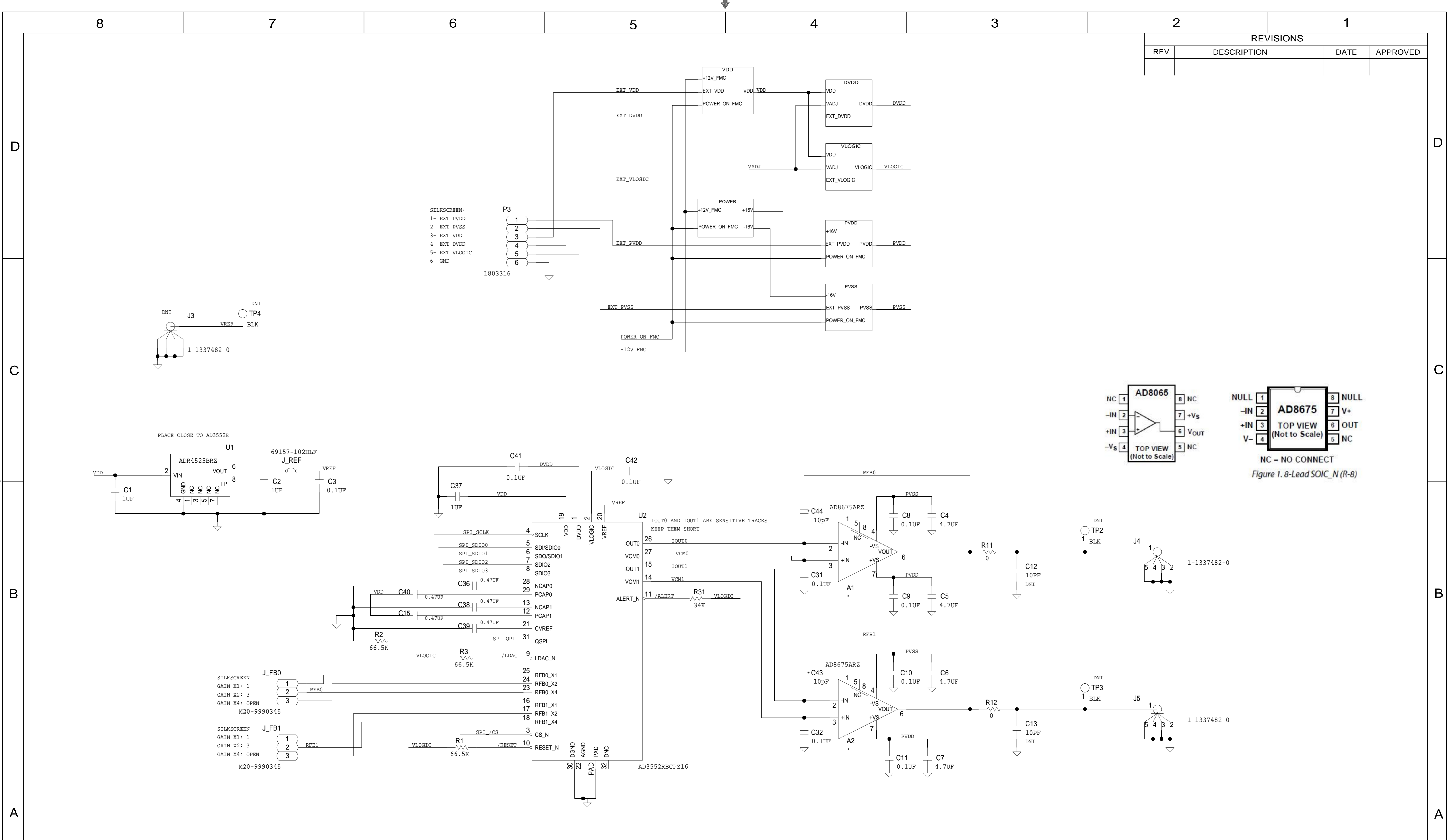


BOARD PRESENT PIN (H2) MUST ALWAYS BE TIED TO GROUND

PINS MUST BE ASSIGNED STARTING WITH LA00 AND MOVING UP THE LA BUS UNTIL IT IS FULL. WHEN SINGLE-ENDED SIGNALING IS USED, THE \_P LINE SHOULD BE USED BEFORE THE \_N LINE OF THE SAME PAIR IS USED.

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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-057486-02	REV E	
PTD ENGINEER Antonio Jimenez	SIZE D	SCALE 1:1	SHEET 2 OF 10

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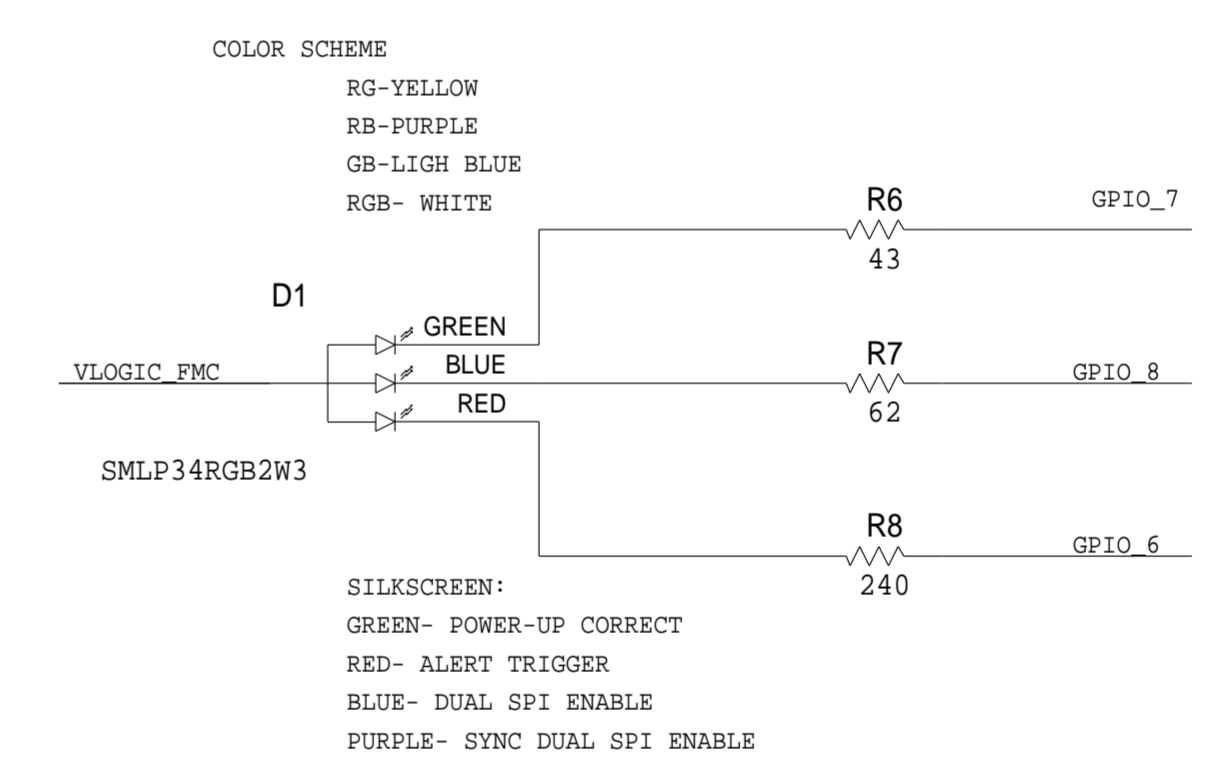
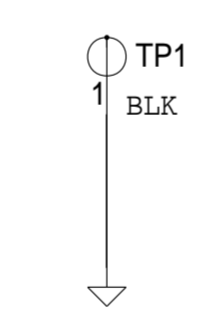
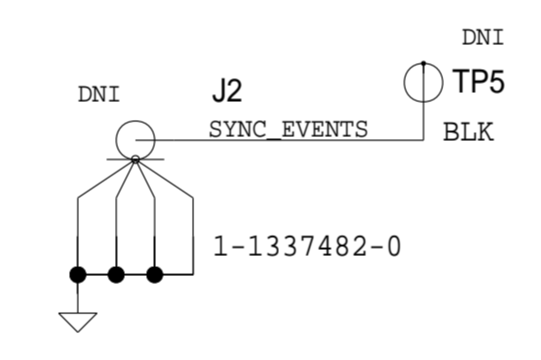
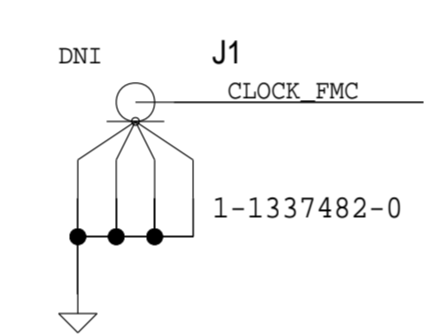
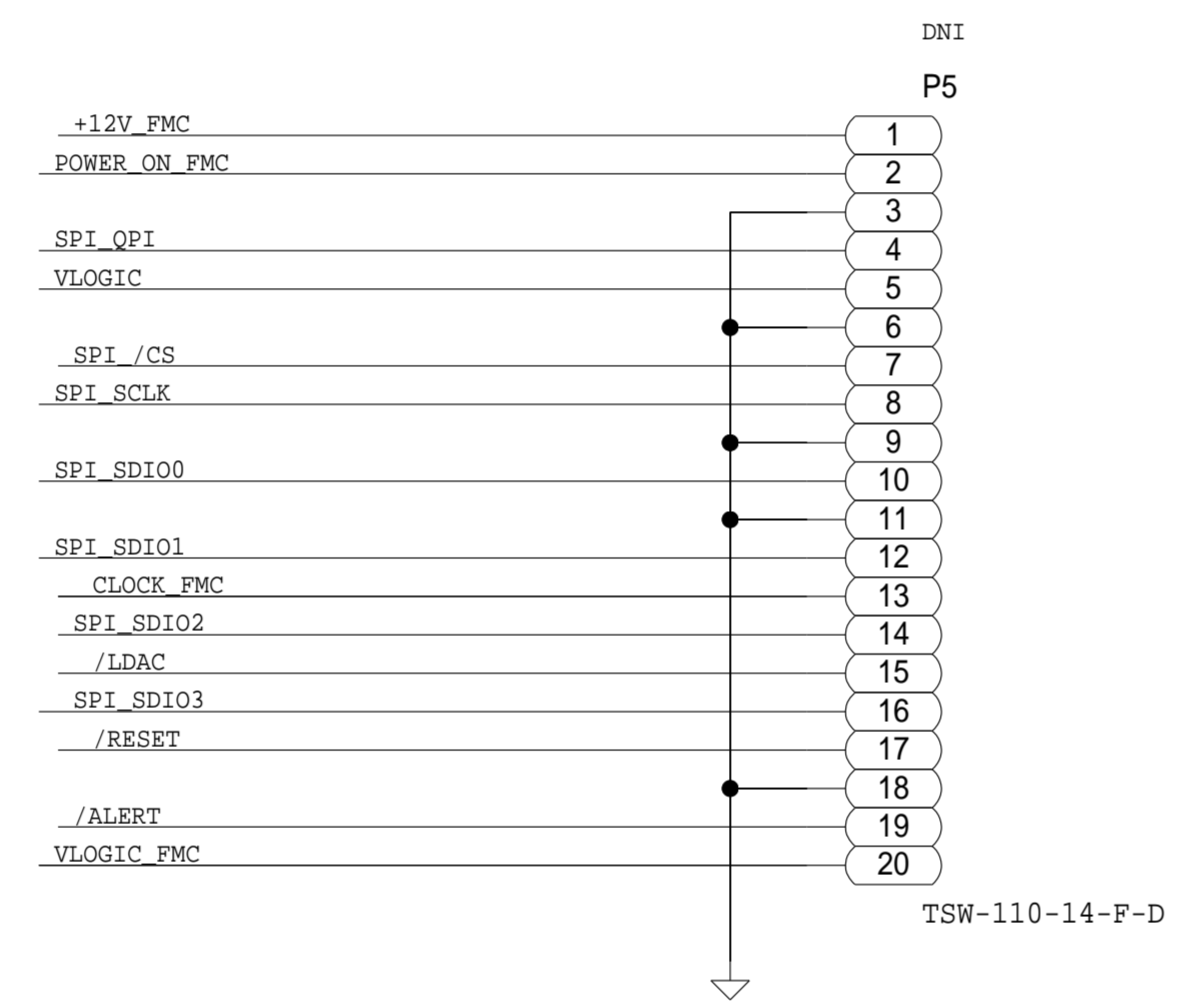
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PTD ENGINEER Antonio Jimenez	SIZE D	SCALE 1:1	SHEET 3 OF 10

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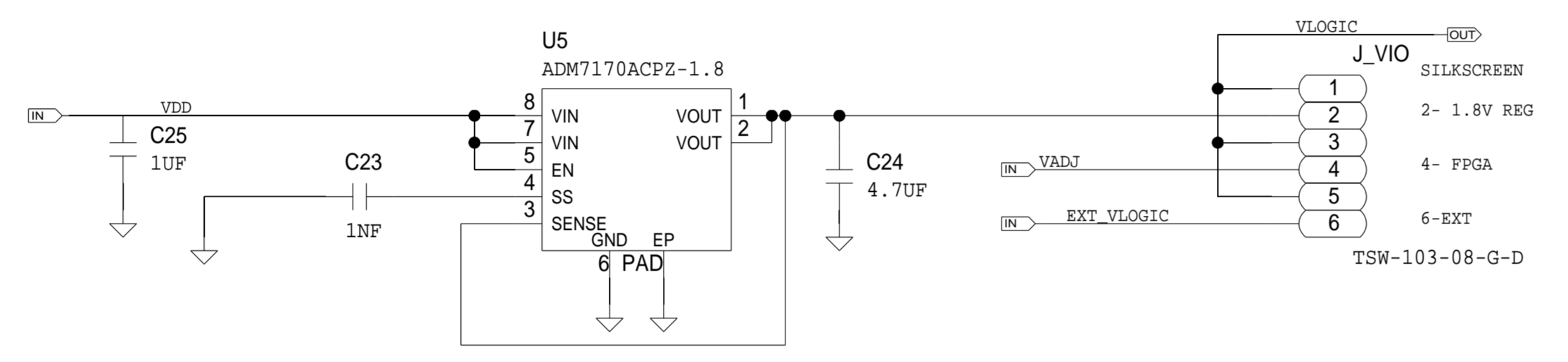
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	<b>SCHEMATIC</b>		
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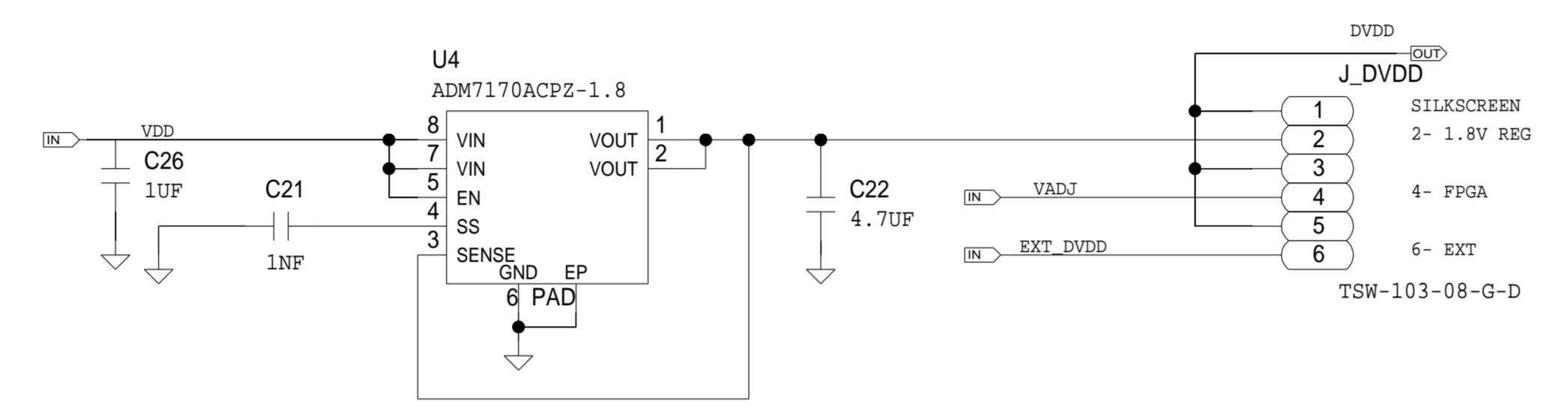
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SHEET 5 OF 10		SHEET 5 OF 10	

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REV	DESCRIPTION	DATE	APPROVED



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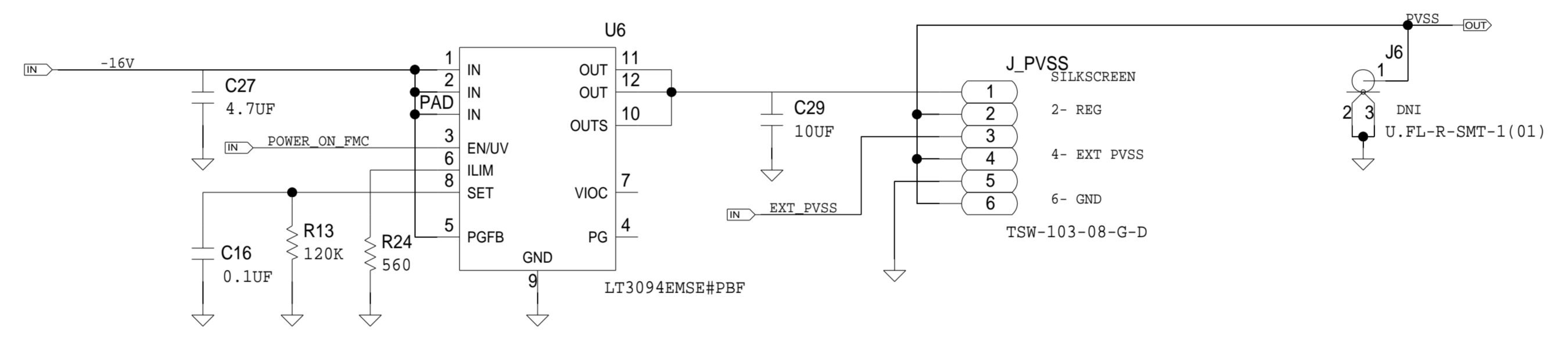
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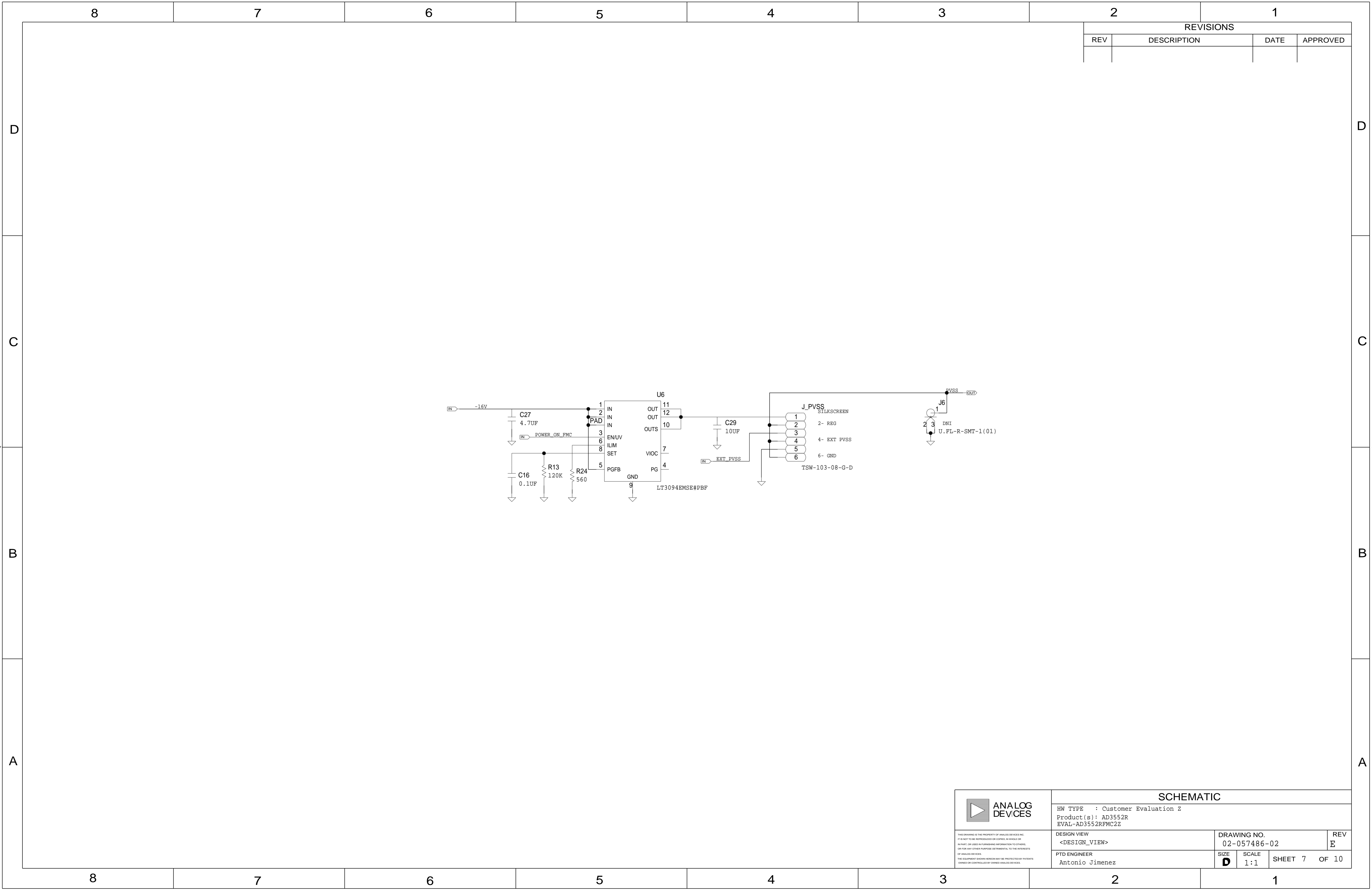
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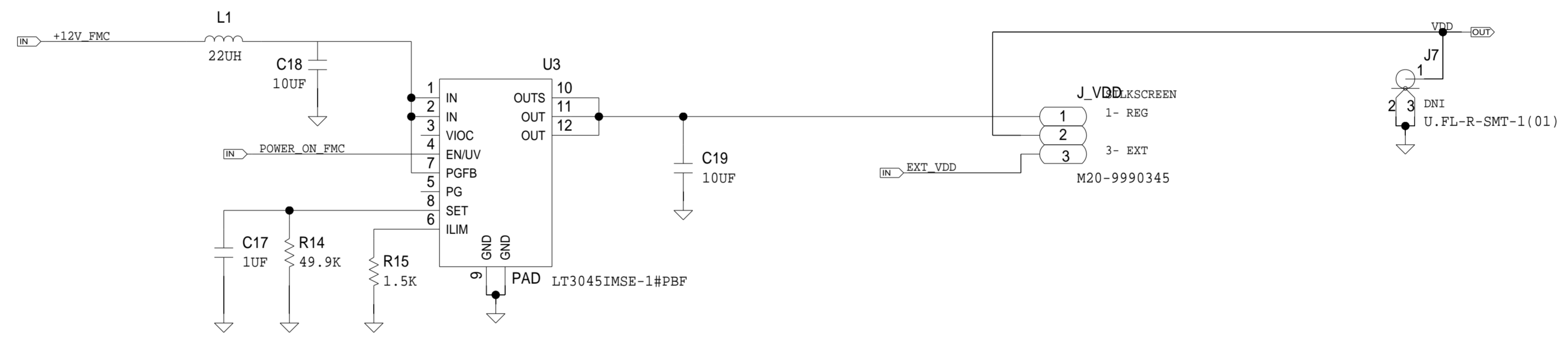
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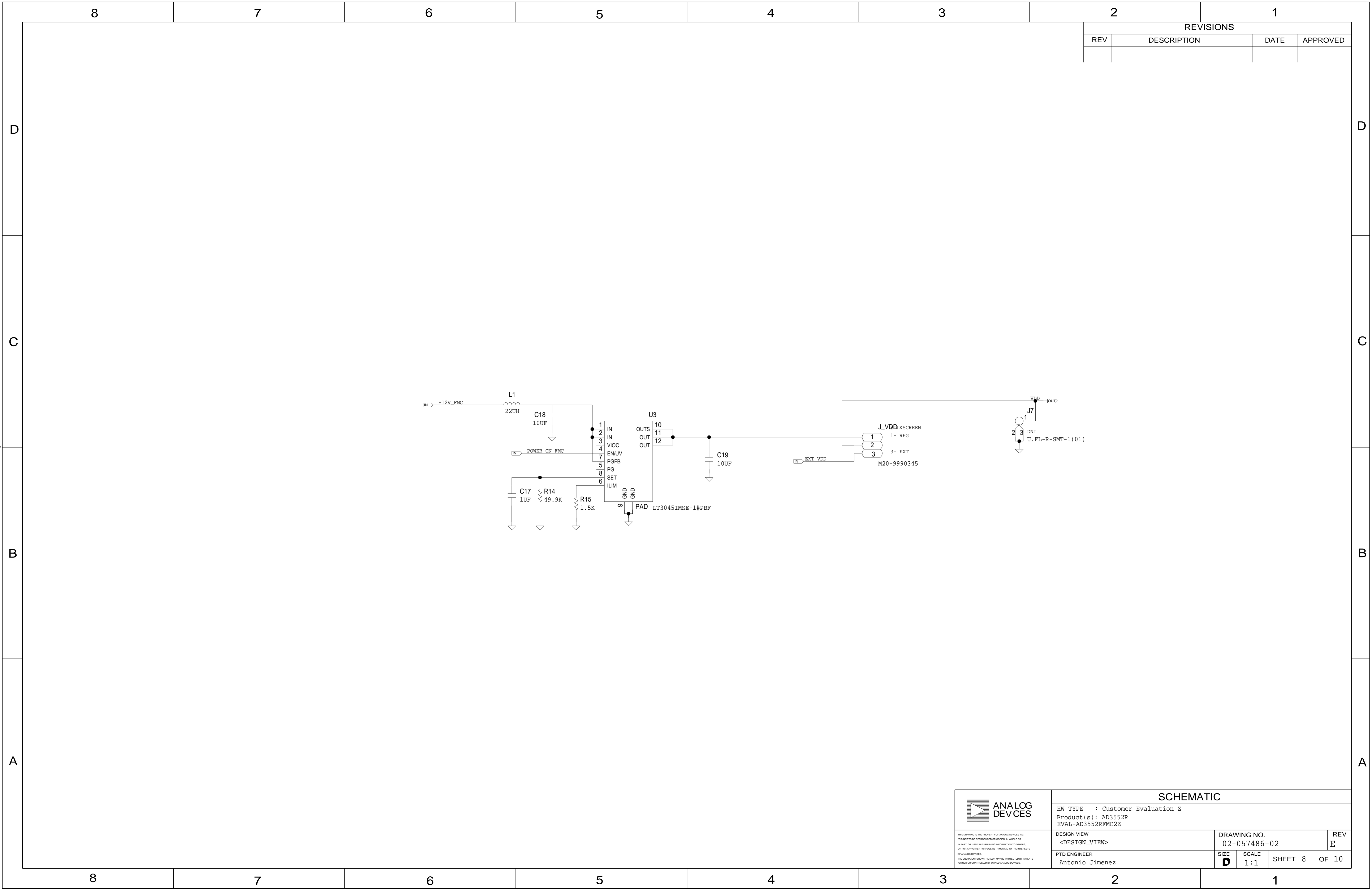
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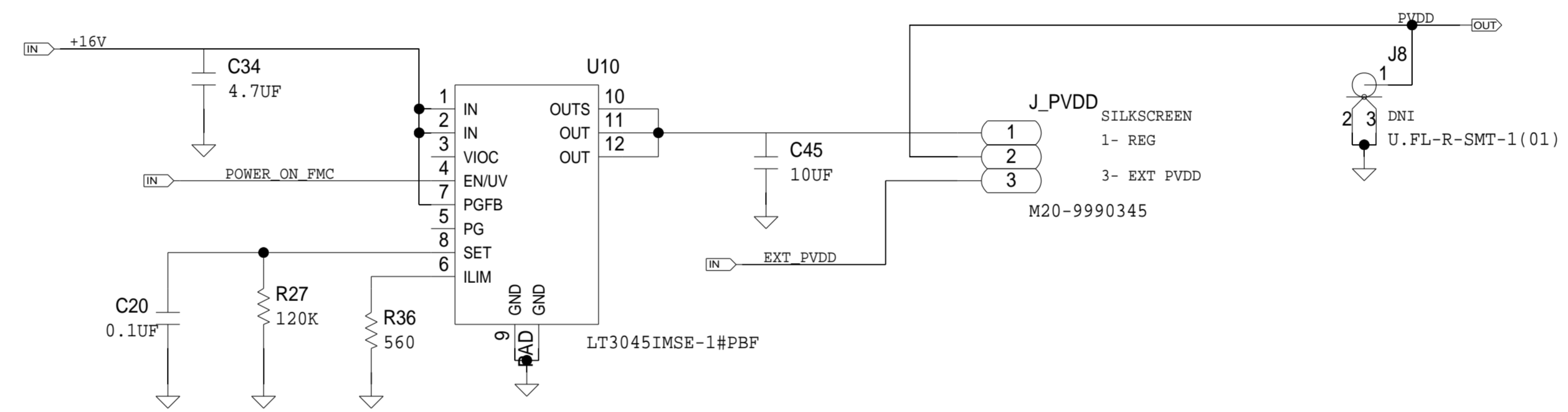


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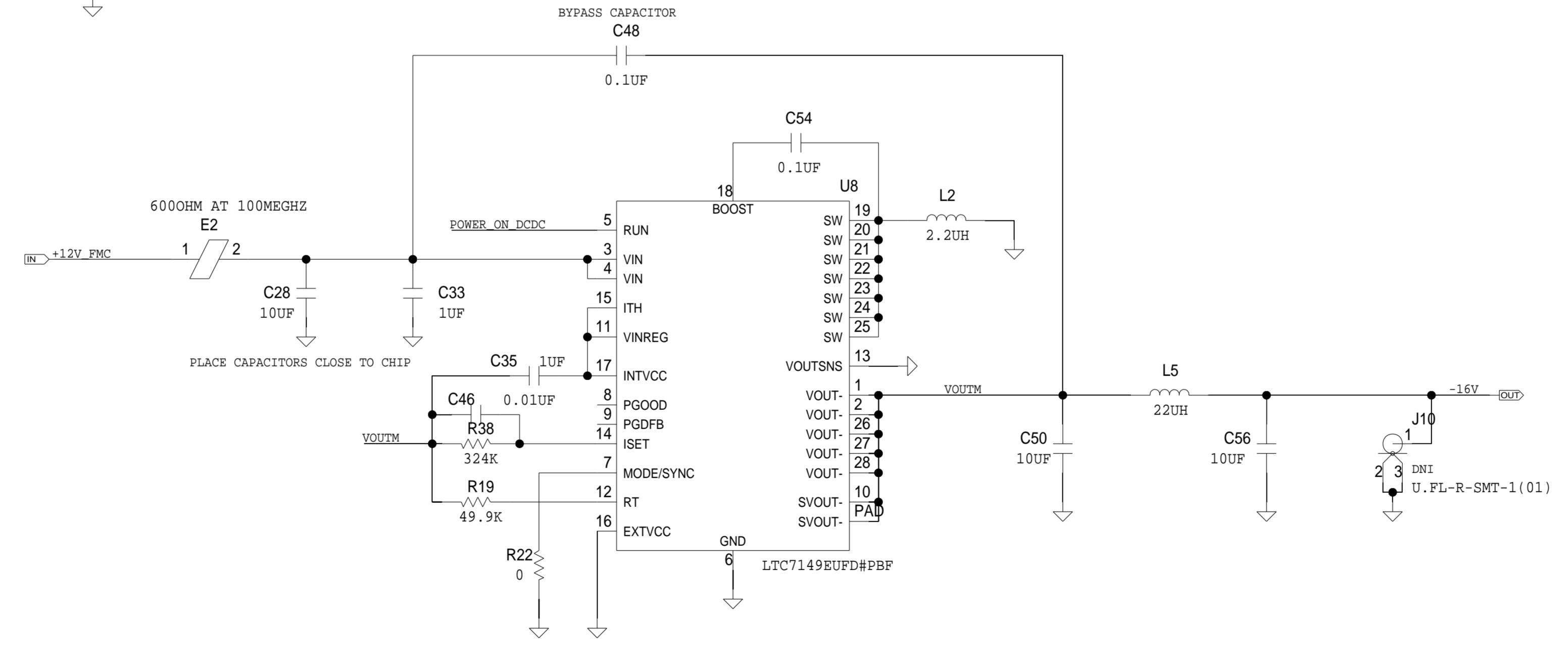
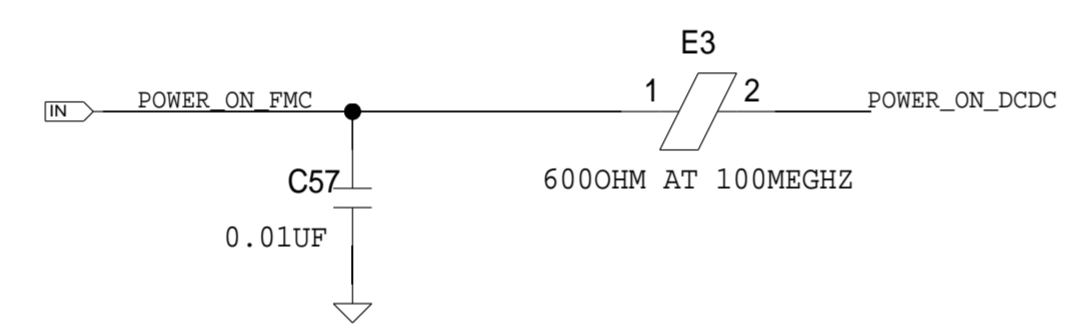
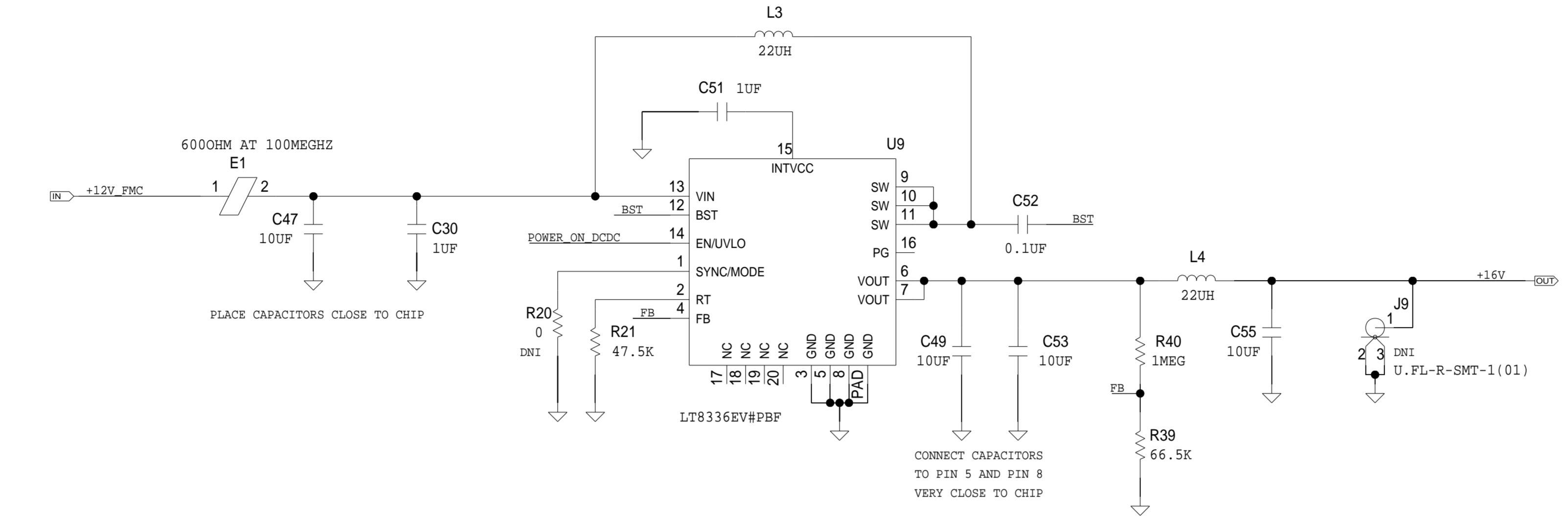


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SHEET 9 OF 10		SHEET 9 OF 10	

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