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RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

5 4

JUMPER TABLE		
JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

2 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	AD9136	5-14	L.W.

USE 13045 REV B BOARDS

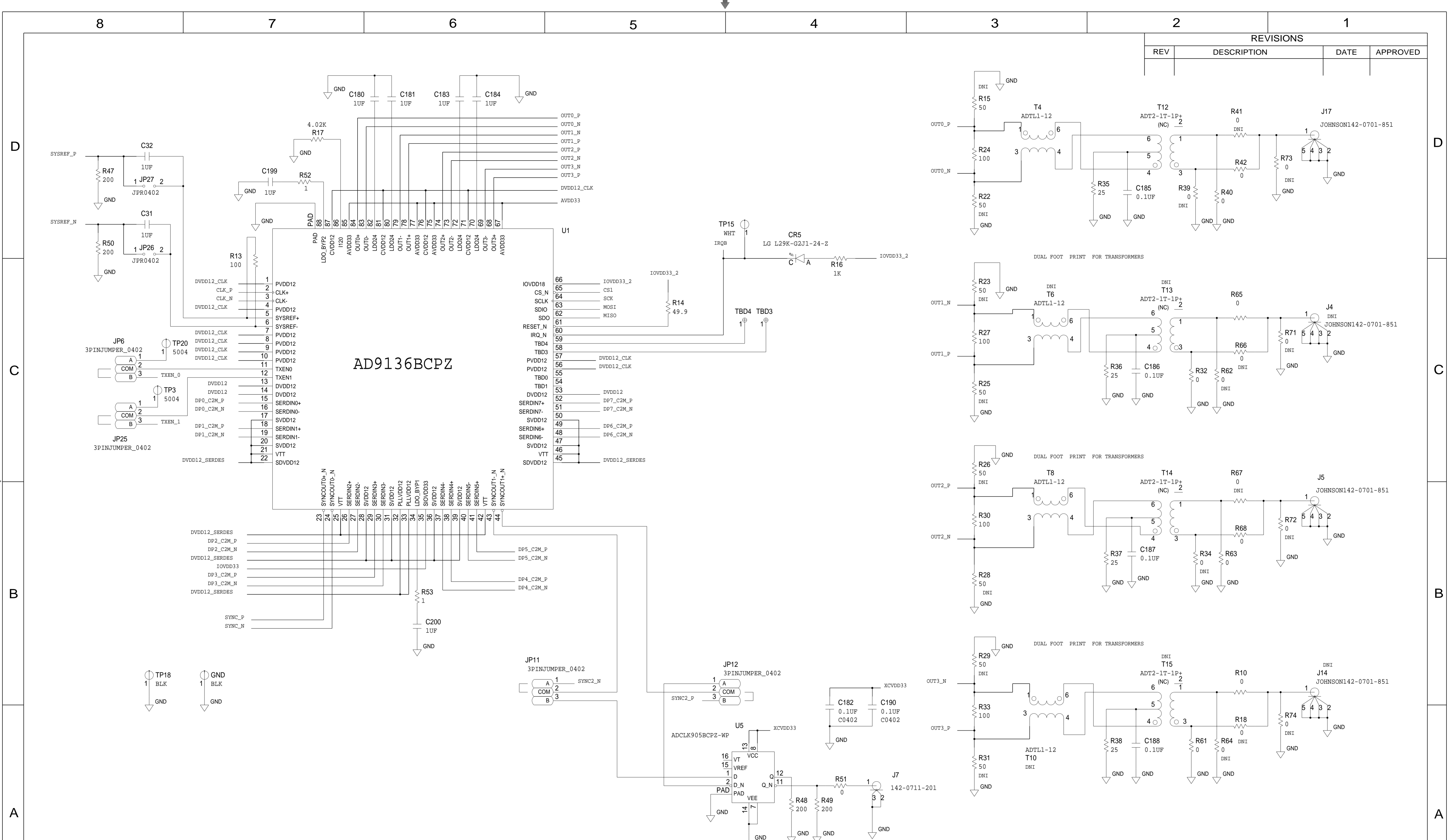
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A

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

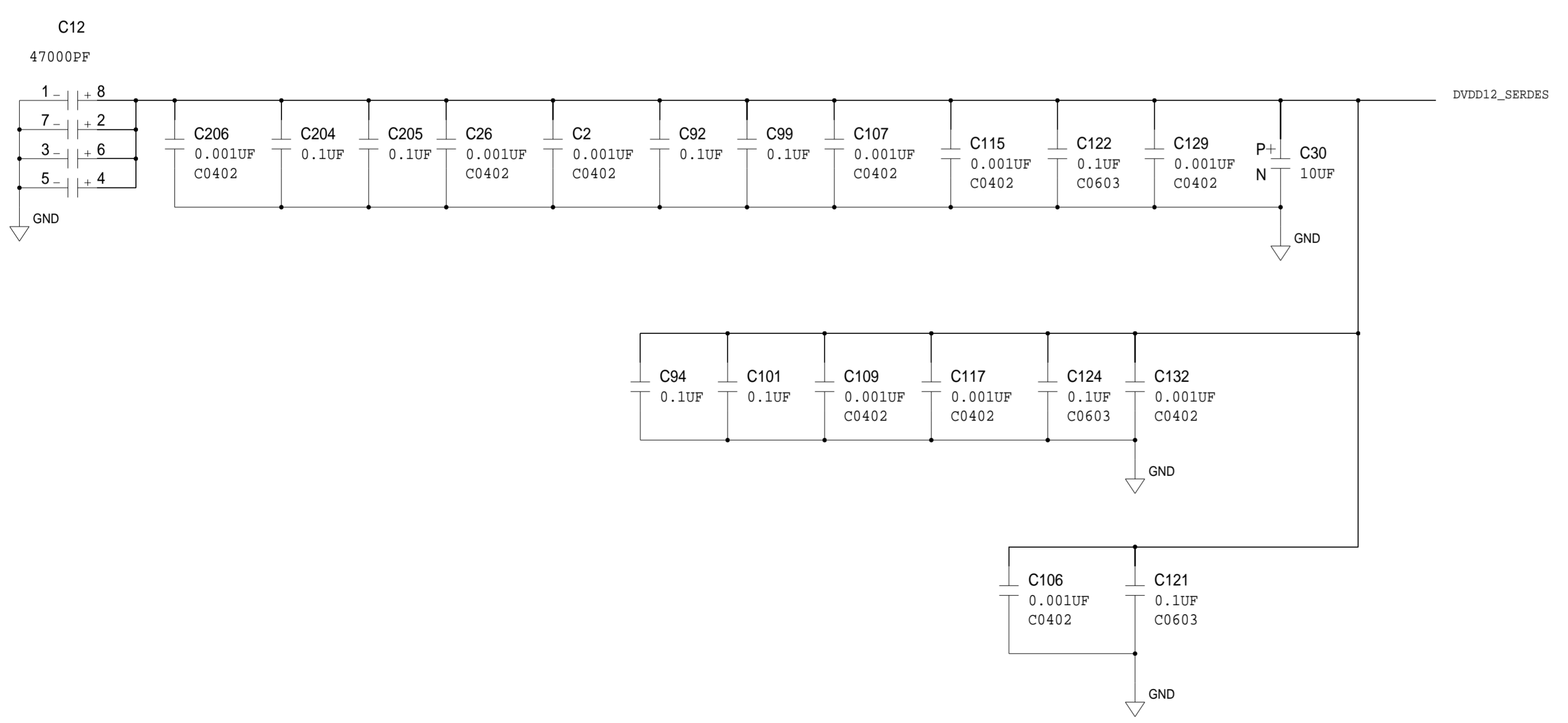
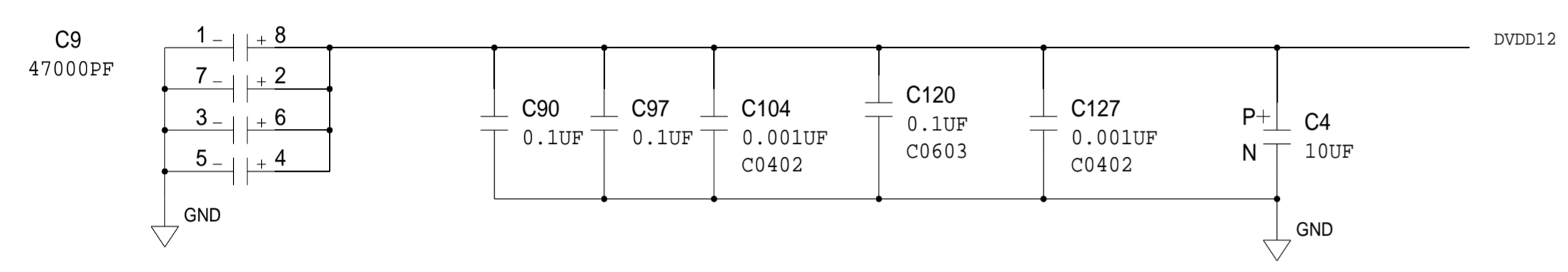
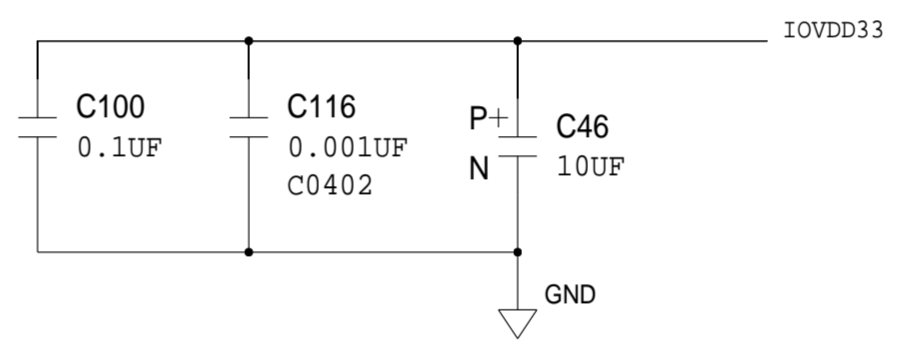
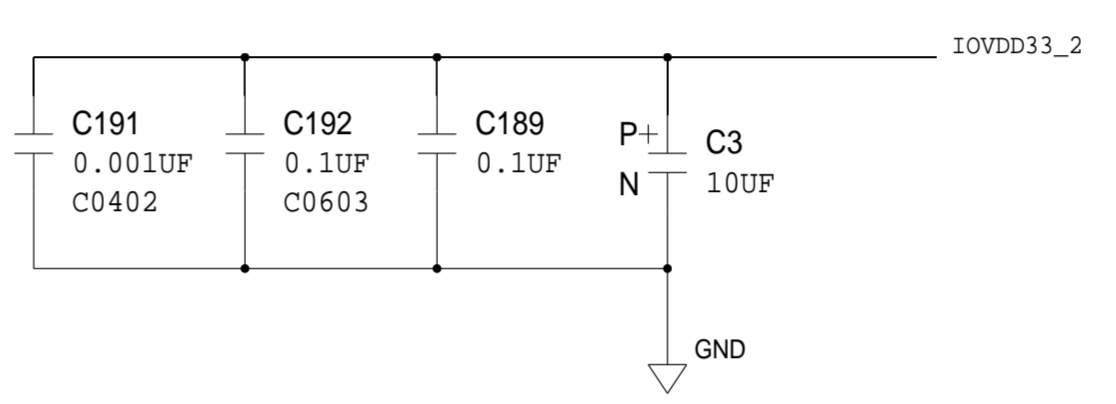
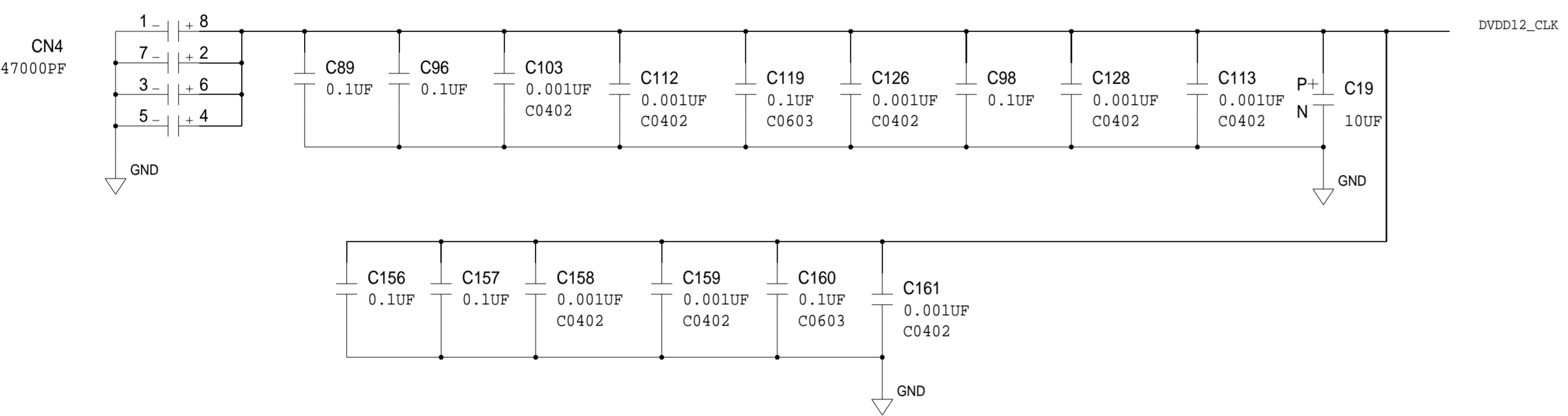
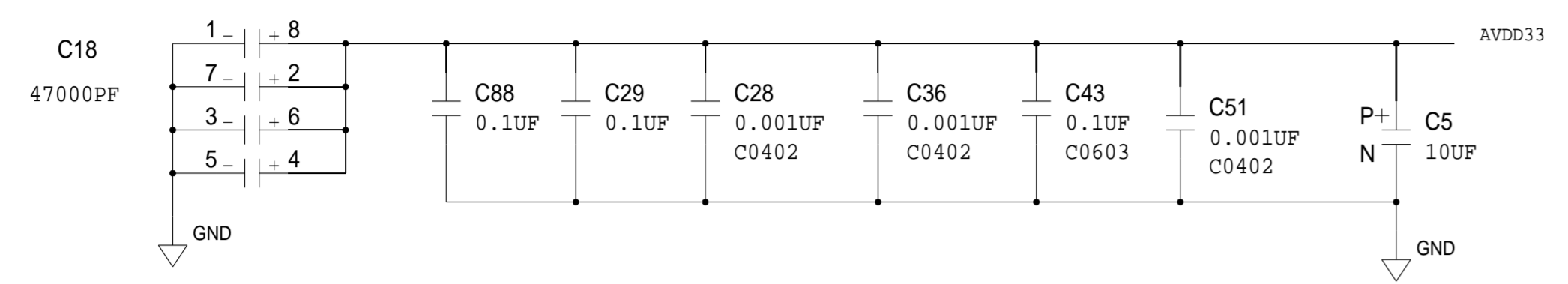
TEMPLATE ENGINEER P. ALONGI	DATE 3/22/11	SCHEMATIC			
HARDWARE SERVICES -		AD9136 FMC EVALUATION BOARD			
HARDWARE SYSTEMS -		<PRODUCT>			
TEST ENGINEER -		<PRODUCT_1>			
COMPONENT ENGINEER -		<DRAWING_TITLE1>			
TEST PROCESS -		<DRAWING_TITLE2>			
HARDWARE RELEASE -		<DRAWING_TITLE3>			
DESIGNER -		<DRAWING_TITLE4>			
PTD ENGINEER <PTD_ENGINEER>		<DRAWING_TITLE5>			
CHECKER -		MASTER PROJECT TEMPLATE <DRAWING_TITLE6>	TESTER TEMPLATE -	DRAWING NO. HSC 14018	REV. A
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		SIZE D	SCALE <SCALE>
		DECIMALS X.XX +0.010 X.XXX +0.005	FRACTIONS +1/32	ANGLES +2	CODE ID NO. SHEET 1 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



	SCHEMATIC		
	AD9136 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 14018	REV A
PTD ENGINEER <PTD_ENGINEER>	SCALE <SCALE>	SHEET 2 OF 8	

REVISIONS			
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	SCHEMATIC		
	AD9136 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 14018	REV A
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	
		SHEET 3 OF 8	

FMC

P1
ASP-134488-01

P1
ASP-134488-01

P1
ASP-134488-01

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ASP-134488-01

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ASP-134488-01

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

D

D

C

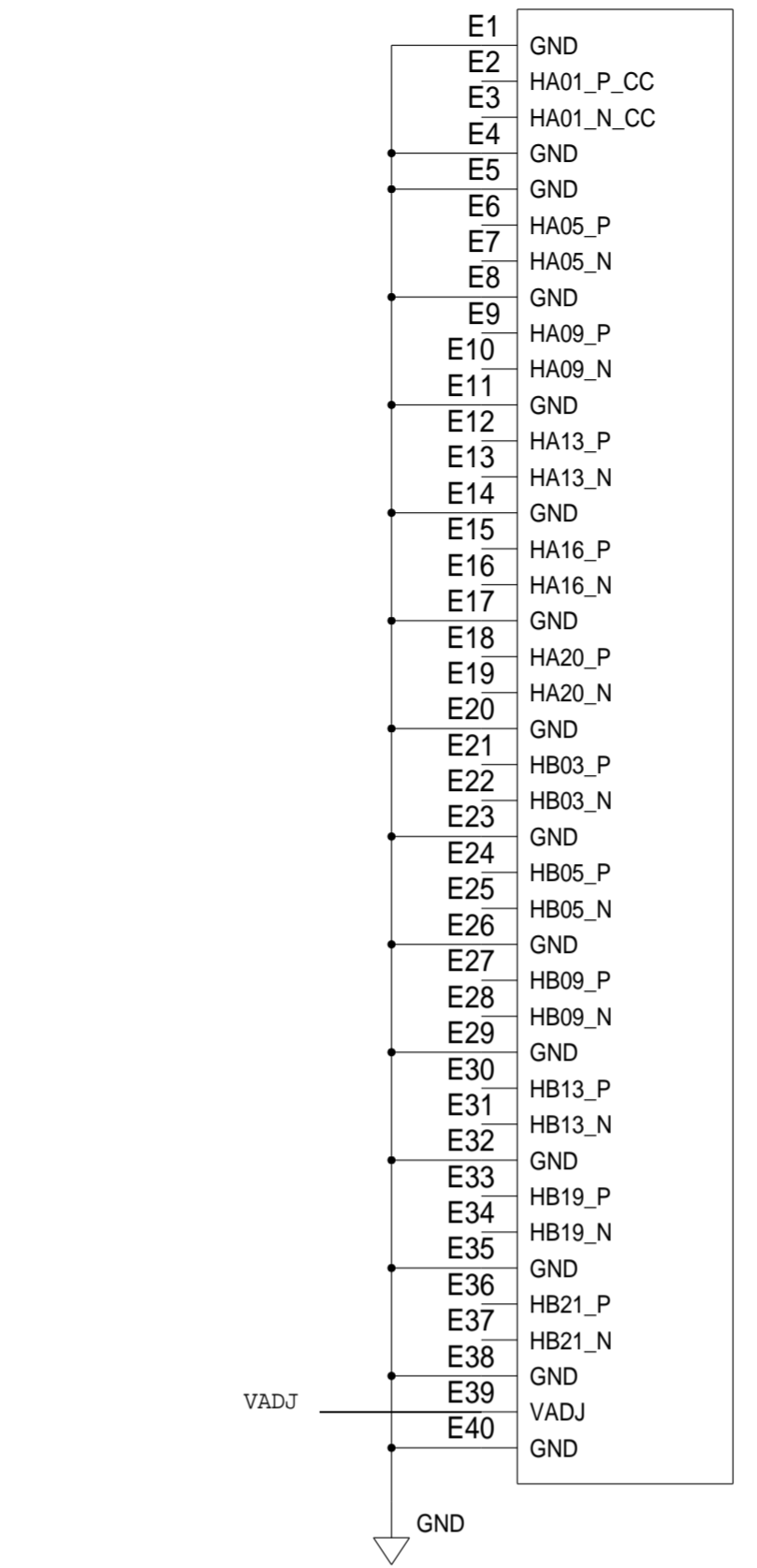
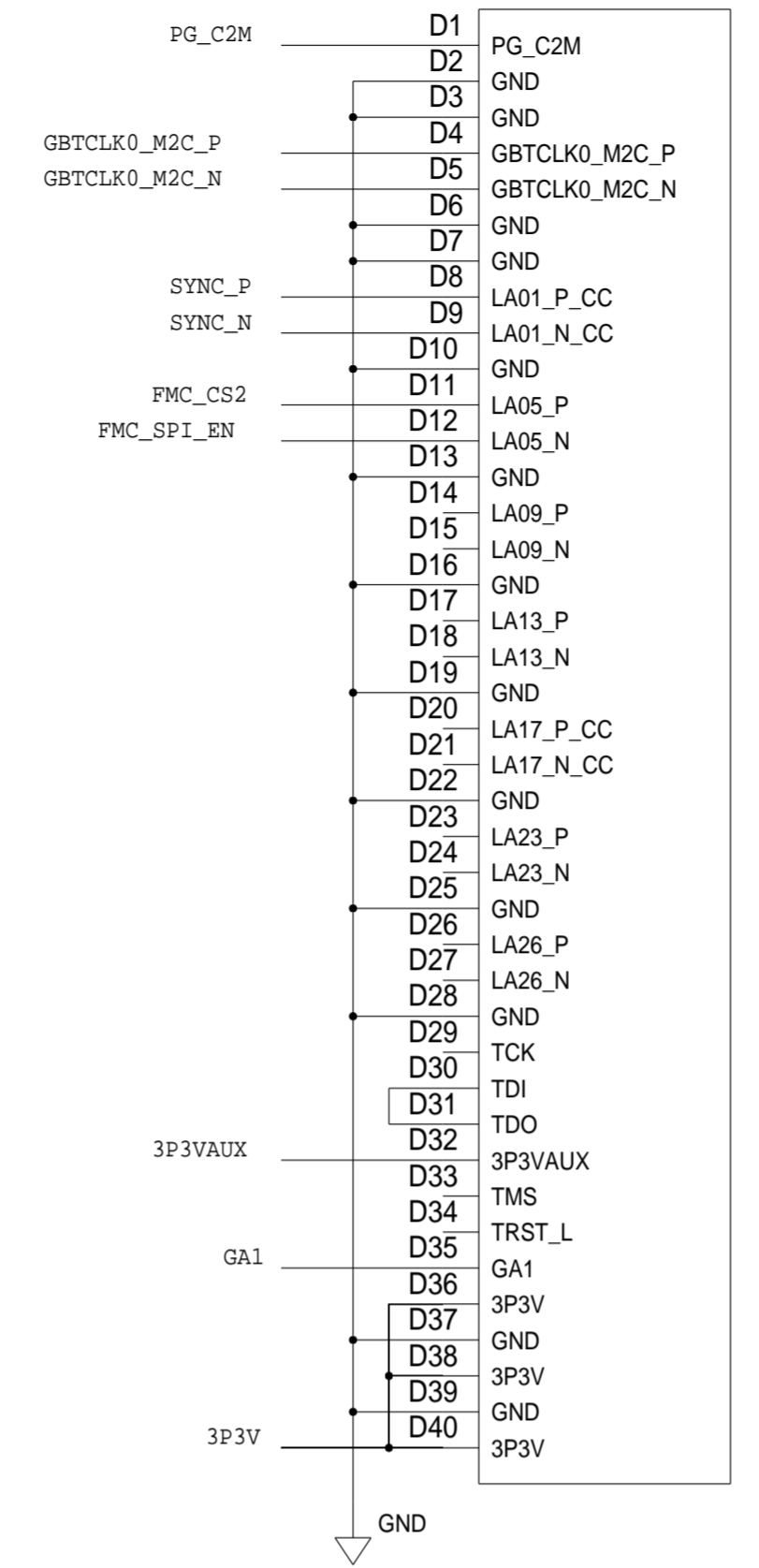
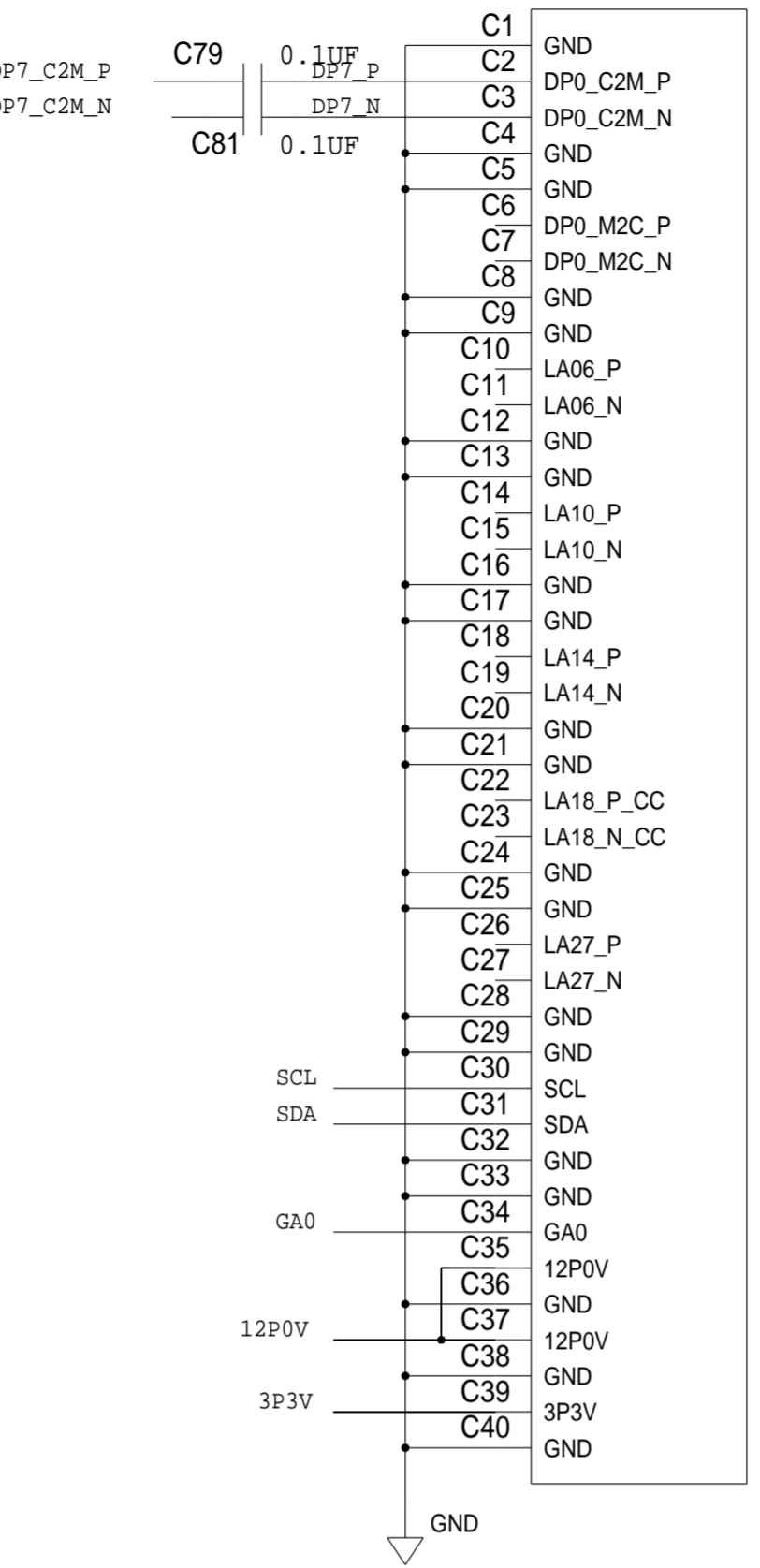
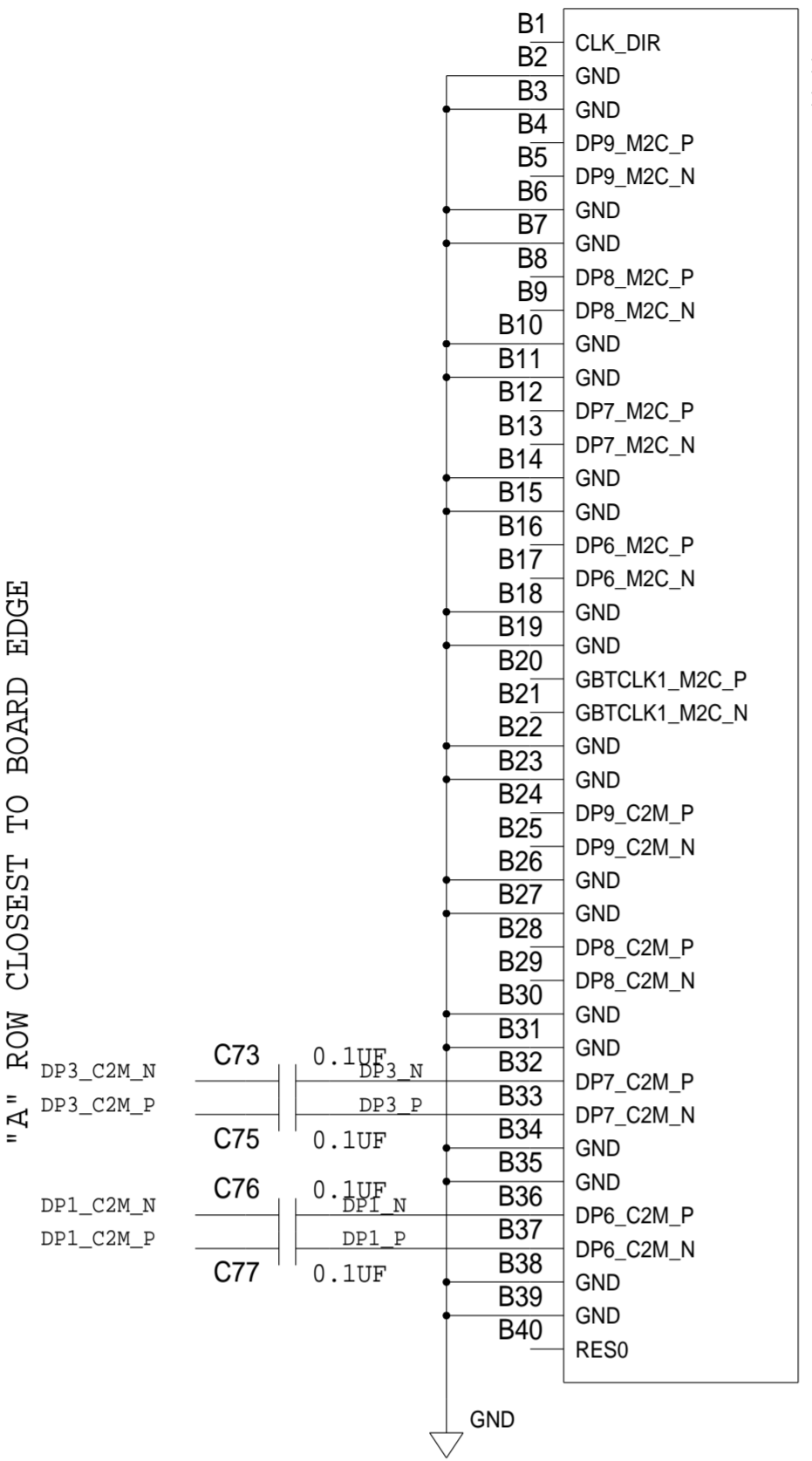
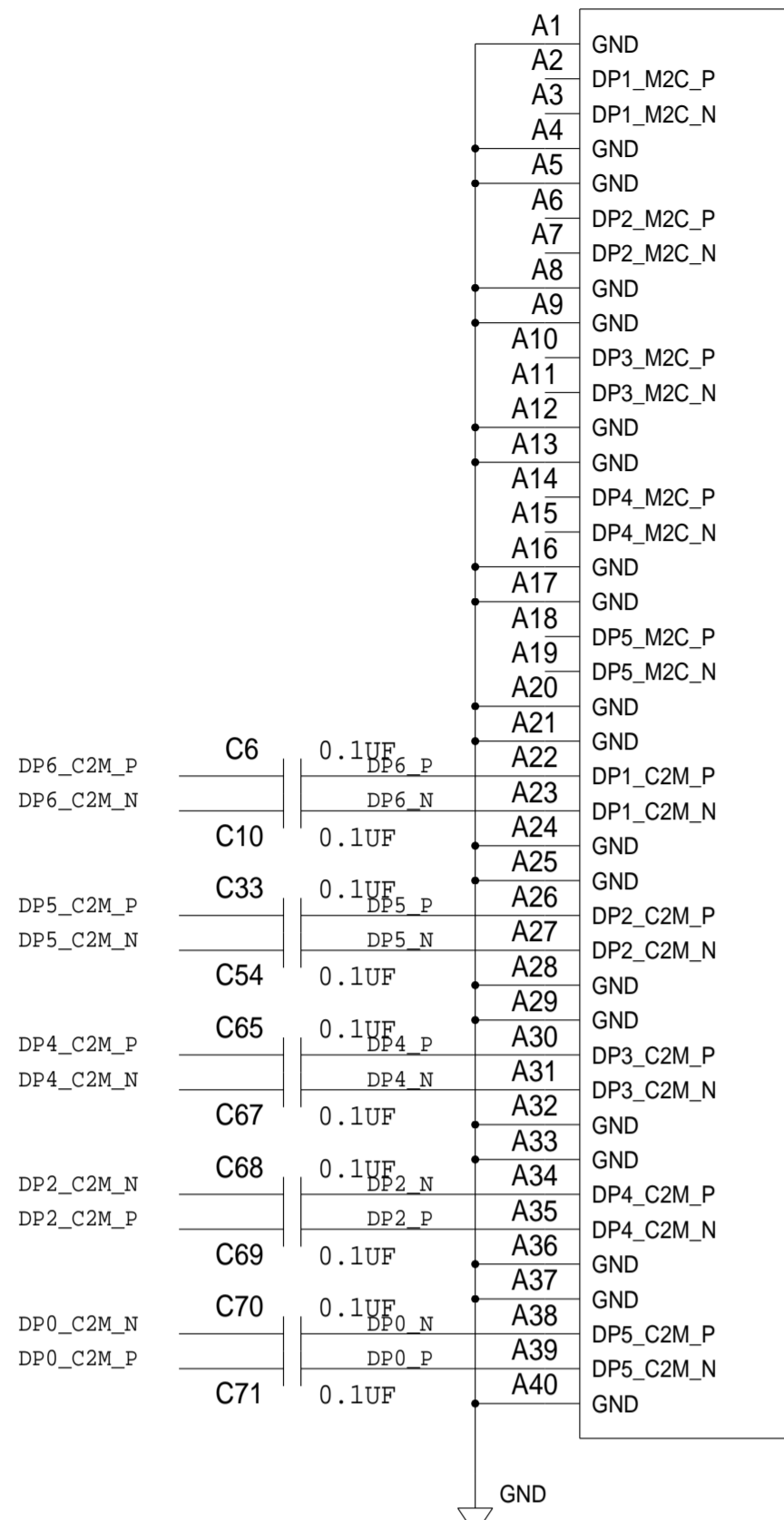
C

B

B

A

A



ON 3P3V, 12P0V, AND VADJ, HAVE PIN-HEADER JUMPER BETWEEN FMC PINS AND REST OF BOARD, TO ALLOW FOR CURRENT MEASUREMENT PER RAIL.

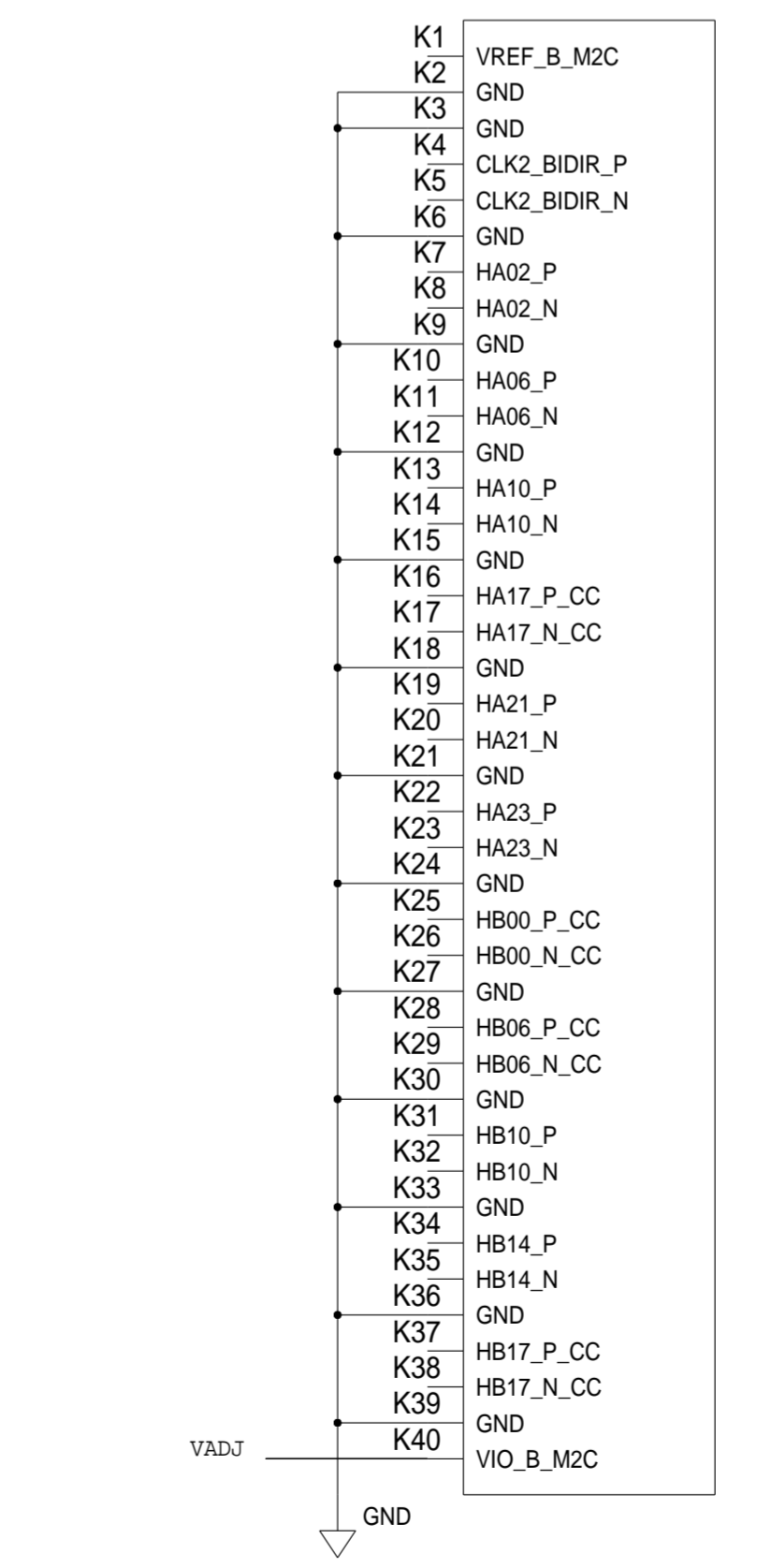
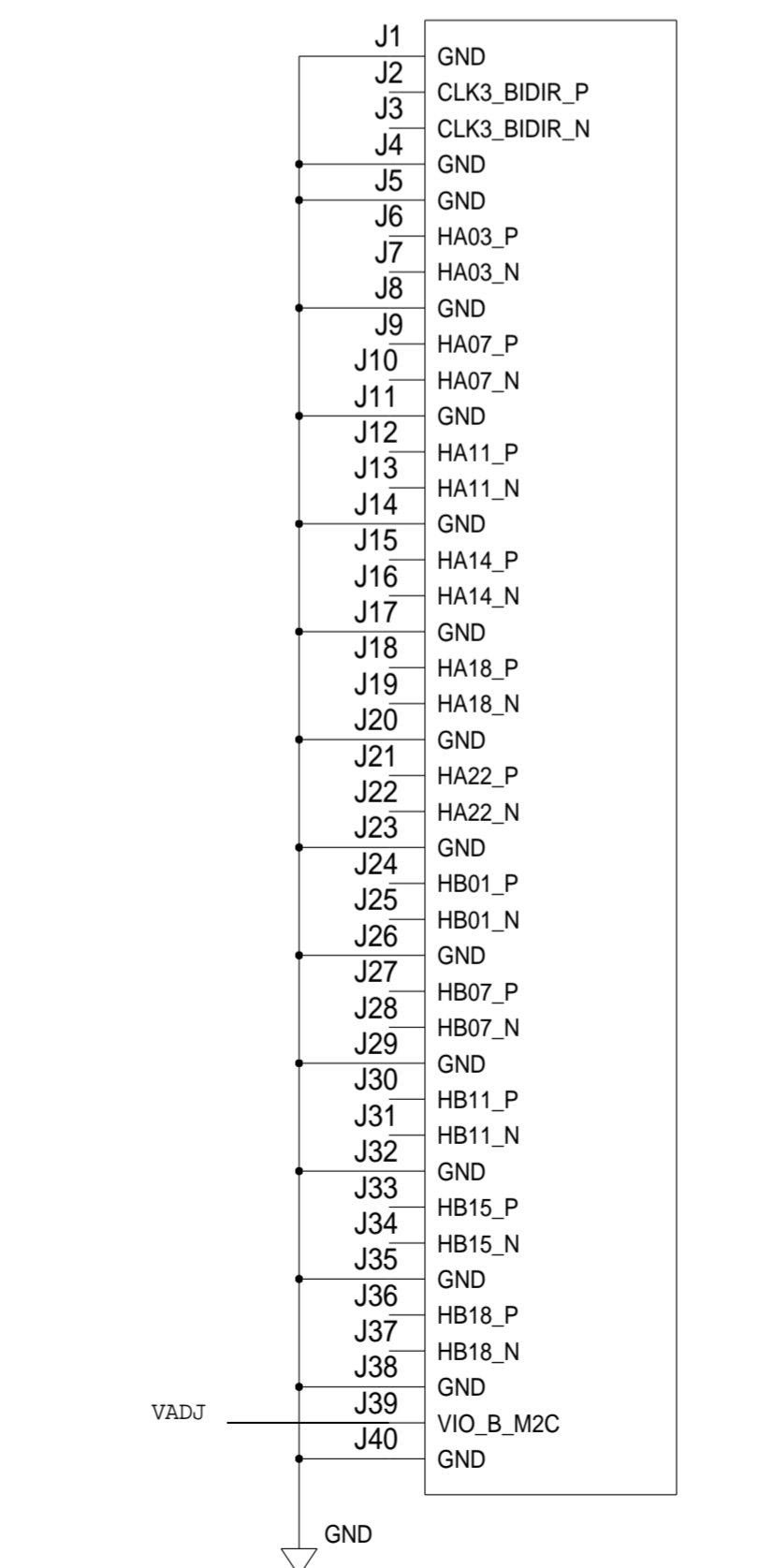
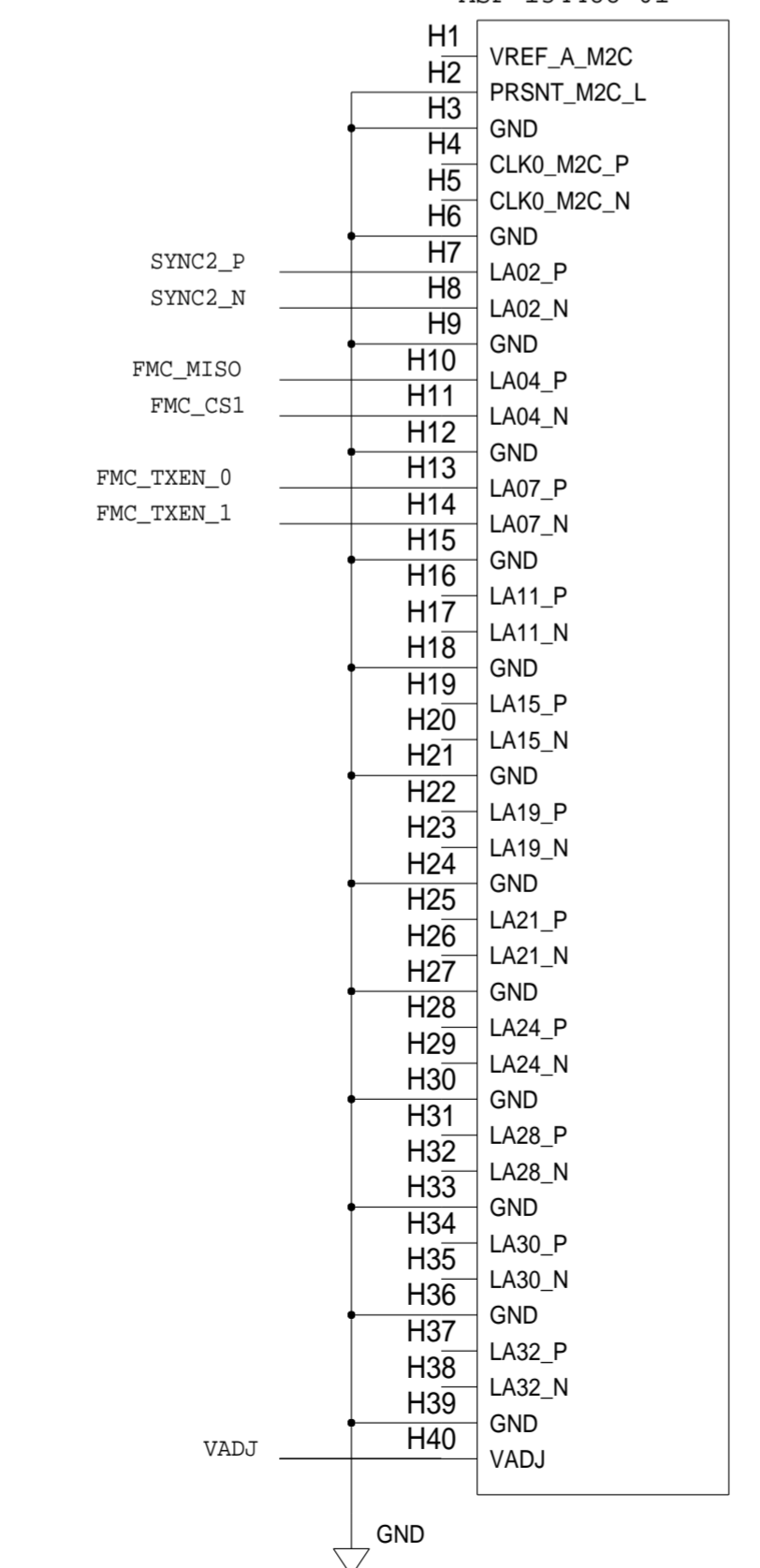
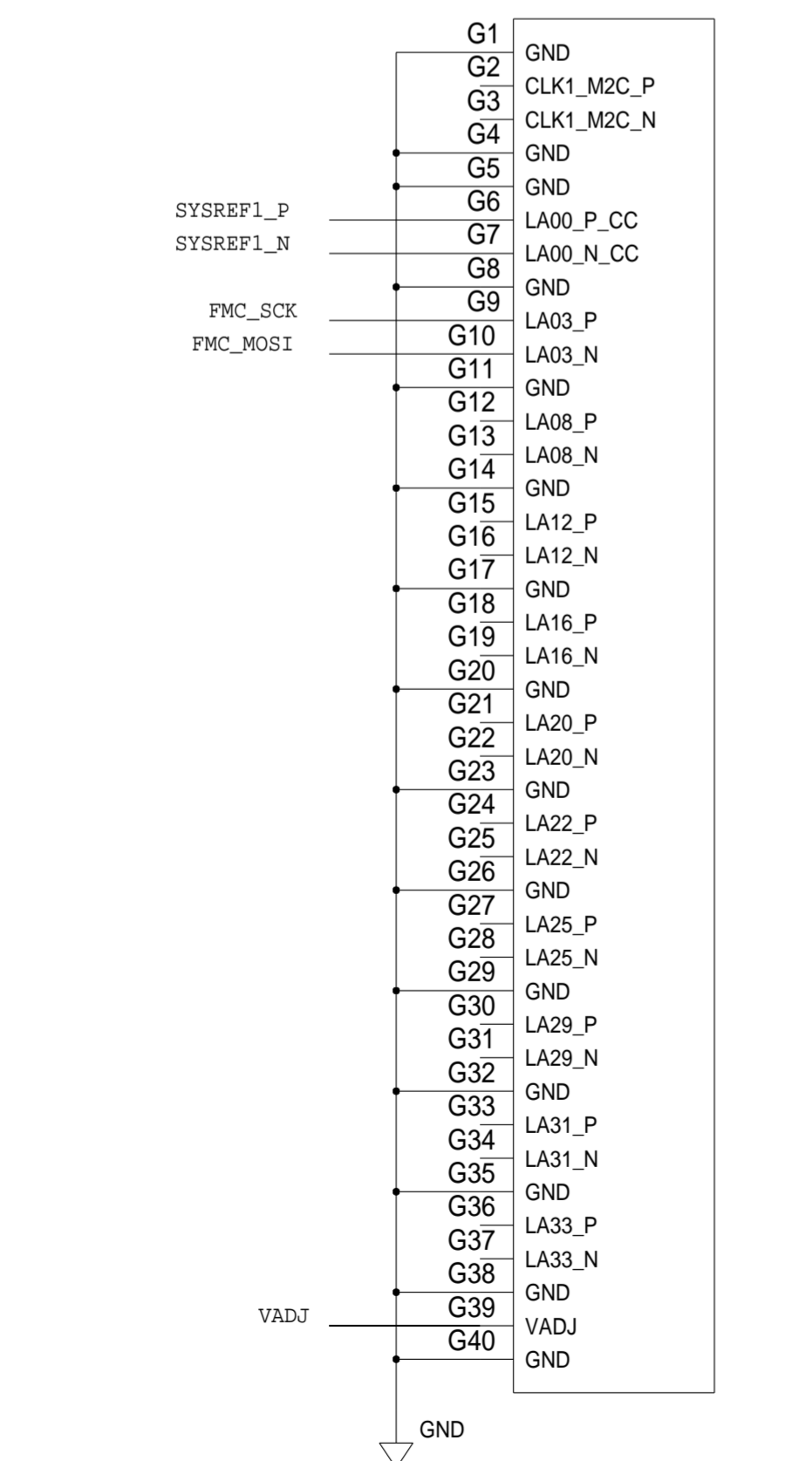
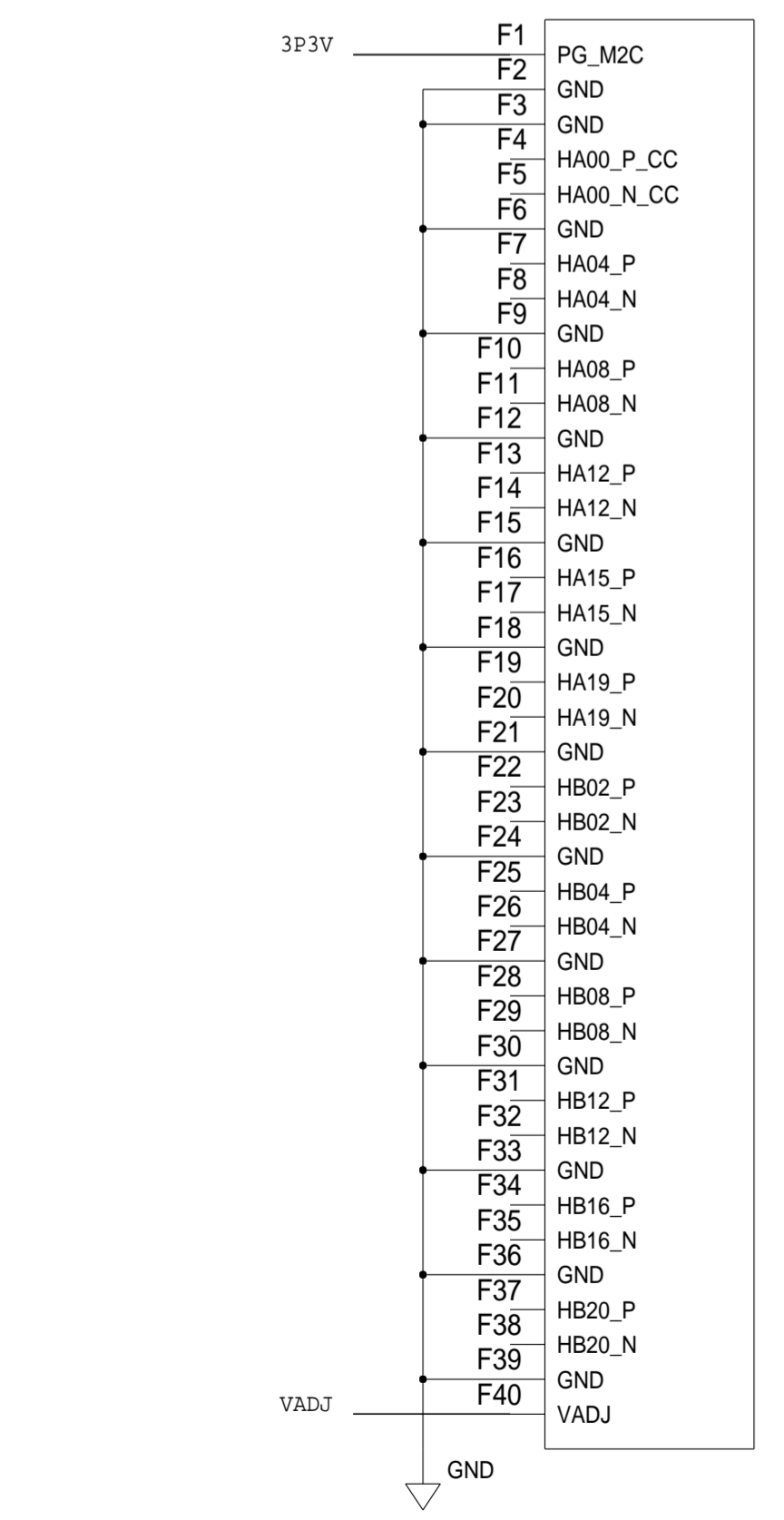
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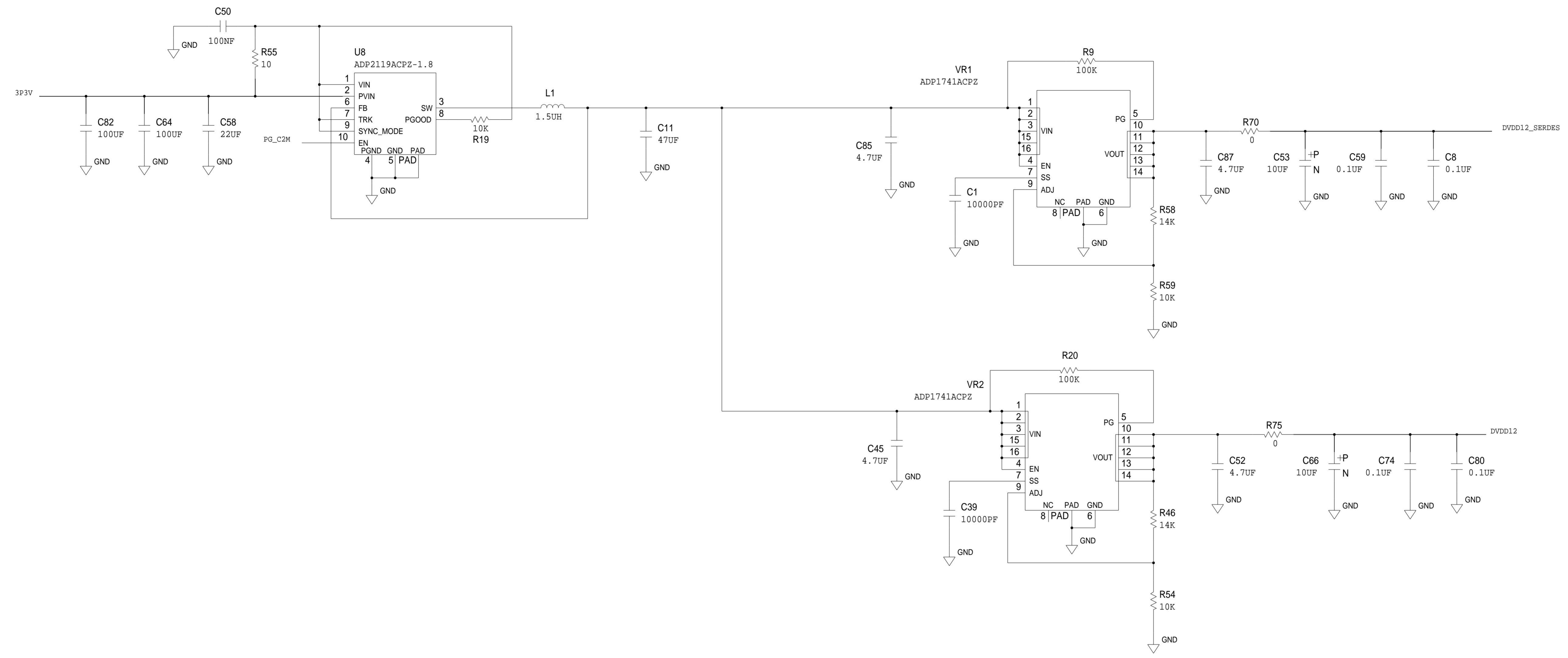
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ASP-134488-01



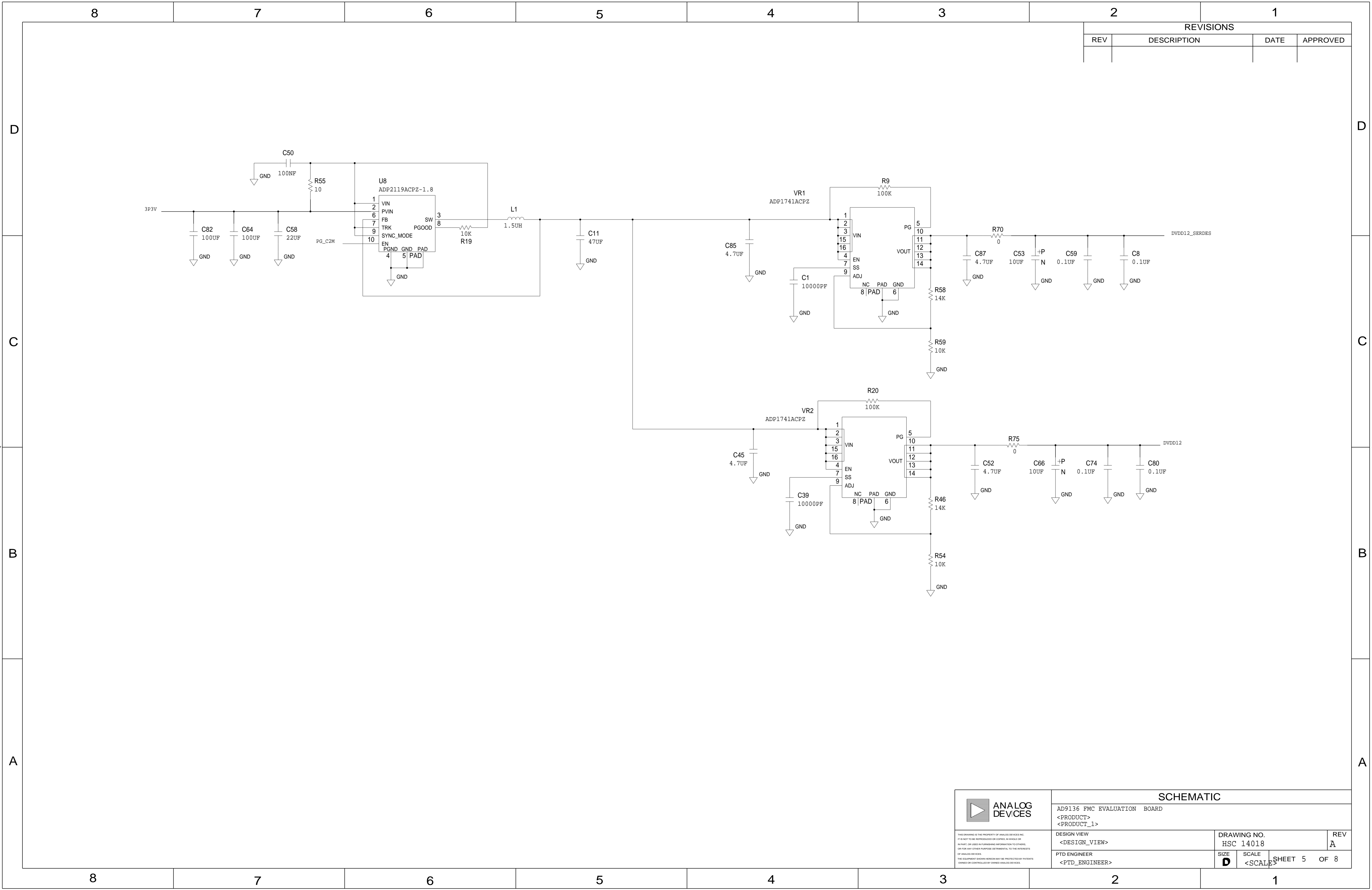
VIO_B_M2C PINS SHOULD HAVE WIDE ETCH CONNECTION TO VADJ PINS

	SCHEMATIC		
	AD9136 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 14018	REV A
PTD ENGINEER <PTD_ENGINEER>	SCALE <SCALE>	SHEET 4 OF 8	

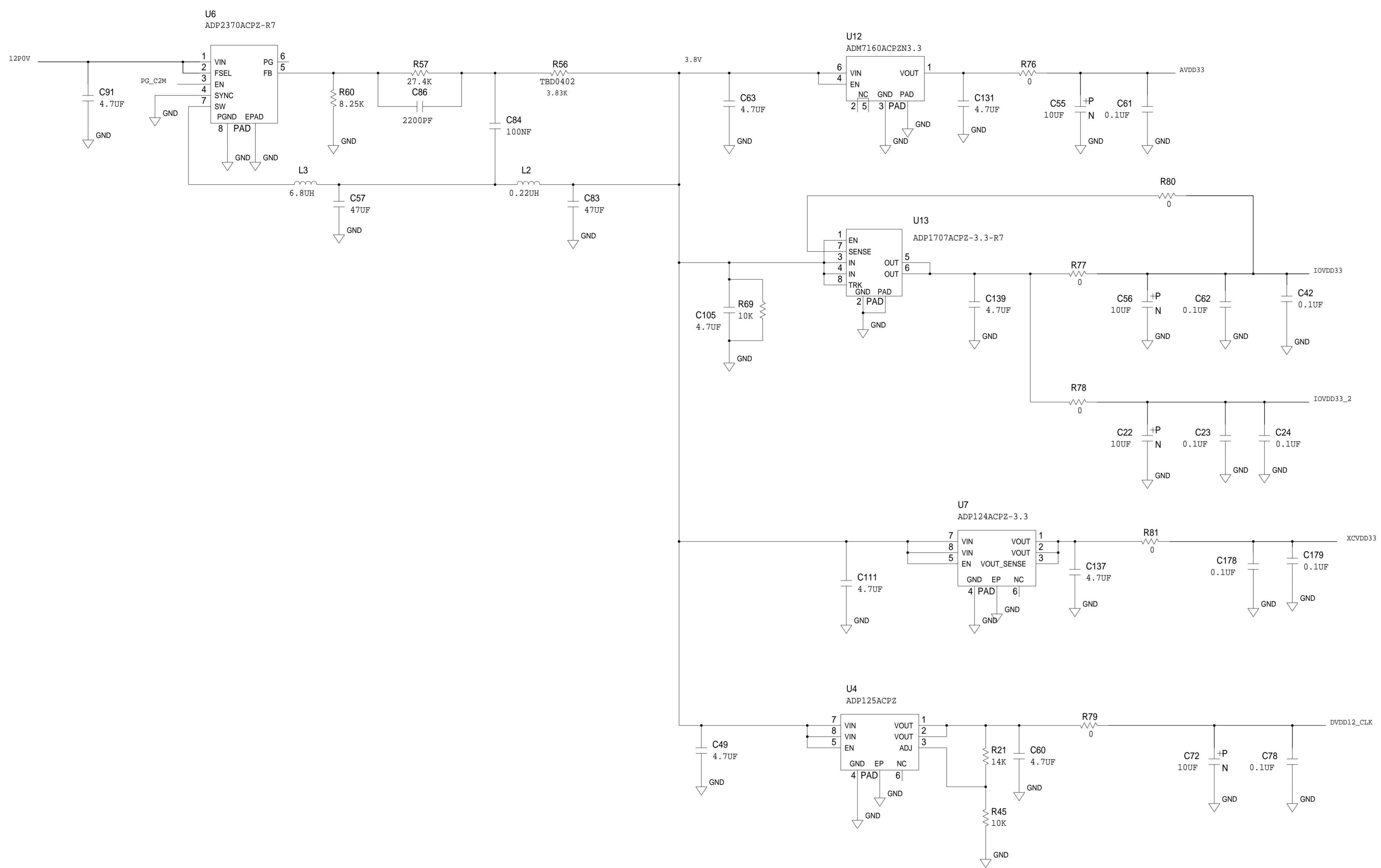
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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	AD9136 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 14018	REV A
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	
SHEET 5 OF 8			

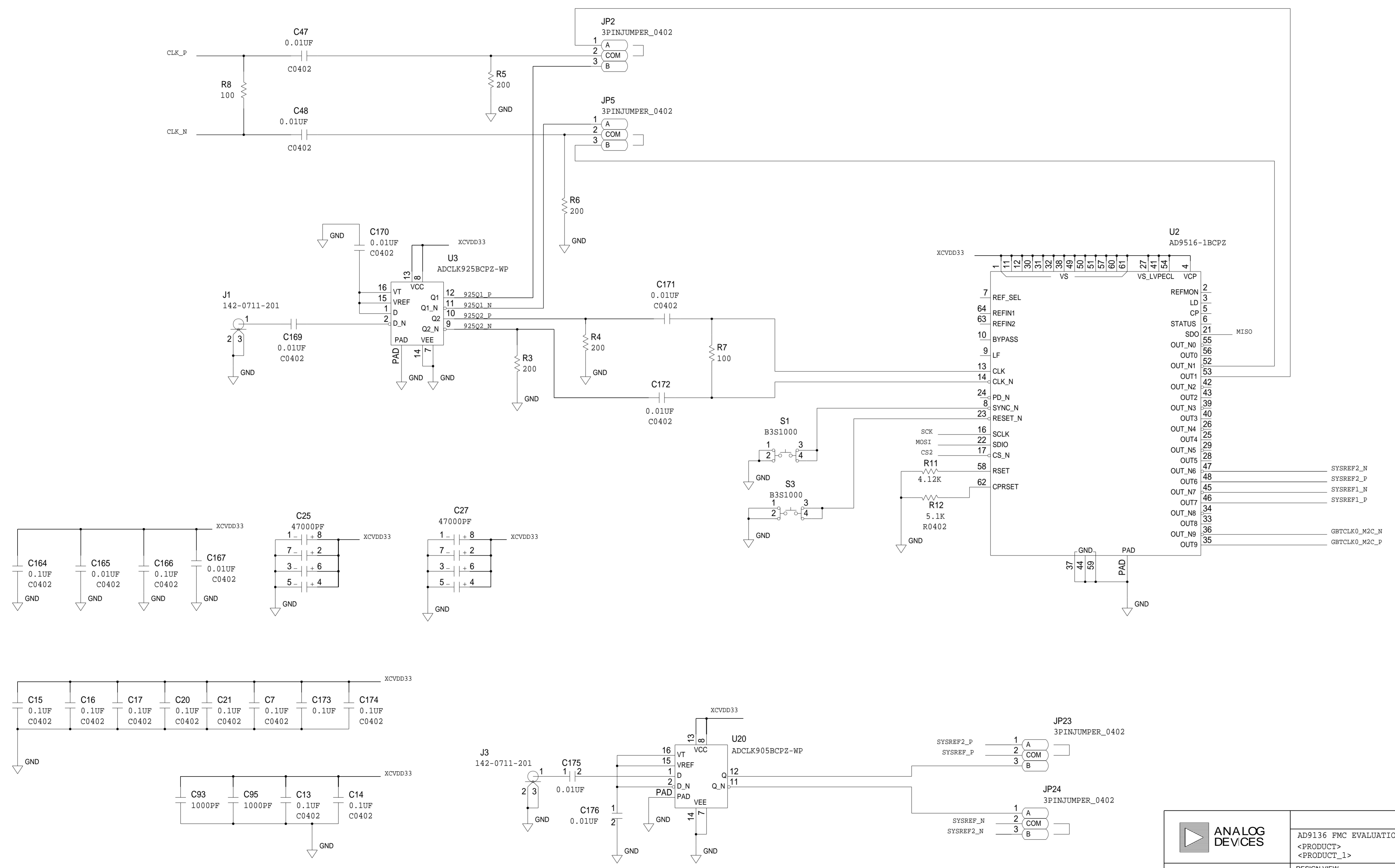


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	SCHEMATIC		
	AD9136 FMC EVALUATION BOARD		
	<PRODUCT> <PRODUCT_1>		
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 6 OF 8

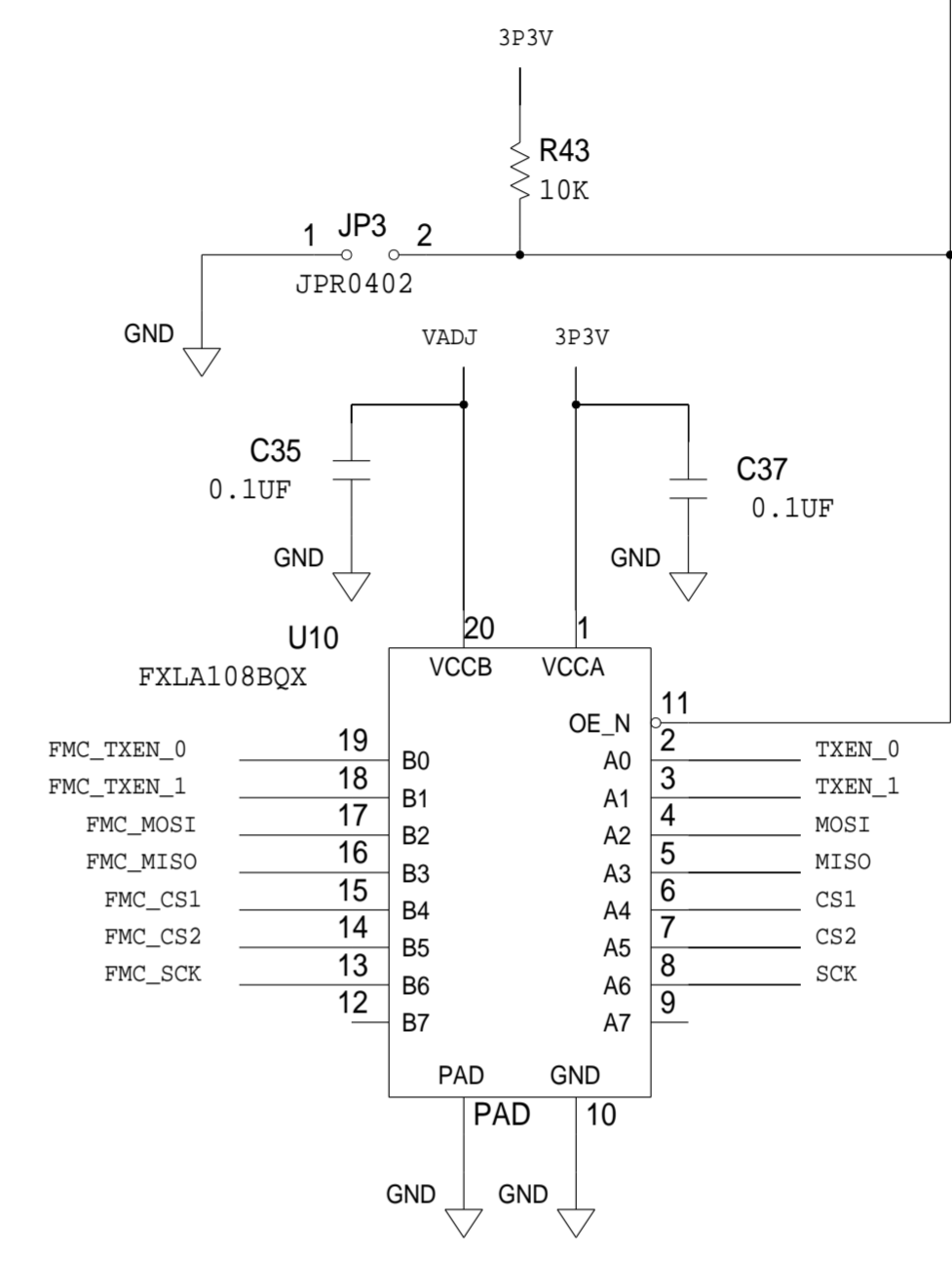
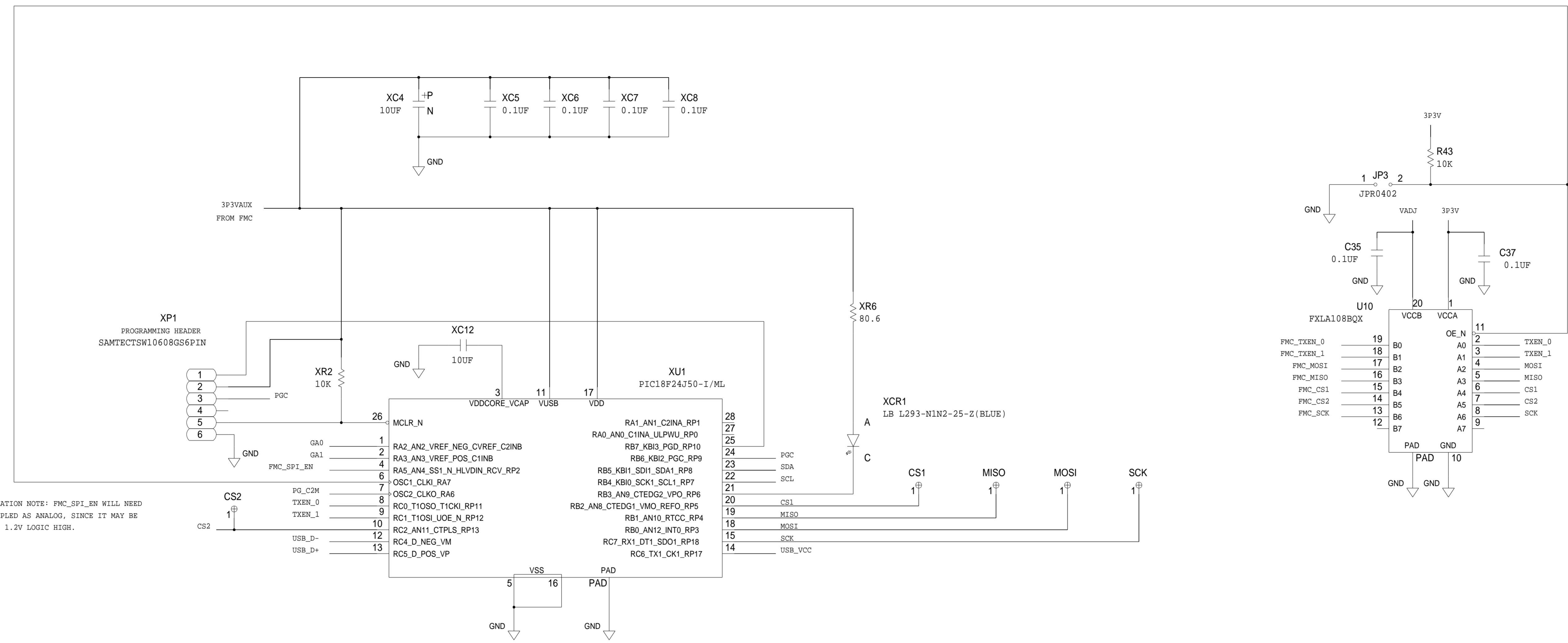
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	<PRODUCT> <PRODUCT_1>		
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	
		SHEET 7 OF 8	

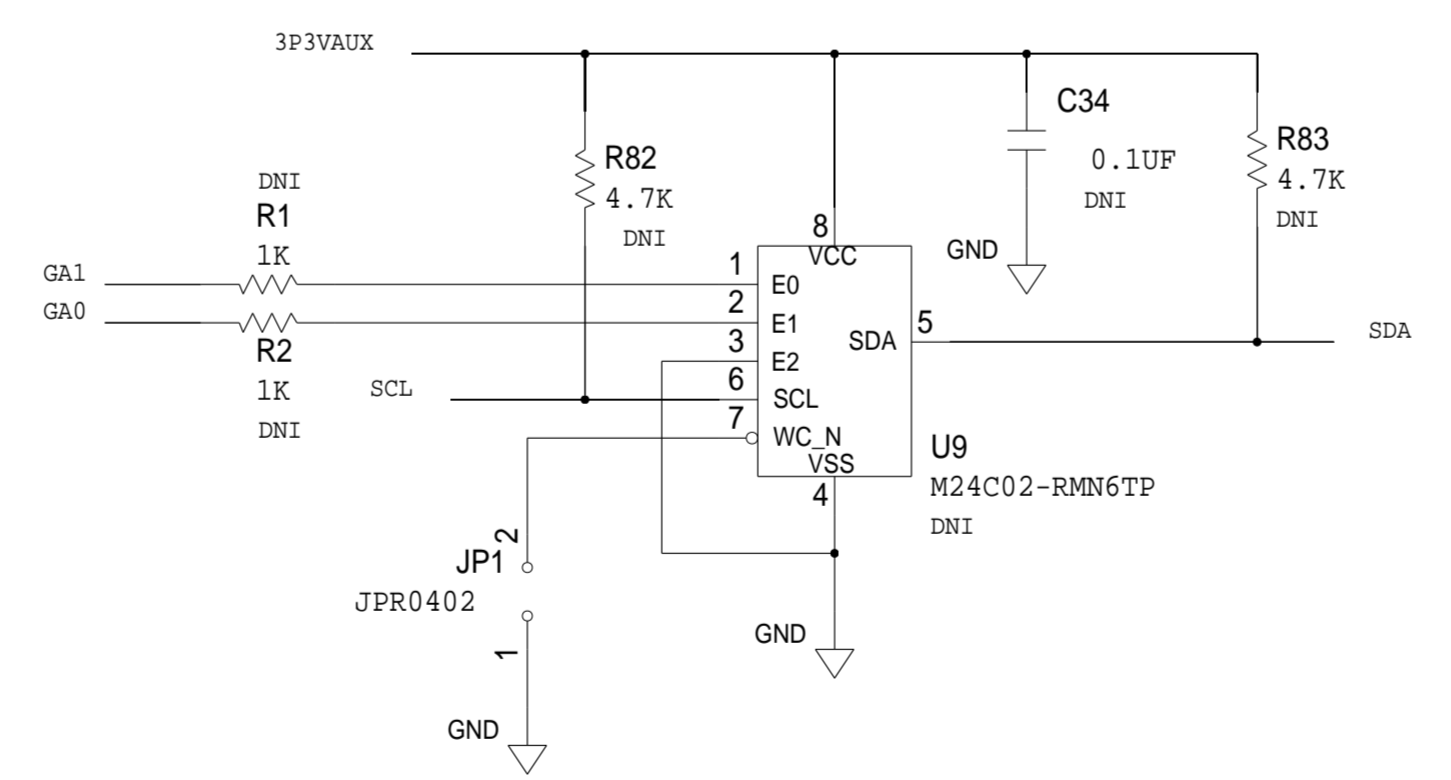
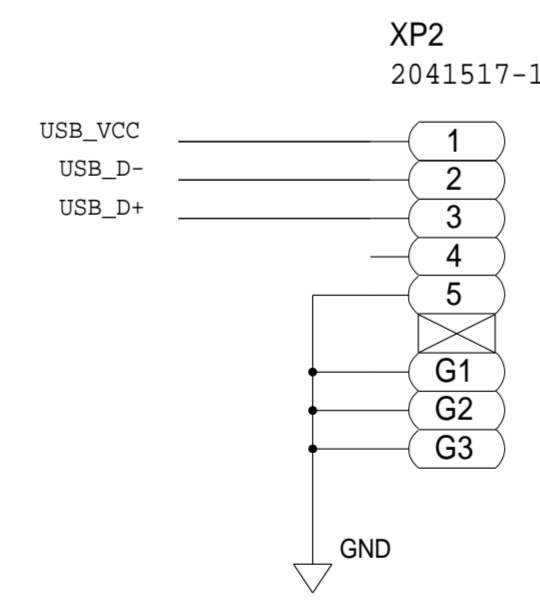
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IMPLEMENTATION NOTE: FMC_SPI_EN WILL NEED TO BE SAMPLED AS ANALOG, SINCE IT MAY BE AS LOW AS 1.2V LOGIC HIGH.

NOTE:
 IF USB CABLE IS PLUGGED IN PIC IS THE SOURCE OF SPI BUS AND TXEN SIGNALS
 IF USB IS UNPLUGGED FMC INTERFACE IS THE SOURCE OF SPI BUS AND TXEN SIGNAL.



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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 8 OF 8