

General Information

Triggered capture capability is designed into the ADS8-V1 for most ADCs that use this capture platform. This is an unadvertised capability which is provided as-is, without guarantee of support, functionality, or performance. This information will hopefully help users who need triggered capture. Users will need to try it, test it, and get it to work in their application.

General ADS8-V1 triggered capture information and procedure:

- ▶ The ADS8-V1 external trigger feature is enabled by setting an FPGA register bit. The address is Register 0x106 Bit1. Keep in mind that this register is on the FPGA on the ADS8-V1. It is not an ADC register.
- ▶ SMA connector J2 on the ADS8-V1 is the trigger input so that the data capture start time can be controlled. The trigger requires an active high 1.8V pulse width that is longer than the FPGA internal peripheral clock period, which usually has a frequency of 50 MHz.
- ▶ SMA connector J3 is used as a system ready indicator when triggered capture is enabled. It indicates that the FPGA is ready to accept an external trigger on J2. This is an active high signal.

The Sequence

1. The FPGA Register 0x106 Bit1 = 1.
2. Initiate the capture.
3. Wait for the ready signal on J3.
4. Apply the trigger to J2.

It is likely that experimentation with trial-and-error will be needed to get this to work.