RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

1-APRIL-2014

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

	DATE
TEMPLATE ENGINEER P ALONGI	
HARDWARE SERVICES -	
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER -	
TEST PROCESS -	
HARDWARE RELEASE -	
DESIGNER -	
PTD ENGINEER <PTD_ENGINEER>	
CHECKER -	

SCHEMATIC

ANALOG DEVICES

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>
<DRAWING_TITLE1>
<DRAWING_TITLE2>
<DRAWING_TITLE3>
<DRAWING_TITLE4>
<DRAWING_TITLE5>

MASTER PROJECT TEMPLATE <DRAWING_TITLE6>
TESTER TEMPLATE -

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES

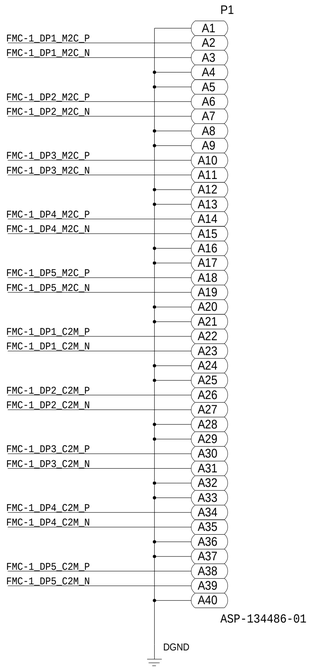
DECIMALS	FRACTIONS	ANGLES
X.XX +-0.010 X.XXX +-0.005	+-1/32	+-2

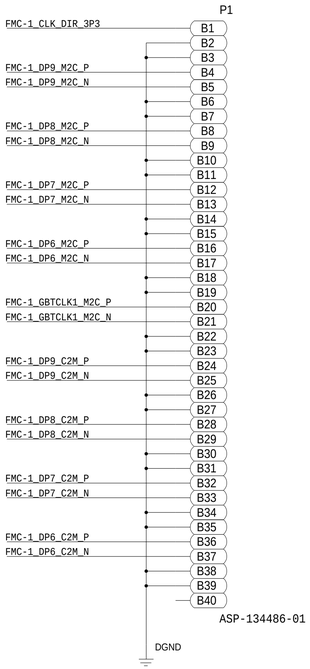
DRAWING NO. HSC 13052
REV. B

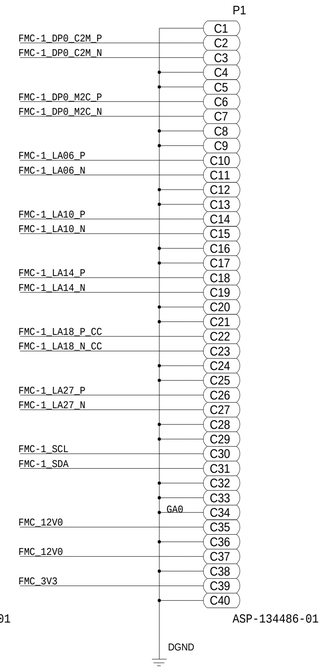
SIZE D | SCALE <SCALE>- | CODE ID NO. | SHEET 1 OF 23

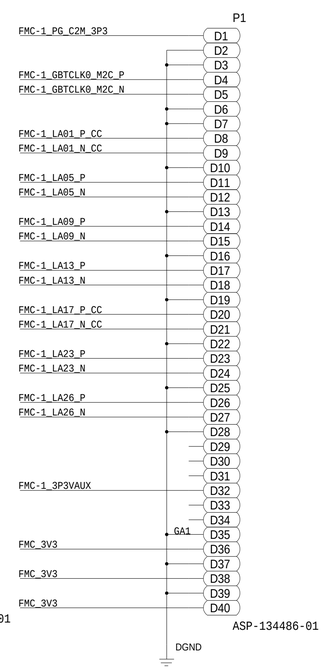
FMC CONNECTOR

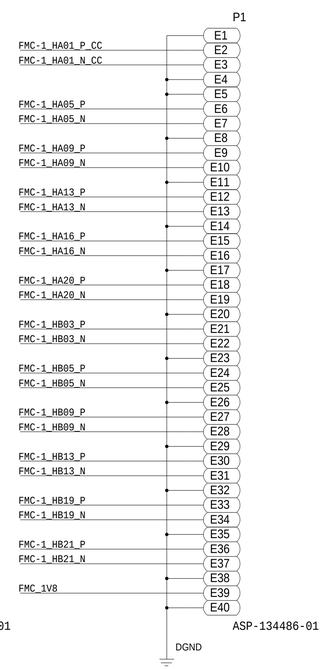
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



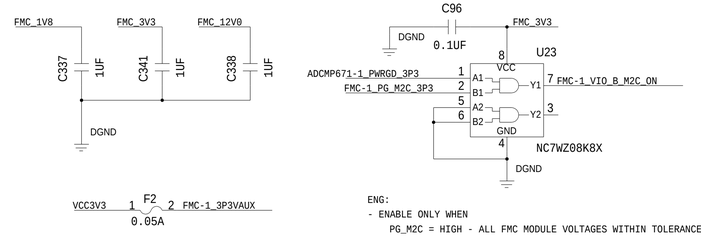






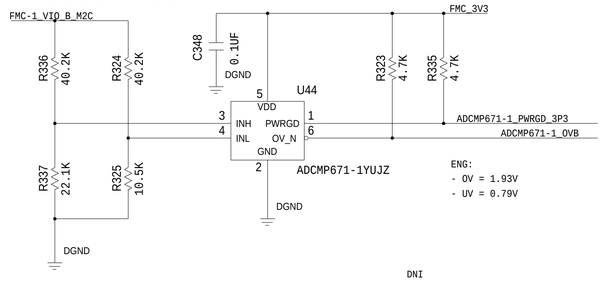


FMC VIO_B_M2C ENABLE LOGIC



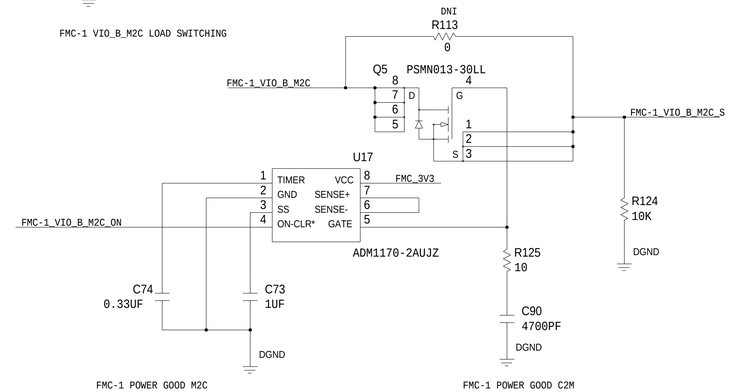
ENG:
- ENABLE ONLY WHEN
  PG_M2C = HIGH - ALL FMC MODULE VOLTAGES WITHIN TOLERANCE
  ADCMP671_OVB = HIGH - NO VIO_B_M2C OV CONDITION

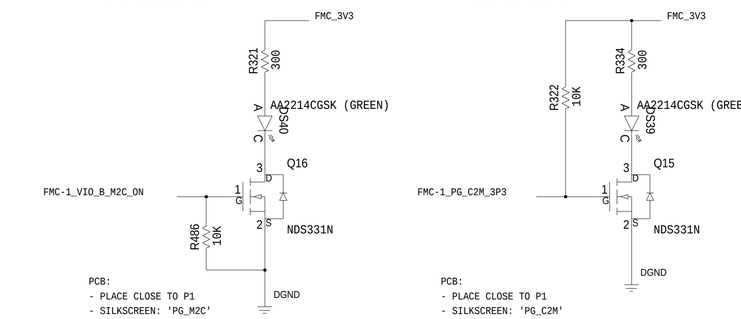
FMC-1 VIO_B_M2C OV PROTECTION

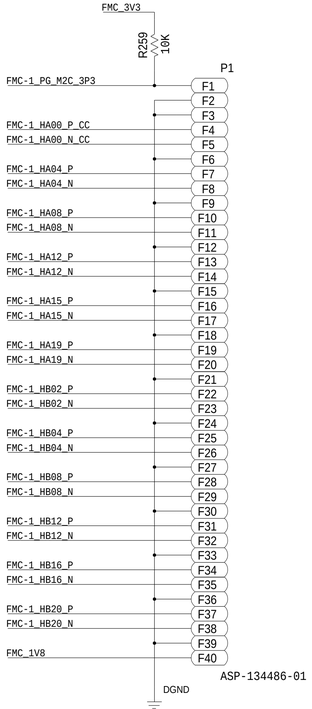


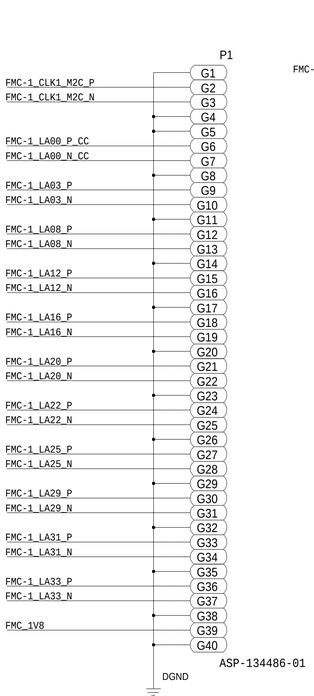
ENG:
- OV = 1.93V
- UV = 0.79V

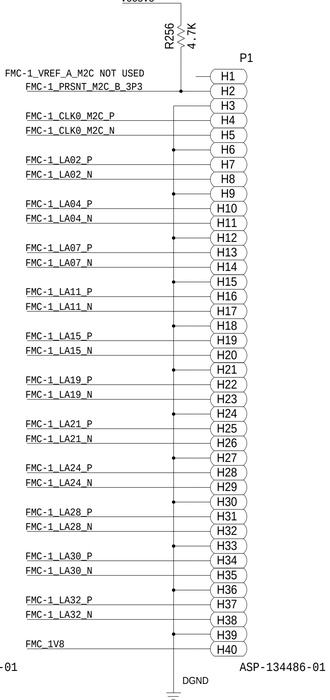
FMC-1 VIO_B_M2C LOAD SWITCHING

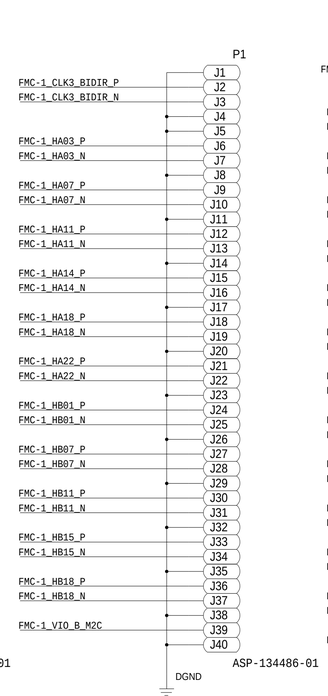


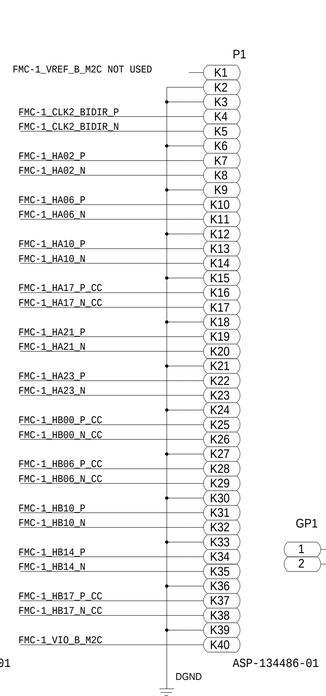








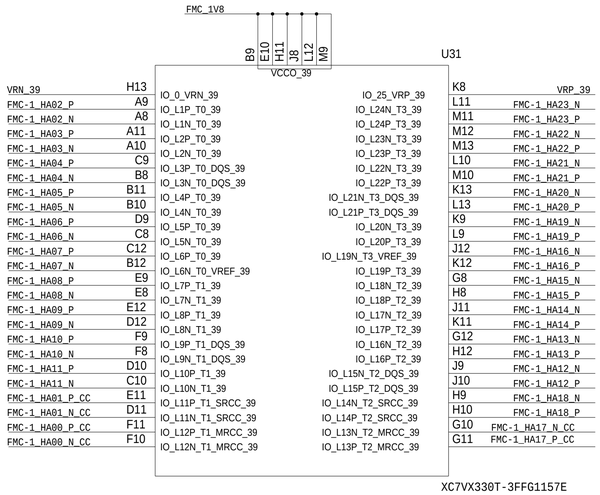


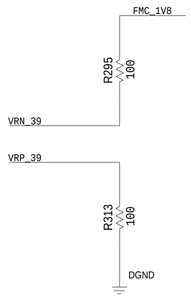


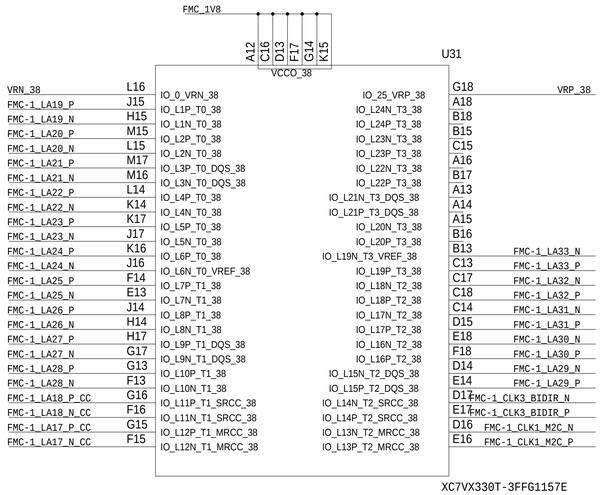
ANALOG DEVICES	SCHEMATIC
	ADS7-V2 BOARD <PRODUCT> <PRODUCT_1>
	DESIGN VIEW <DESIGN_VIEW> / DRAWING NO. HSC 13052 / REV B PTD ENGINEER <PTD_ENGINEER> / SIZE D / SCALE <SCALE> / SHEET 2 OF 23

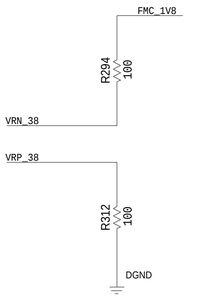
FMC BANKS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

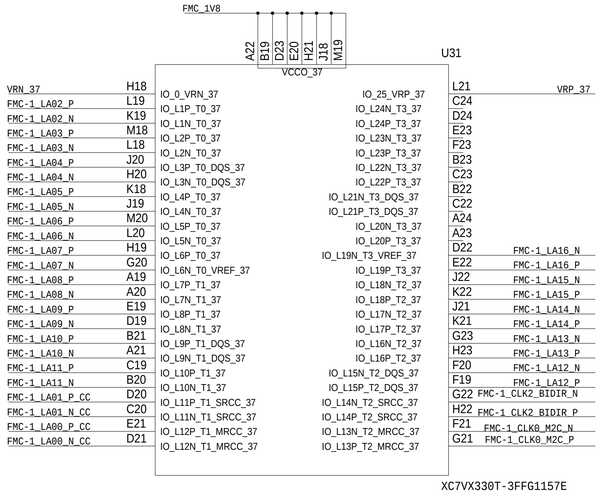


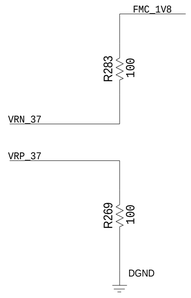


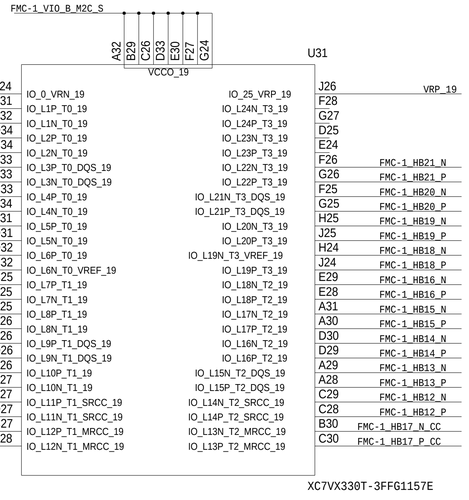


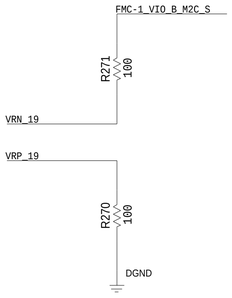


PCB:
- HA, HB AND LA BUS SIGNALS CAN BE MOVED WITHIN THE BANK, EXCEPT FOR SIGNALS GOING TO _MRCC AN_SRCC IOS
- DIFFERENTIAL PAIRS SHALL BE KEPT TOGETHER AND CONNECT TO APPROPRIATE P AND N PIN ON FPGA









ANALOG DEVICES

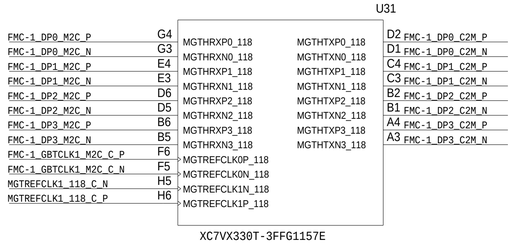
SCHEMATIC

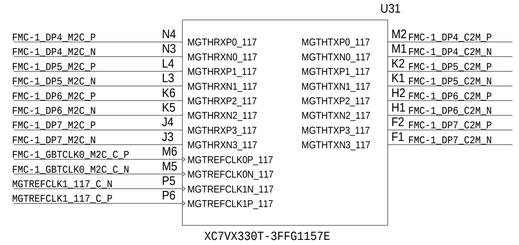
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

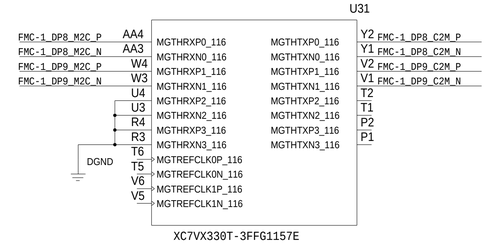
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13052	REV B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 3 OF 23

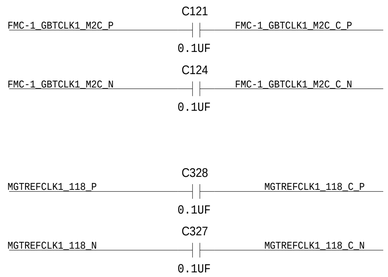
FMC MGT BANKS

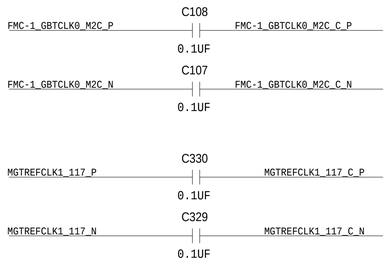
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

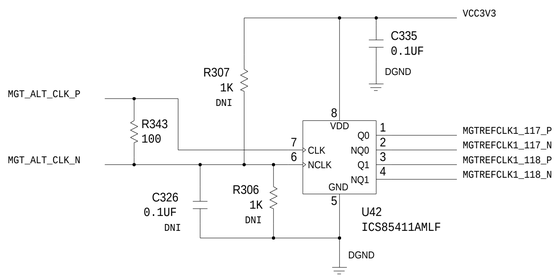


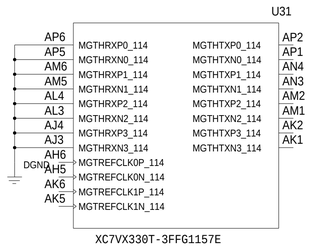


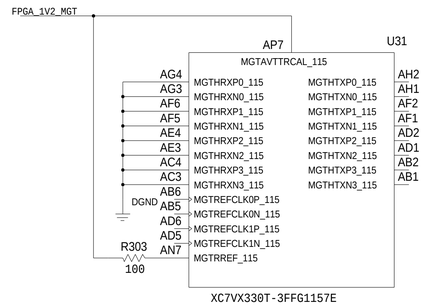












TRACE LENGTH FROM THE RESISTOR PINS TO THE FPGA PINS MGTRREF AND MGTAVTTRCAL MUST BE EQUAL IN LENGTH AND HAVE THE SAME GEOMETRY

ANALOG DEVICES

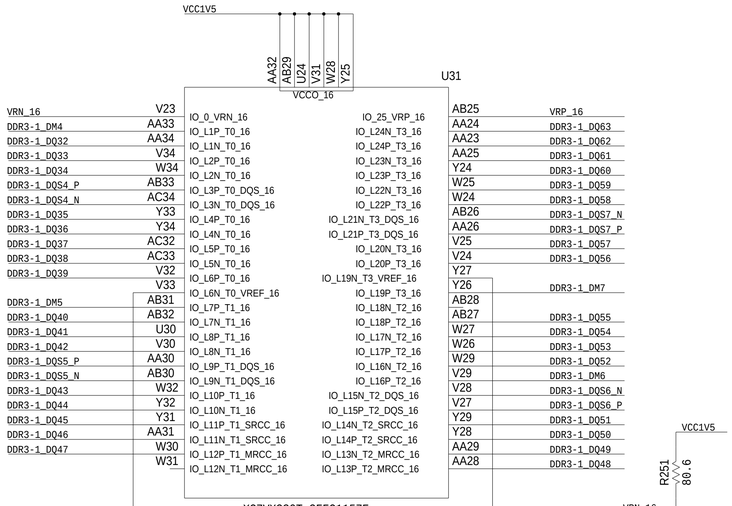
SCHEMATIC

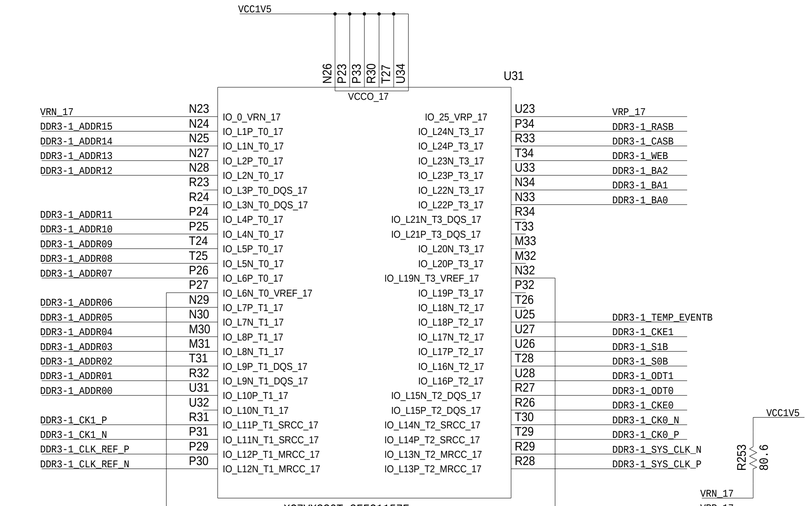
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

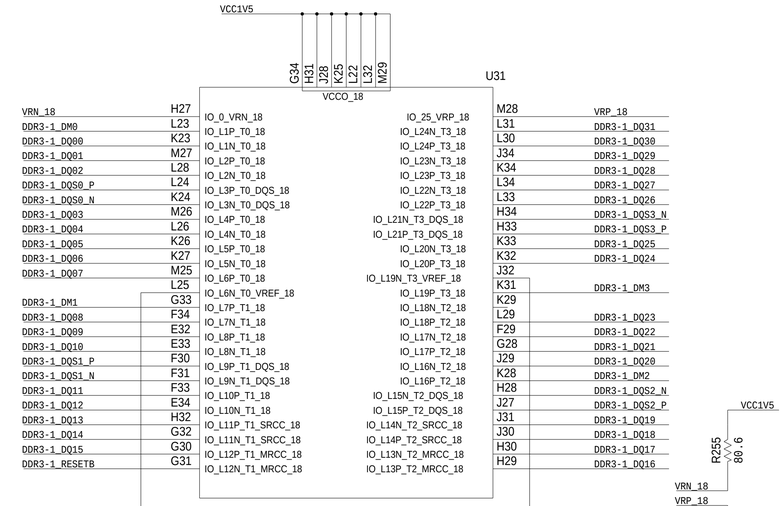
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 4 OF 23
<PTD_ENGINEER>	D / <SCALE>	

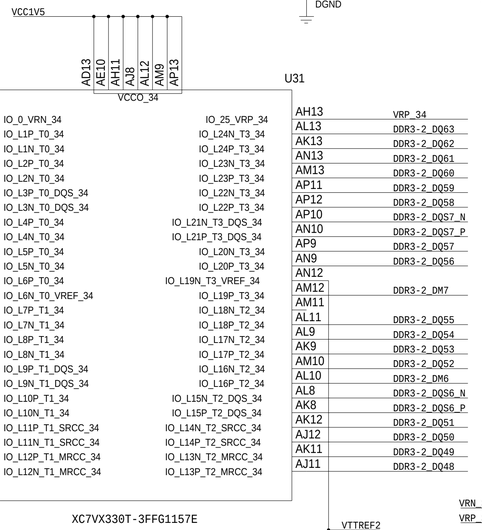
DDR3-1 AND DDR3-2 BANKS

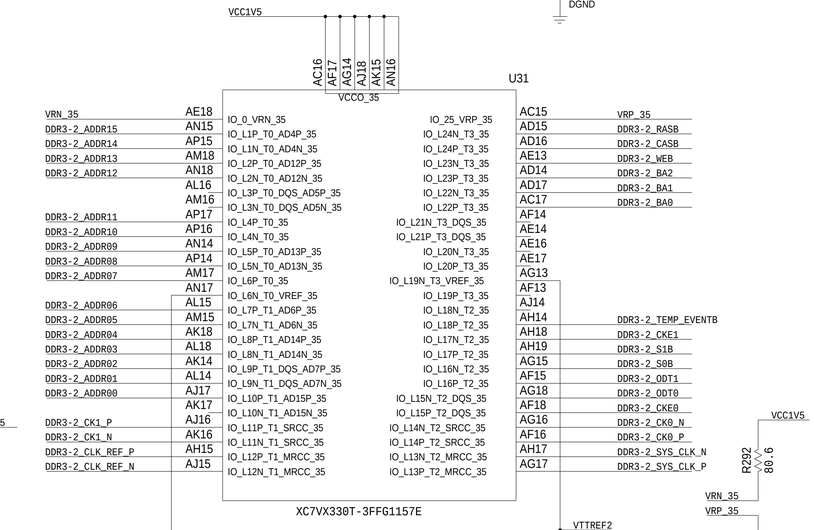
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

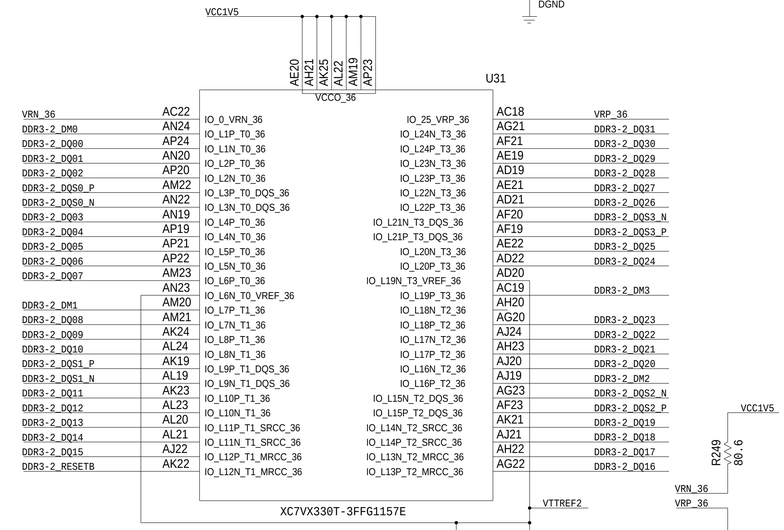












PCB:
- ALL DQ AND DM NETS IN A BYTE GROUP MUST BE MATCHED TO THEIR ASSOCIATED DQS NETS
- IT IS RECOMMENDED THAT THE TRANSMISSION LINE OF A DQ/DM NET BE MATCHED TO ITS ASSOCIATED DQS NET WITHIN +-5 PS
- ALL ADDR, CMD, AND CONTROL SIGNALS MUST BE MATCHED TO THE CK CLOCK SIGNAL WITHIN +- 5 PS
- PLACE VTTREF DECOUPLING CAPS AS CLOSE AS POSSIBLE TO RELEVANT FPGA PINS
- VRN/VRP TRACES SHOULD BE MATCHED AND SHOULD BE AS SHORT AS POSSIBLE

ANALOG DEVICES

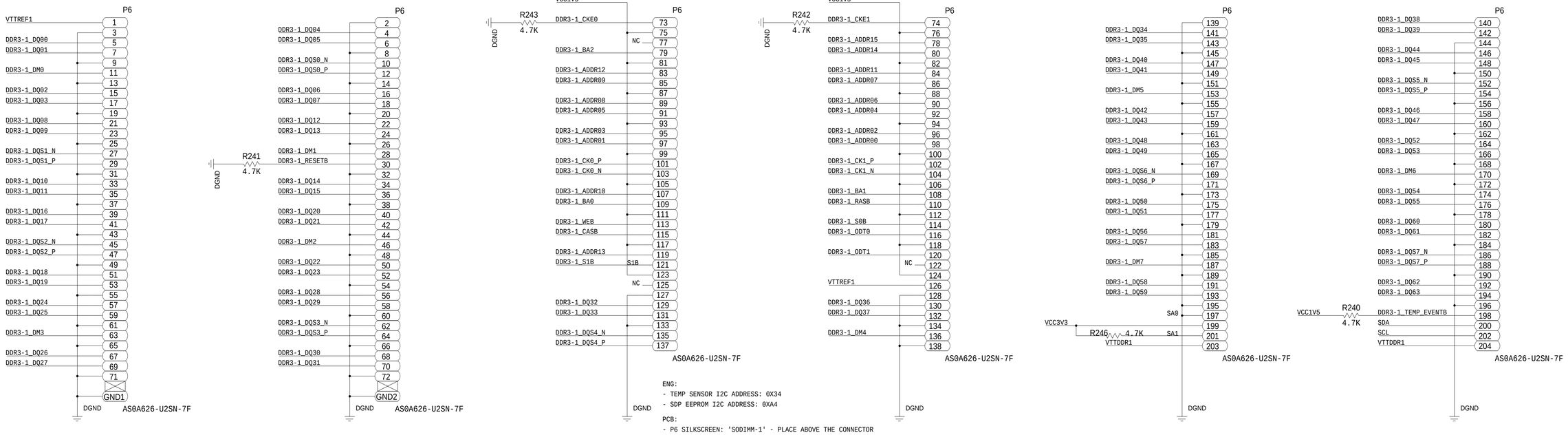
SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE: D / SCALE: <SCALE>	SHEET 5 OF 23
<PTD_ENGINEER>		

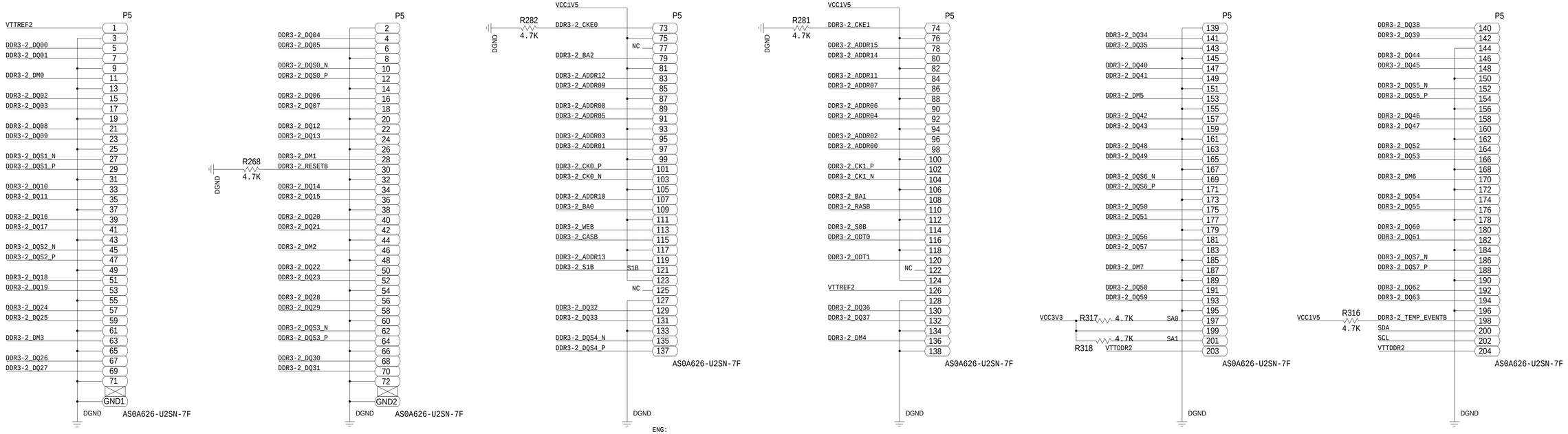
DDR3-1 AND DDR3-2 SODIMM

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ENG:
- TEMP SENSOR I2C ADDRESS: 0X34
- SDP EEPROM I2C ADDRESS: 0XA4

PCB:
- P6 SILKSCREEN: 'SODIMM-1' - PLACE ABOVE THE CONNECTOR



ENG:
- TEMP SENSOR I2C ADDRESS: 0X36
- SDP EEPROM I2C ADDRESS: 0XA6

PCB:
- P5 SILKSCREEN: 'SODIMM-2' - PLACE ABOVE THE CONNECTOR

ANALOG DEVICES

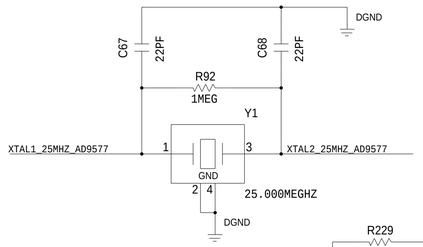
SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

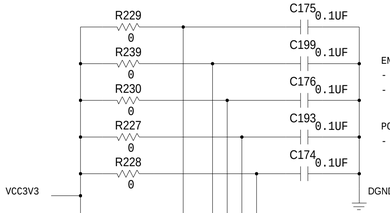
DESIGN VIEW: <DESIGN_VIEW>
PTD ENGINEER: <PTD_ENGINEER>
DRAWING NO.: HSC 13052
REV: B
SIZE: D
SCALE: <SCALE>
SHEET 6 OF 23

DDR3 CLOCKING

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



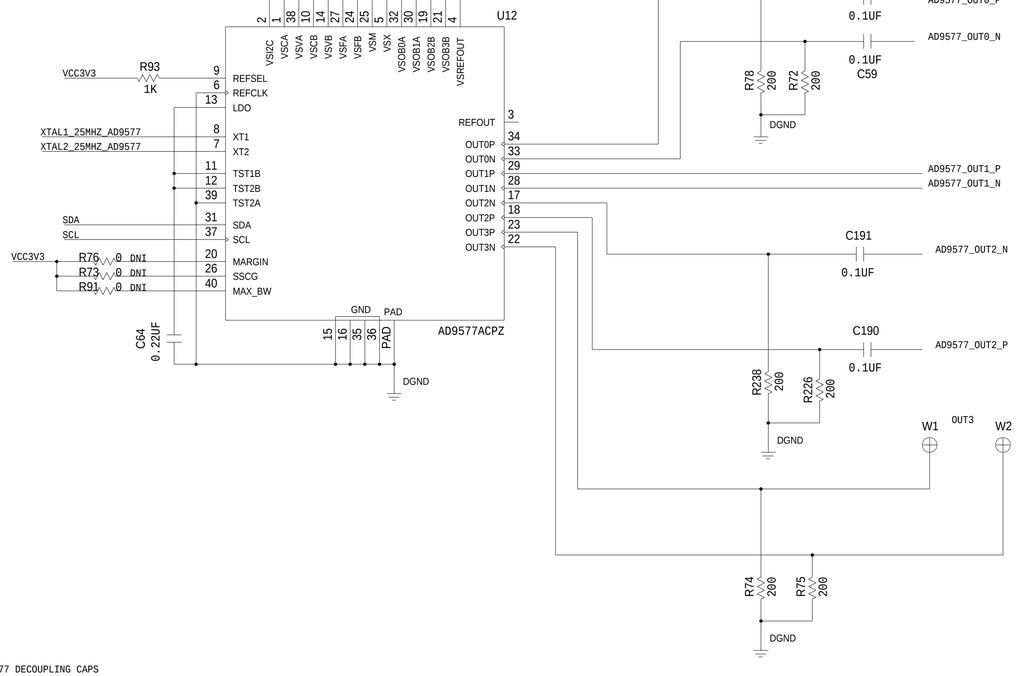
ENG:
- I2C ADDRESS: 0X80
- OUTPUT ASSIGNMENT:
  REFOUT - NOT USED
  OUT0 - DDR REF_CLK
  OUT1 - FPGA SYS_CLK
  OUT2 - DDR SYS_CLK
  OUT3 - NOT USED

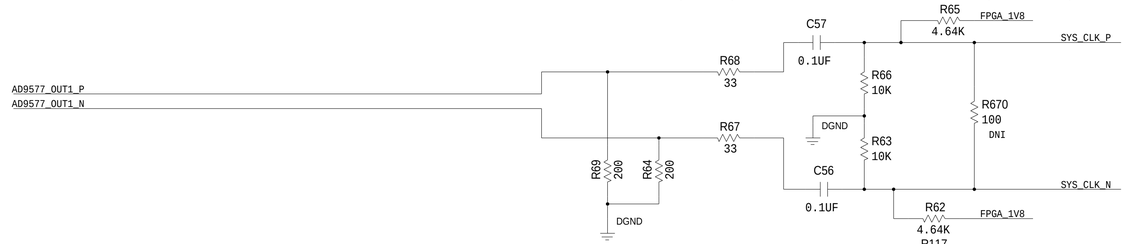


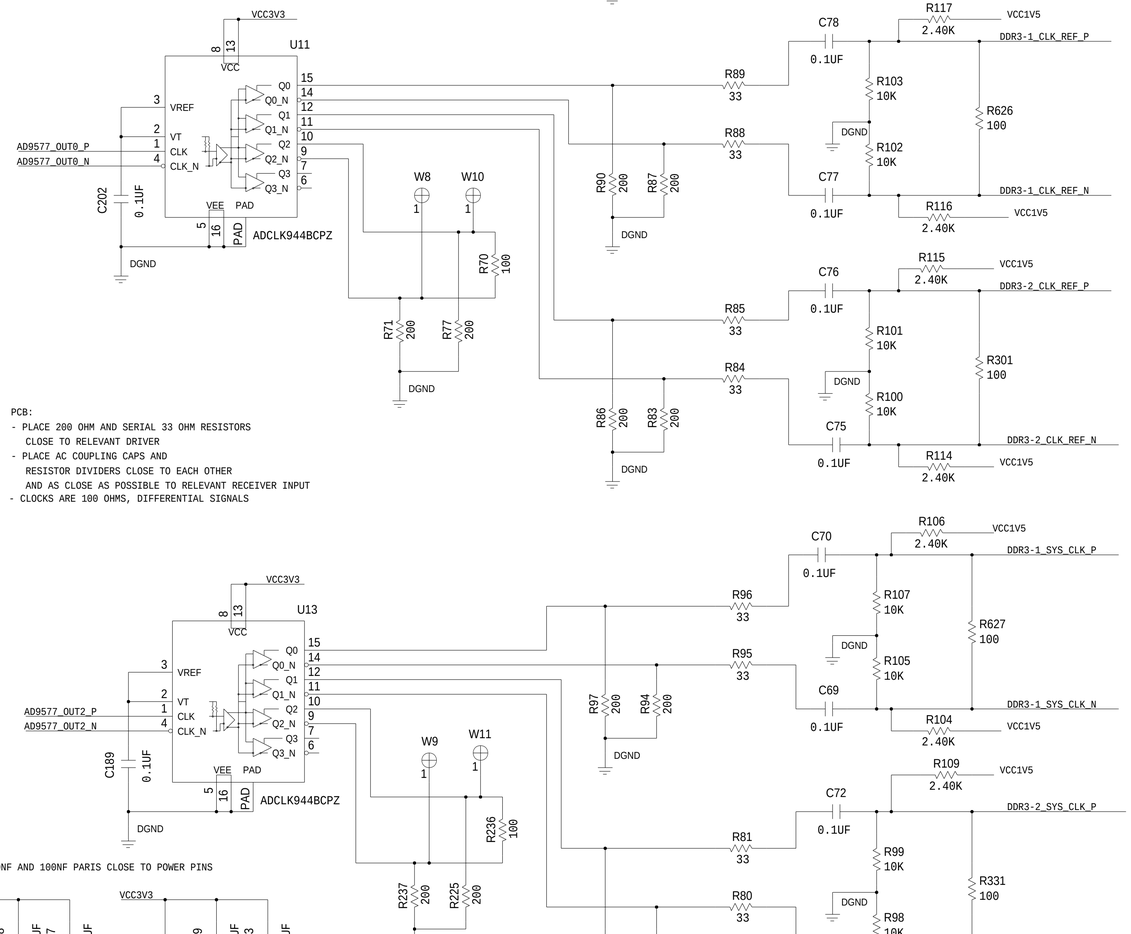
ENG:
- 0 OHM RES AND 0.1UF CAP FOR SENSITIVE / AGRESIVE POWER PINS
- 0 OHM RESISTOR TO BE REPLACED WITH FERRITE BEADS
  AFTER IDENTIFYING COUPLING ISSUES

PCB:
- PLEASE AS CLOSE AS POSSIBLE TO APPROPRIATE POWER PINS

PCB:
- OUTPUT CLOCKS ARE 100 OHMS, DIFFERENTIAL SIGNALS
- PLACE RESISTORS AND AC COUPLING CAPS
  AS CLOSE AS POSSIBLE TO THE DRIVER

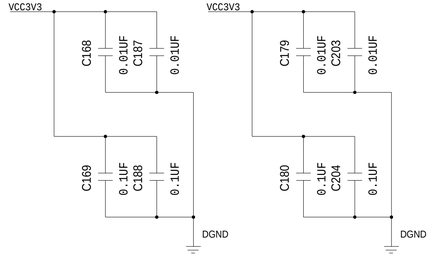




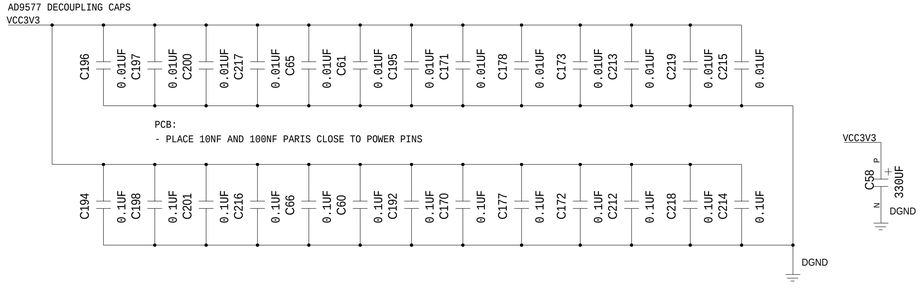


PCB:
- PLACE 200 OHM AND SERIAL 33 OHM RESISTORS
  CLOSE TO RELEVANT DRIVER
- PLACE AC COUPLING CAPS AND
  RESISTOR DIVIDERS CLOSE TO EACH OTHER
  AND AS CLOSE AS POSSIBLE TO RELEVANT RECEIVER INPUT
- CLOCKS ARE 100 OHMS, DIFFERENTIAL SIGNALS

PCB:
- PLACE 10NF AND 100NF PARIS CLOSE TO POWER PINS



AD9577 DECOUPLING CAPS



PCB:
- PLACE 10NF AND 100NF PARIS CLOSE TO POWER PINS

ANALOG DEVICES	SCHEMATIC		
	ADS7-V2 BOARD <PRODUCT> <PRODUCT_1>		
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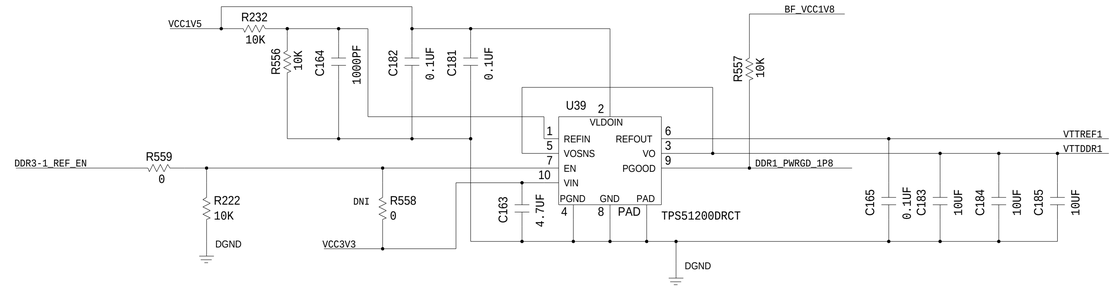
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 7 OF 23

DDR3 REFERENCE VOLTAGES

DDR-1 AND DDR-2 VTTREF - 0.75V
DDR-1 AND DDR-2 VTTDDR - 0.75V

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES

SCHEMATIC

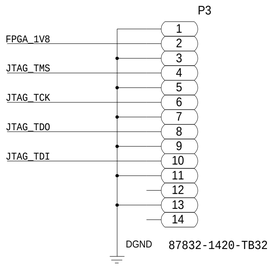
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 8 OF 23
<PTD_ENGINEER>	D / <SCALE>	

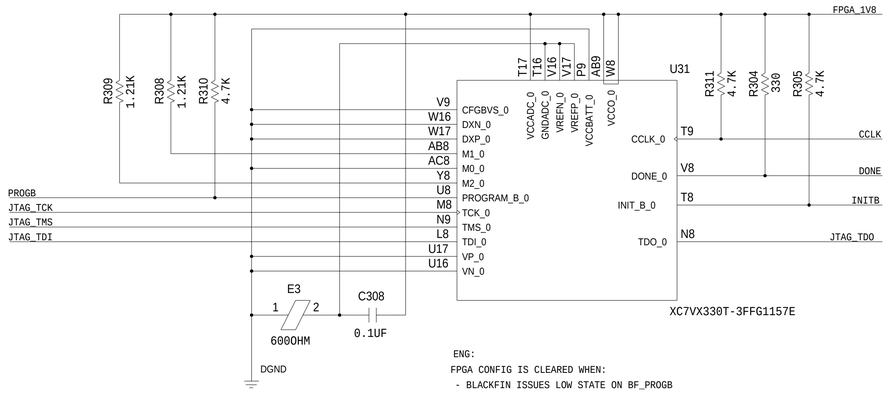
FPGA CONFIGURATION AND MISC BANKS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

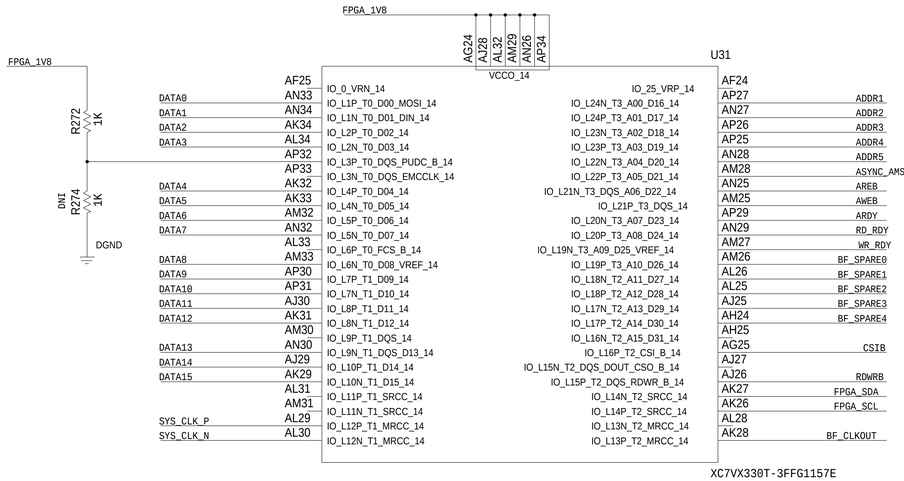
JTAG CONNECTOR



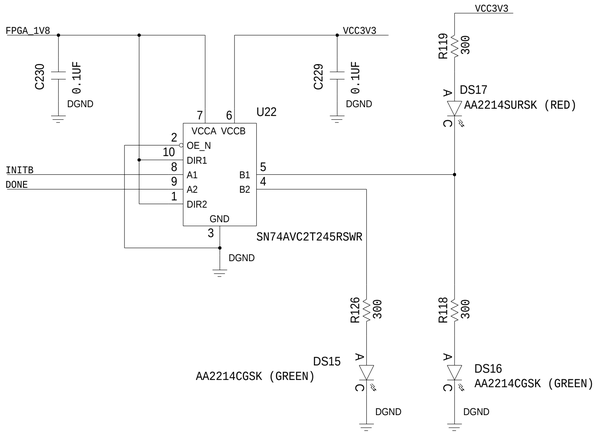
PCB:
- SILKSCREEN: 'FPGA JTAG'



ENG:
FPGA CONFIG IS CLEARED WHEN:
- BLACKFIN ISSUES LOW STATE ON BF_PROGB

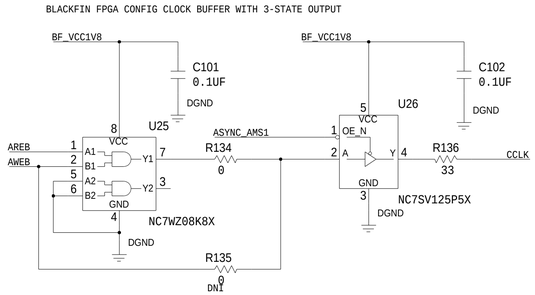


FPGA CONFIG SIGNALS LEVEL TRANSLATION



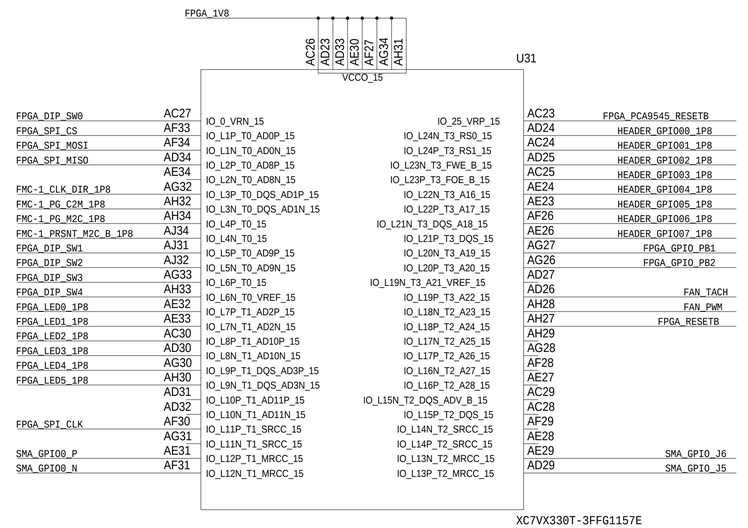
PCB:
- PLACE RED AND GREEN DS24 AND DS25 LED NEXT TO EACH OTHER
- DS24, DS25 SILKSCREEN: 'FPGA INITB'
- DS 23 SILKSCREEN: 'FPGA DONE'

BLACKFIN FPGA CONFIG CLOCK BUFFER WITH 3-STATE OUTPUT



FPGA RESET GENERATION
PCB:
- PLACE CLOSE TO BF527
- SILKSCREEN: 'FPGA RESETB'

ENG:
FPGA LOGIC IS RESET WHEN:
- FPGA RESET BUTTON IS PRESSED
- BLACKFIN ISSUES LOW
  STATE ON BF_FPGA_RESETB



ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
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DESIGN VIEW: <DESIGN_VIEW>
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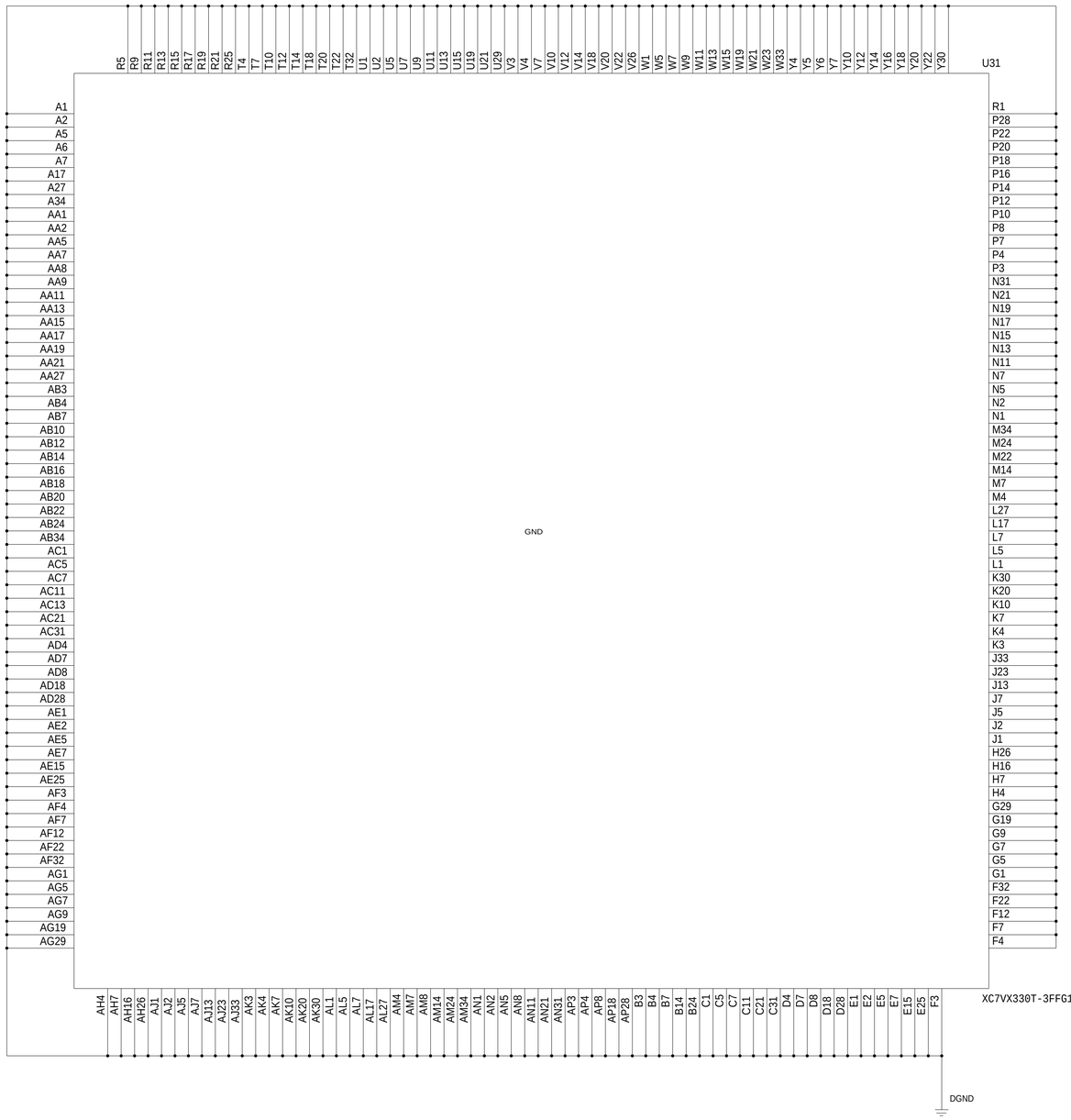
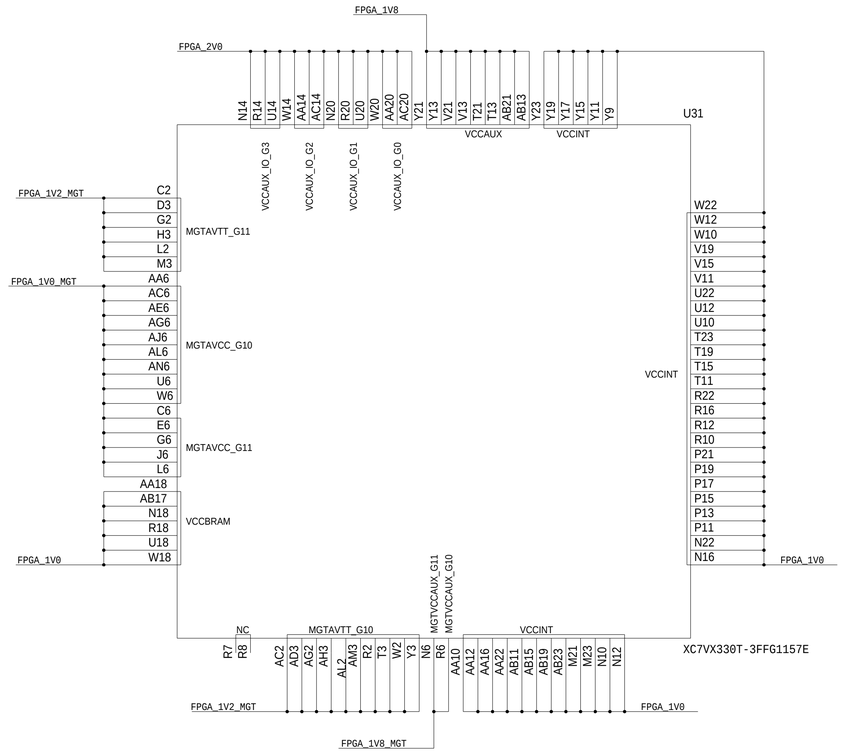
DRAWING NO.: HSC 13052
REV: B
SIZE: D
SCALE: <SCALE>
SHEET 9 OF 23

FPGA POWER AND GROUND

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
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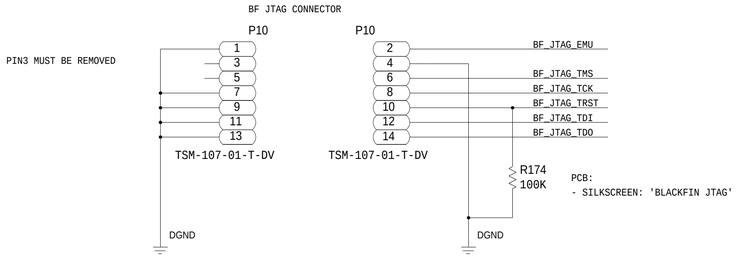
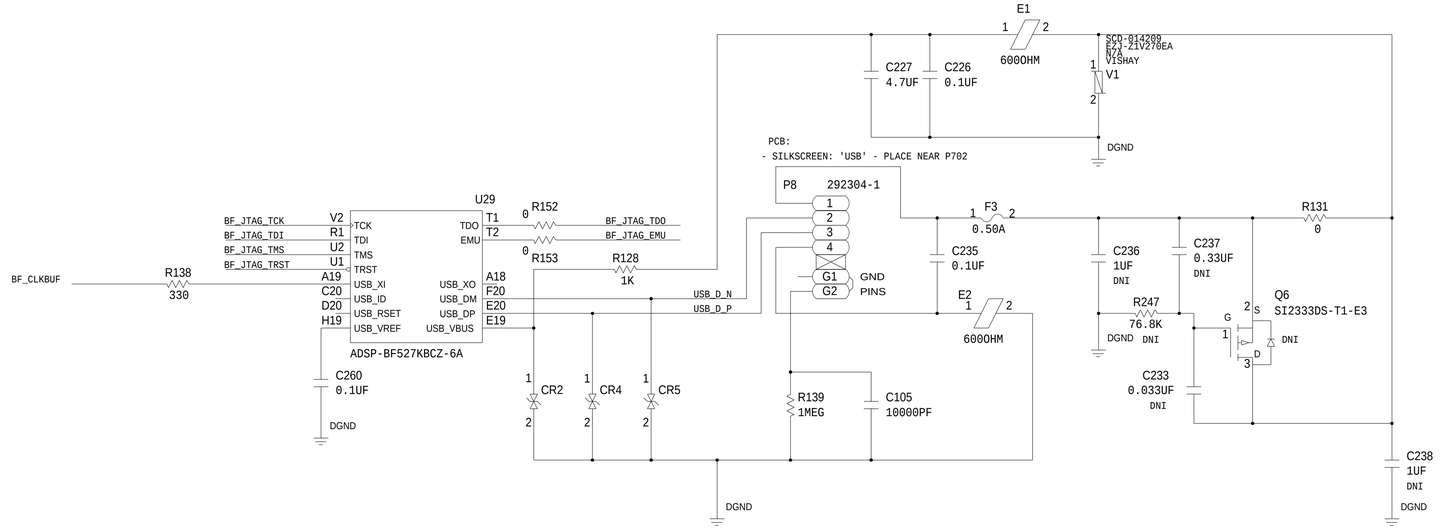
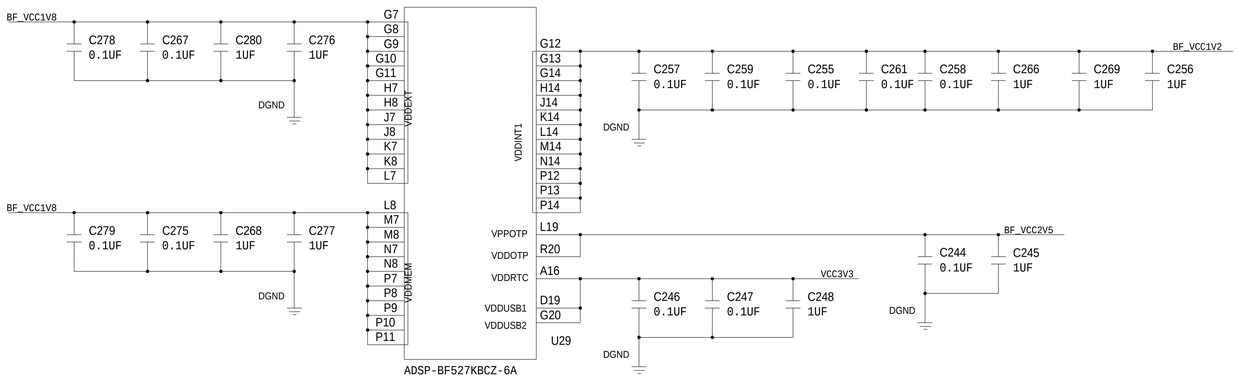
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13052	REV B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 10 OF 23

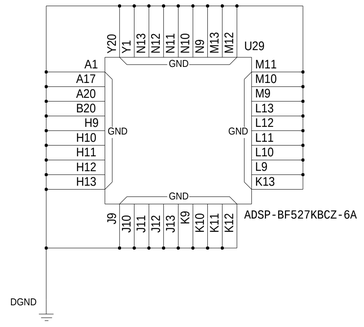
BLACKFIN

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED









ANALOG DEVICES	SCHEMATIC	
	ADS7-V2 BOARD <PRODUCT> <PRODUCT_1>	
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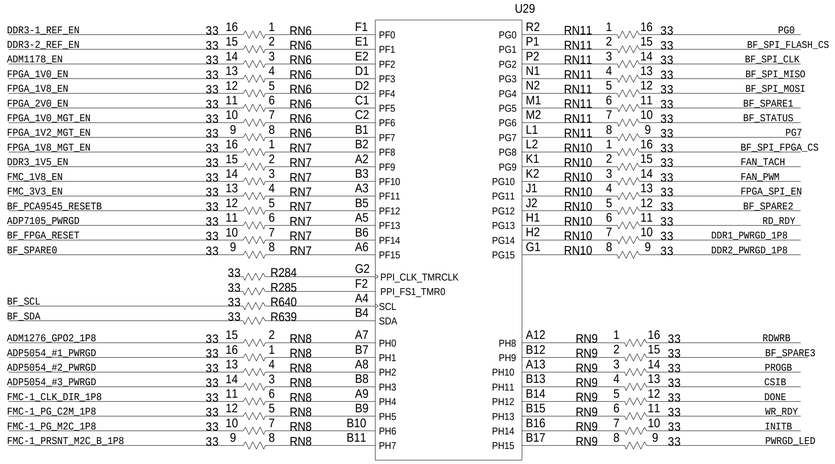
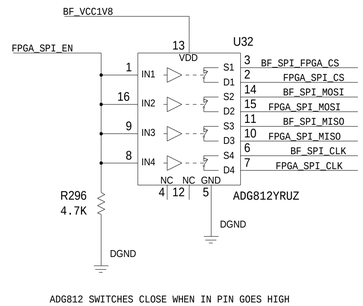
	PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE> SHEET 11 OF 23

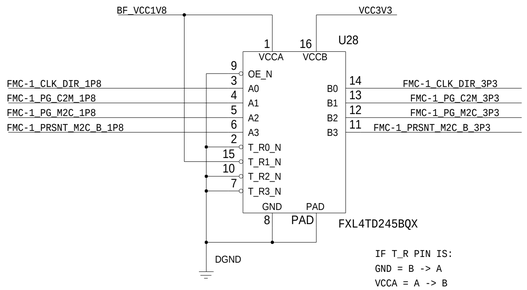
BLACKFIN IO

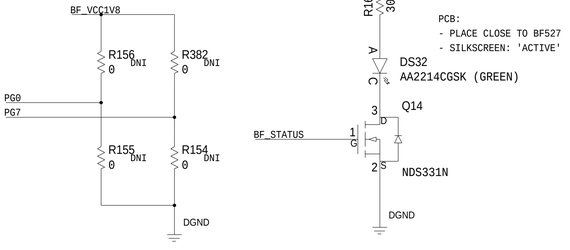
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





ADG812 SWITCHES CLOSE WHEN IN PIN GOES HIGH





ANALOG DEVICES

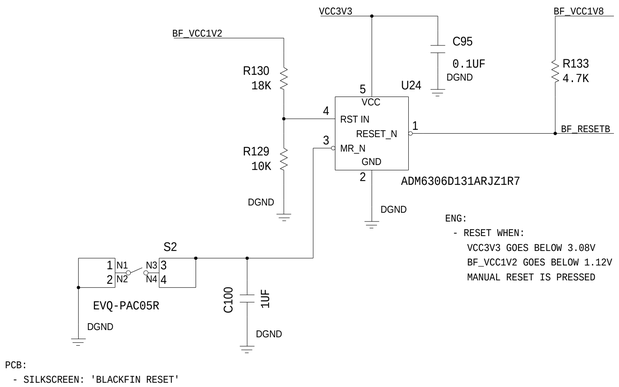
SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW <DESIGN_VIEW>
DRAWING NO. HSC 13052
REV B
PTD ENGINEER <PTD_ENGINEER>
SIZE D
SCALE <SCALE>
SHEET 12 OF 23

BLACKFIN MEMORIES AND RESET

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



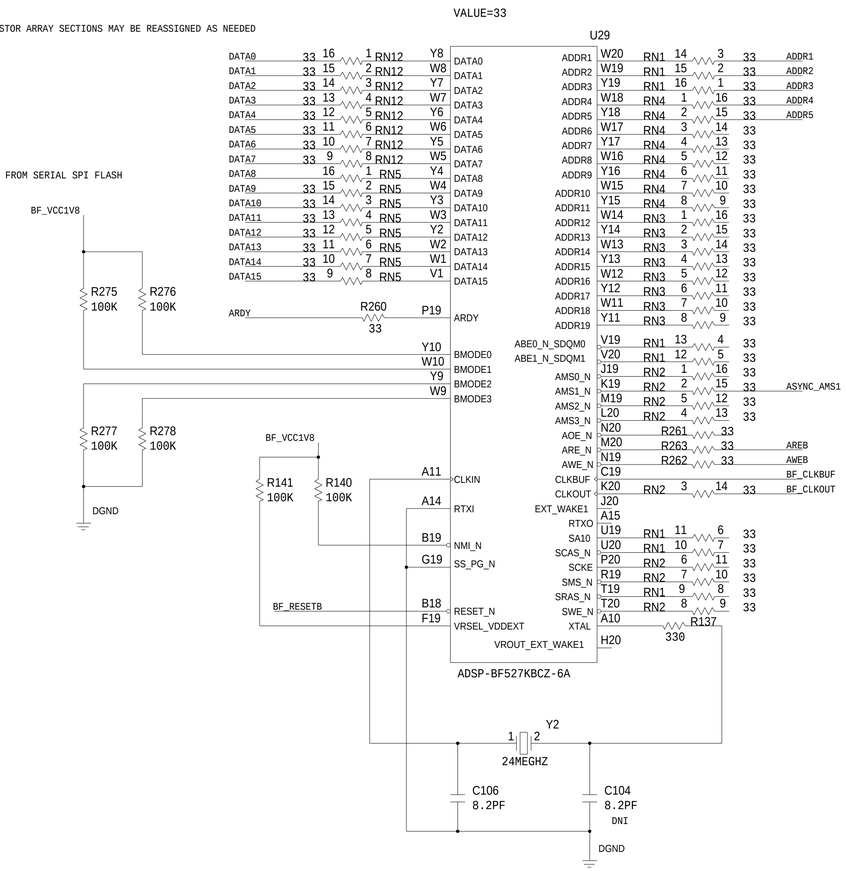
ENG:
- RESET WHEN:
  VCC3V3 GOES BELOW 3.08V
  BF_VCC1V2 GOES BELOW 1.12V
  MANUAL RESET IS PRESSED

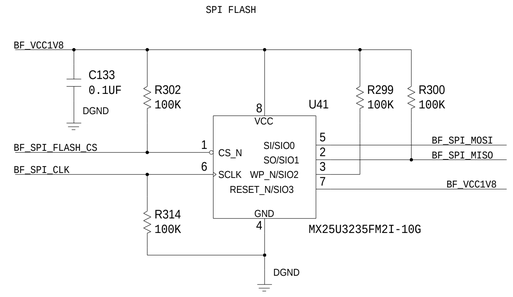
PCB:
- SILKSCREEN: 'BLACKFIN RESET'

PCB:
- RESISTOR ARRAY SECTIONS MAY BE REASSIGNED AS NEEDED

ENG:
- BOOT FROM SERIAL SPI FLASH

VALUE=33





ANALOG DEVICES

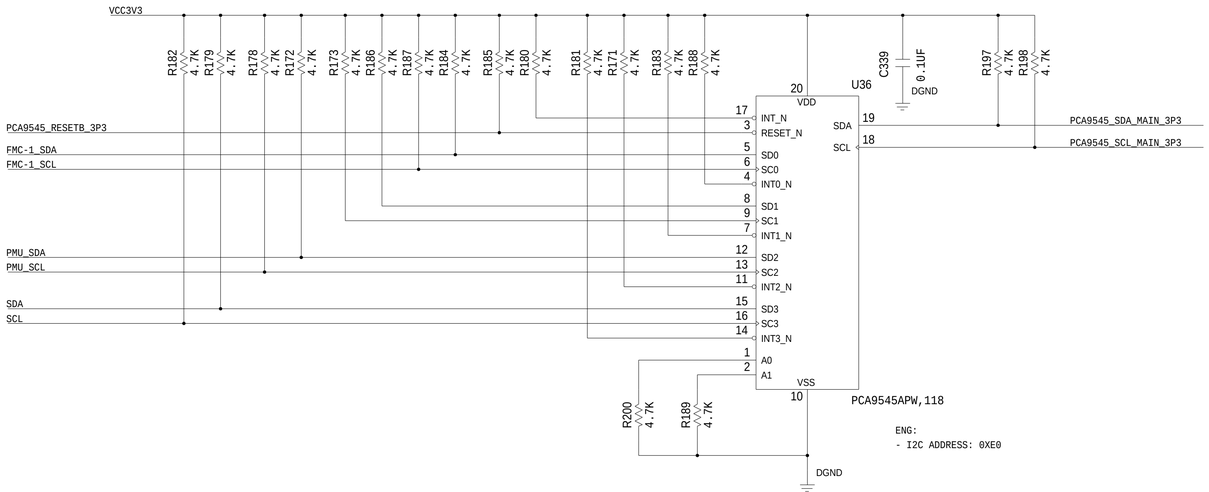
SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

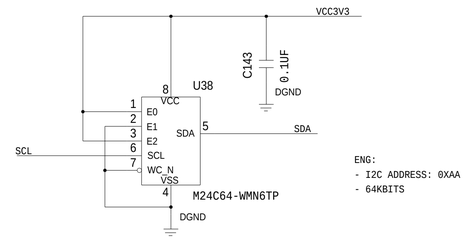
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 13 OF 23
<PTD_ENGINEER>	D / <SCALE>	

I2C MUX

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



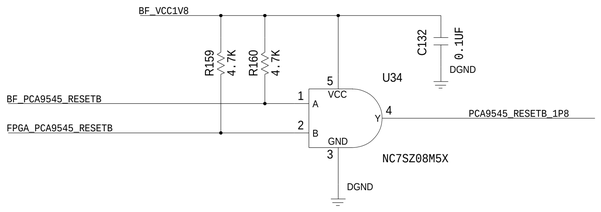
I2C EEPROM

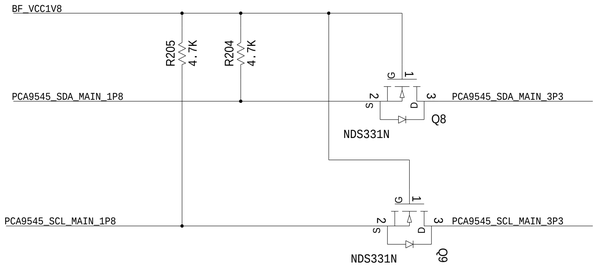


PMU I2C HEADER

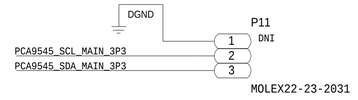
PCB
- SILKSCREEN: 'PMU I2C' - PLACE ABOVE THE CONNECTOR

PCA9545 RESET GENERATION





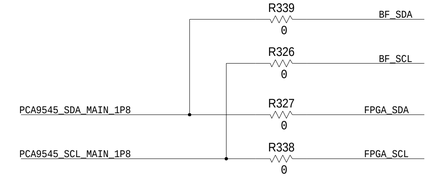
I2C HEADER



PCB
- SILKSCREEN: 'I2C' - PLACE ABOVE THE CONNECTOR

I2C MAP:

DEVICE	ADDRESS (8-BIT FORMAT -> I2C ADDRESS BYTE + R/W BIT)			
PCA9545APW	0XE0			
	BUS 3	BUS 2	BUS 1	BUS0
ADM1276		0X40		
ADM1178		0XE4		
ADM1293		0X22,0X24,0X26 0X82,0X84,0X86 0X88,0X8A,0X8C		
AD9577	0X80			
DDR3 MEM TEMP SENSOR	0X34, 0X36			
DDR3 SPD EEPROM	0XA4, 0XA6			
AD5258	0X30			
RTC-8564	0XA2			
ADS7-V1 EEPROM	0XAA			
FMC EEPROM				0XA0
FMC DEVICES				0X??



ANALOG DEVICES

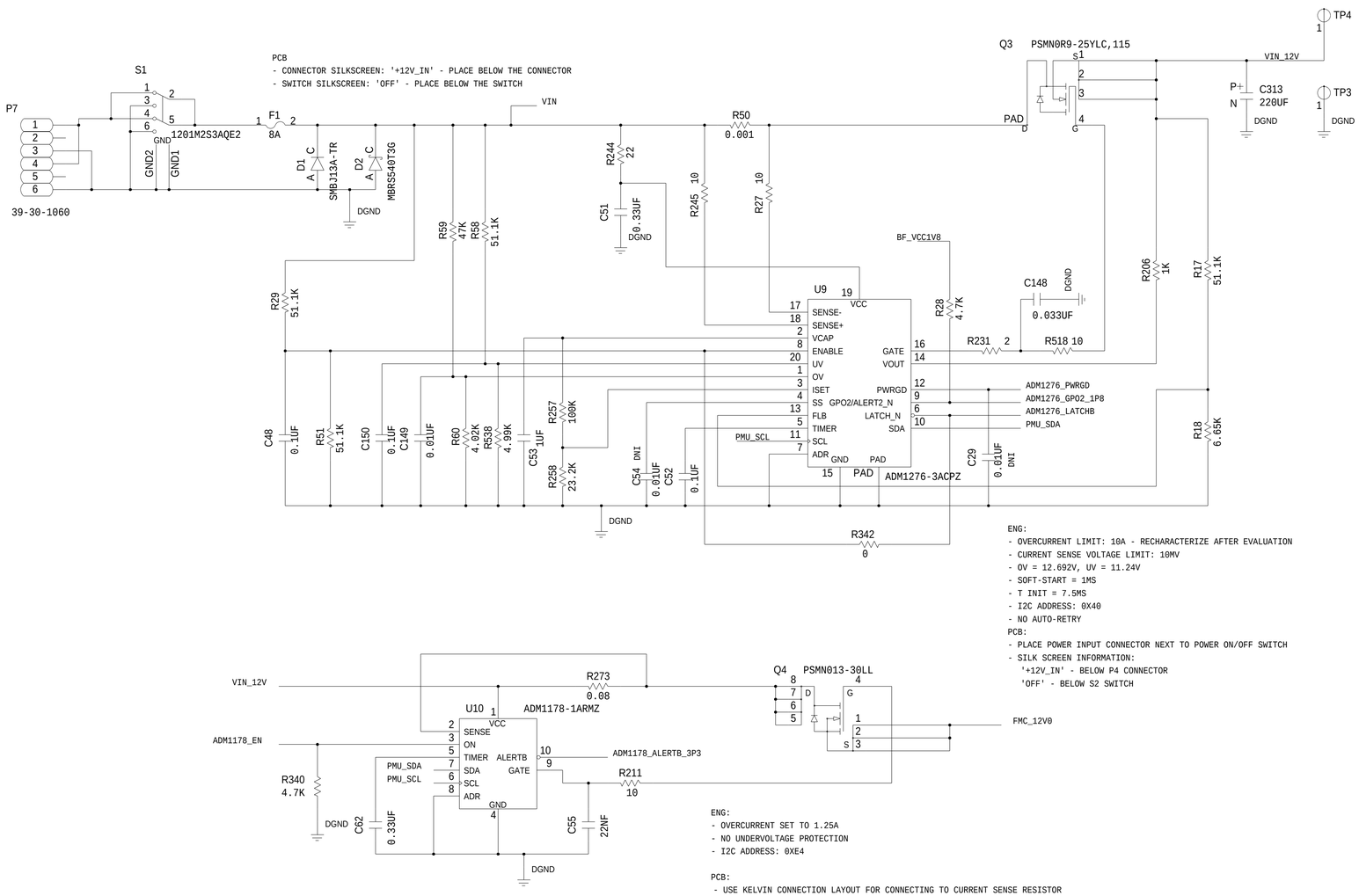
SCHEMATIC

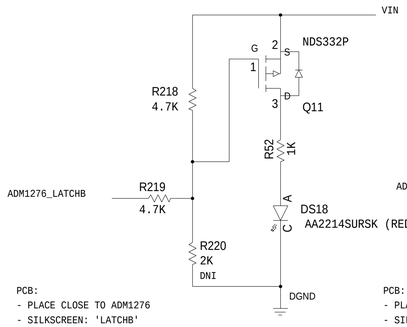
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

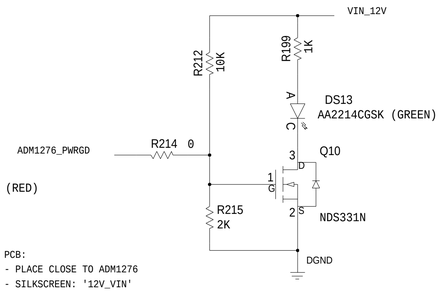
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13052	REV B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 14 OF 23

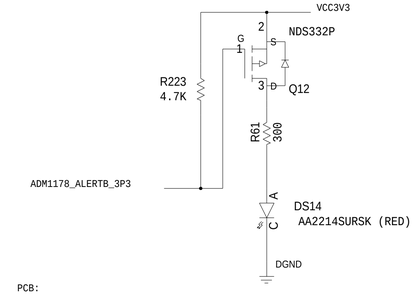
POWER INPUT

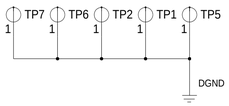
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED











ANALOG DEVICES	SCHEMATIC		
	ADS7-V2 BOARD <PRODUCT> <PRODUCT_1>		
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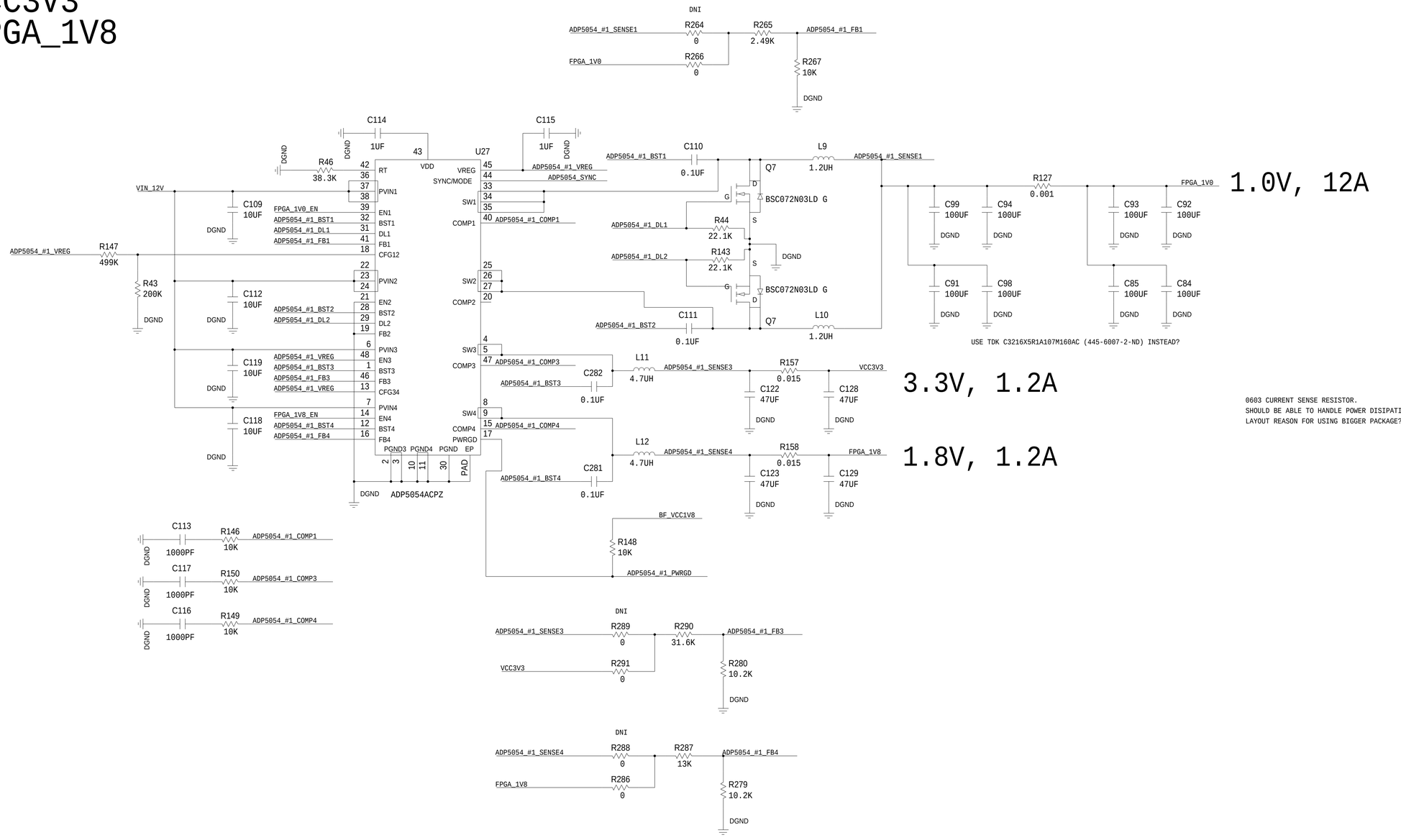
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 15 OF 23	

POWER ADP5054#1

FPGA_1V0
VCC3V3
FPGA_1V8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES	SCHEMATIC		
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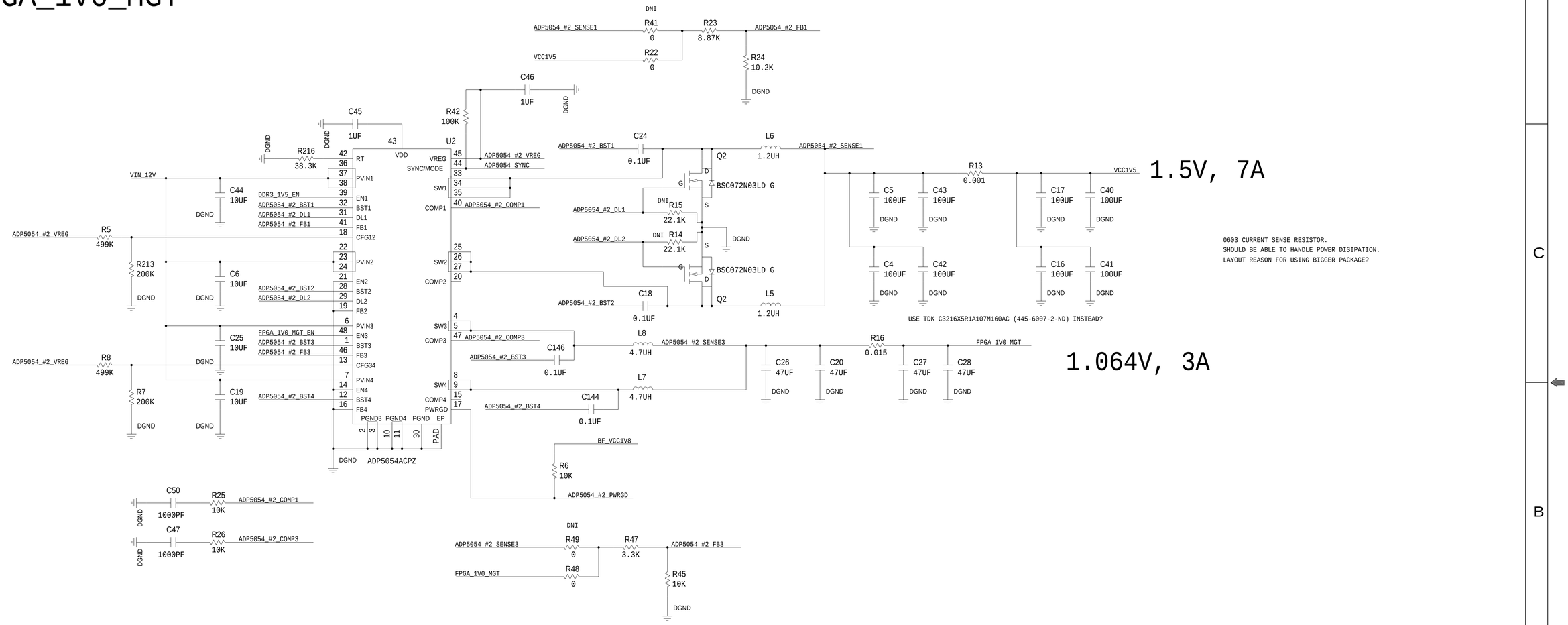
		SHEET 16 OF 23	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER ADP5054#2

VCC1V5

FPGA_1V0_MGT



ANALOG DEVICES	SCHEMATIC		
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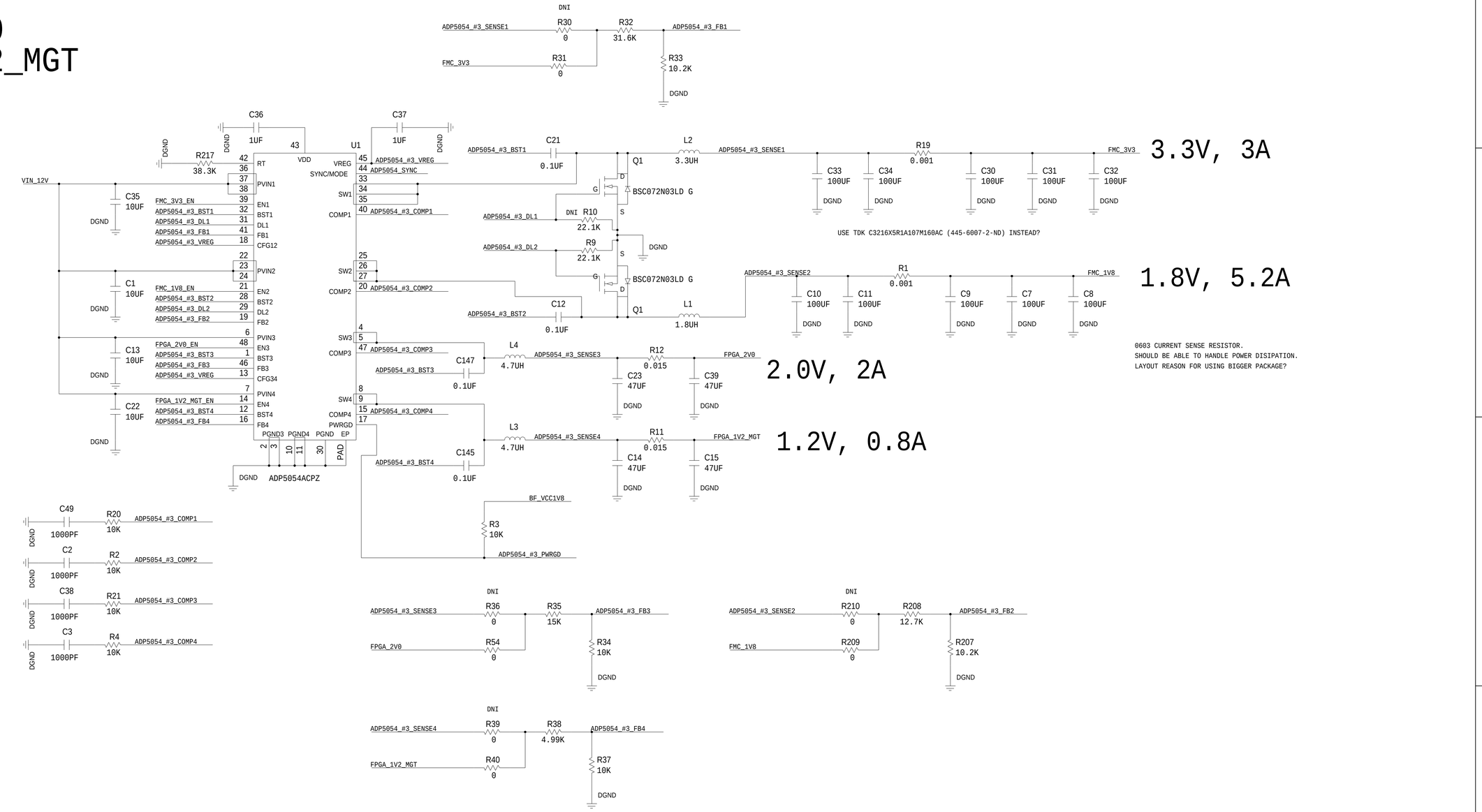
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 17 OF 23	

POWER ADP5054#3

FMC_3V3
FMC_1V8
FPGA_2V0
FPGA_1V2_MGT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES	SCHEMATIC		
	ADS7-V2 BOARD <PRODUCT> <PRODUCT_1>		
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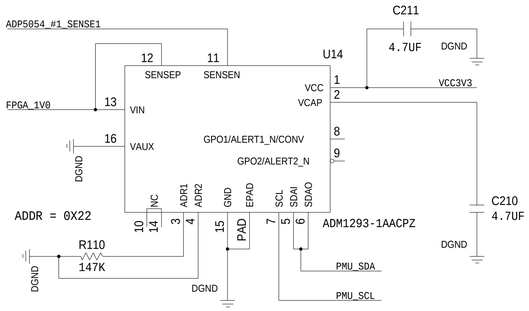
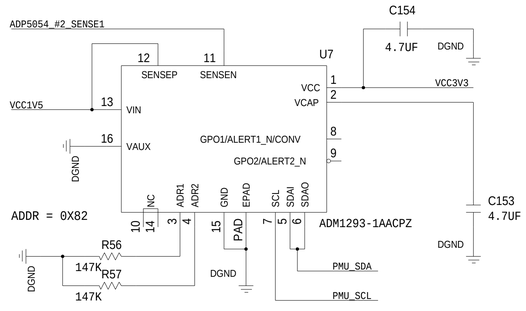
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 18 OF 23	

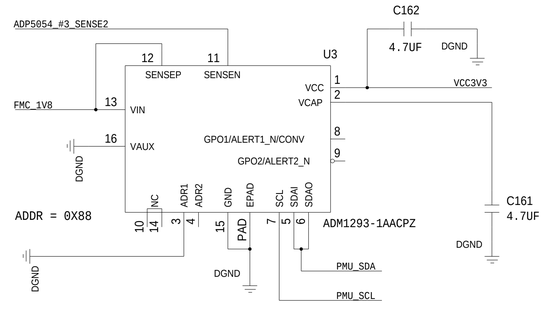
POWER MEASUREMENT

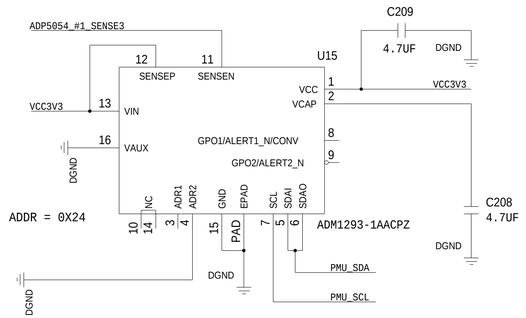
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

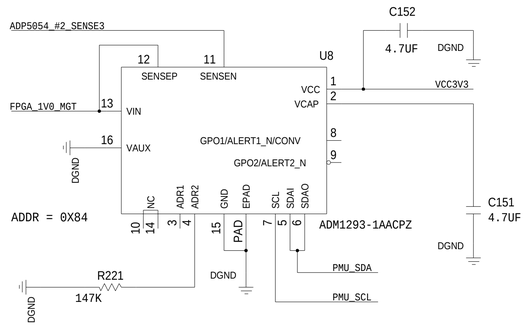
ADM1293 ADDRESSES:
00 = ADR PIN TIED TO GROUND
01 = ADR PIN TIED TO GROUND THROUGH 147K RESISTOR
10 = ADR PIN NOT CONNECTED
11 = ADR PIN TIED TO VCAP

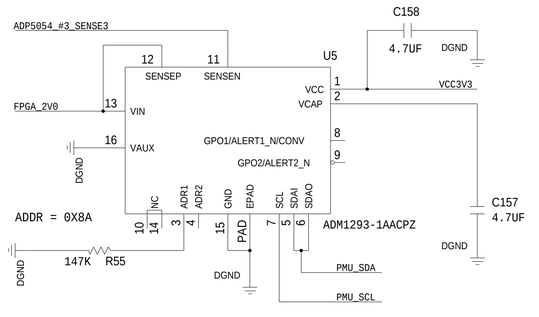


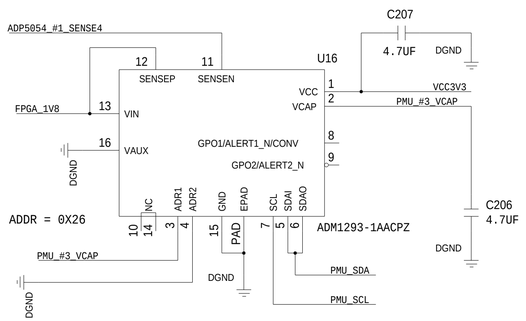


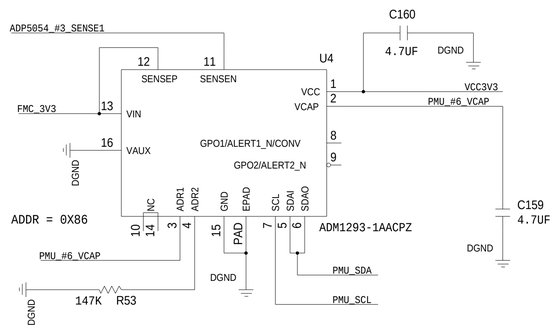


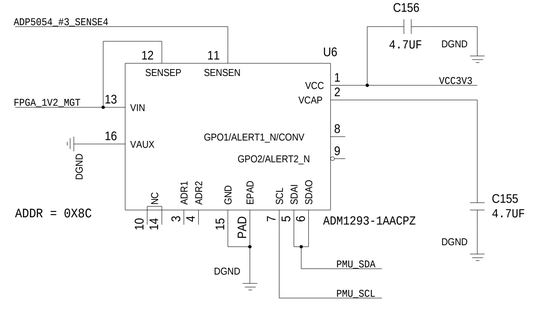












ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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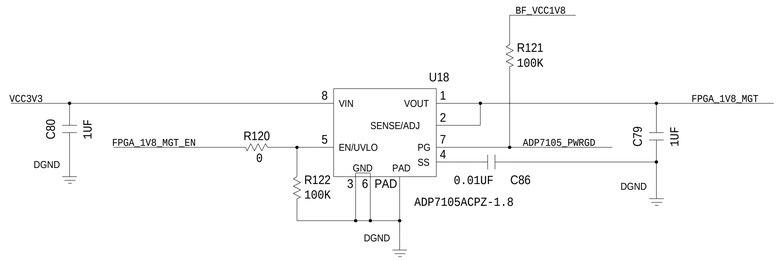
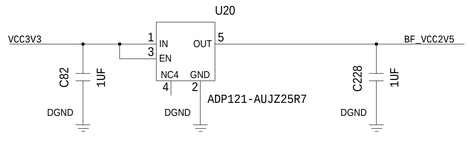
POWER - LINEAR

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



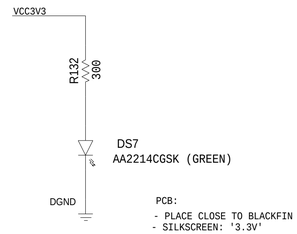
1.8V, 0.5A



2.5V, 0.15A, BLACKFIN

1.8V, 0.2A, BLACKFIN

1.2V, 0.5A, BLACKFIN



PCB:
- PLACE CLOSE TO BLACKFIN
- SILKSCREEN: '3.3V'

ANALOG DEVICES	SCHEMATIC	
	ADS7-V2 BOARD <PRODUCT> <PRODUCT_1>	
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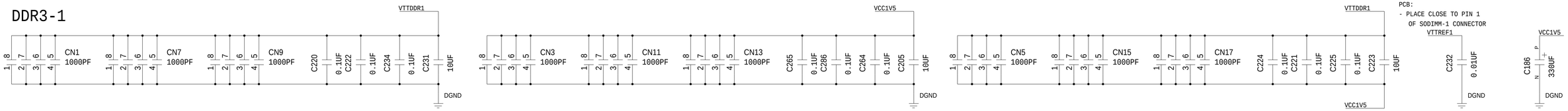
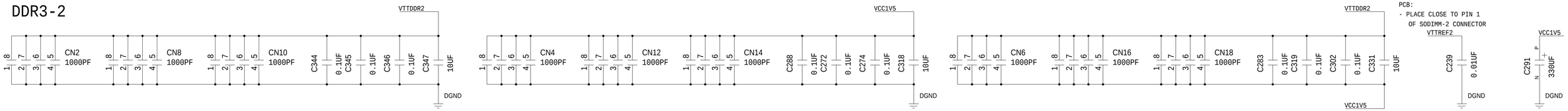
DECOUPLING CAPS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

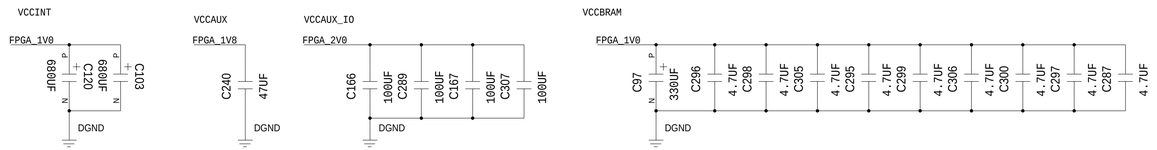
DDR3-1

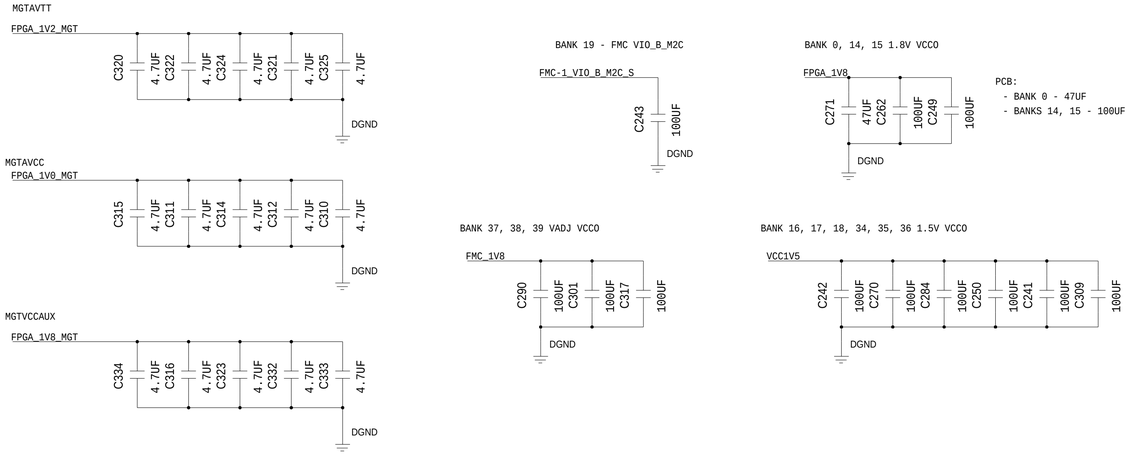


DDR3-2



FPGA





ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
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DESIGN VIEW	DRAWING NO.	REV
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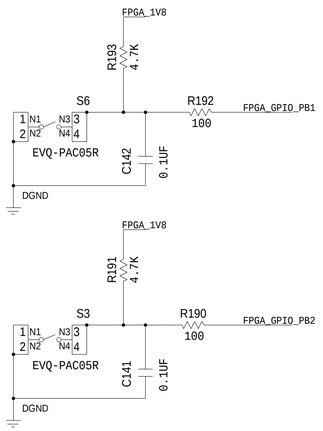
FAN CONTROL, FPGA GPIO, BUTTONS, RTC

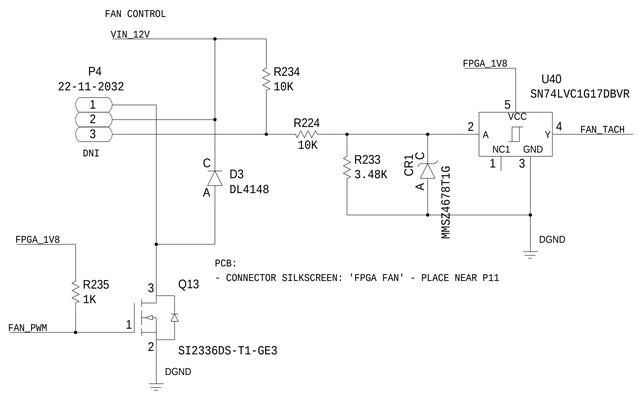
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FPGA PUSHBUTTONS



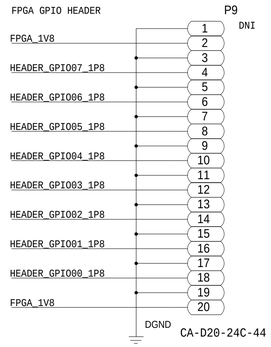
PCB:
- SILKSCREEN: 'PB1' 'PB2'

FAN CONTROL

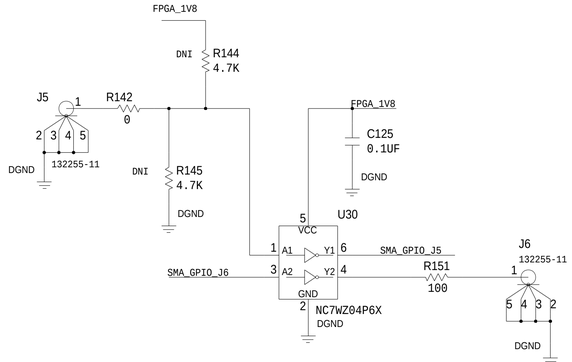


PCB:
- CONNECTOR SILKSCREEN: 'FPGA FAN' - PLACE NEAR P11

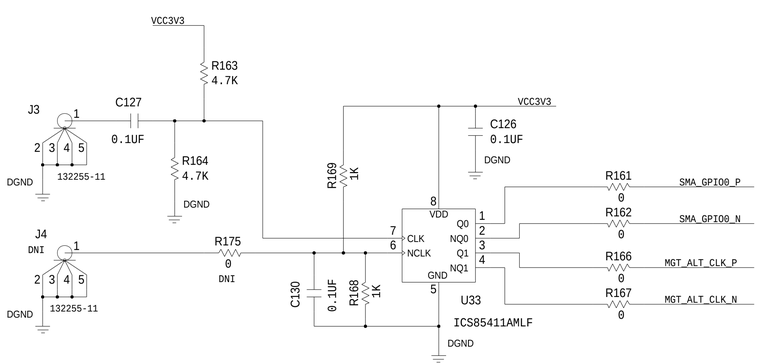
FPGA GPIO HEADER

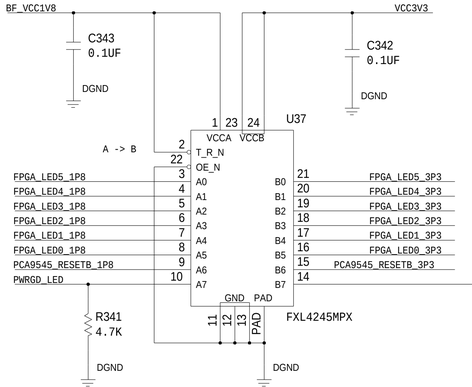


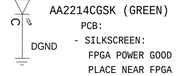
SMA GPIO
- J5 - TRIGGER INPUT
- J6 - READY OUTPUT



SMA GPIO CLOCK INPUTS

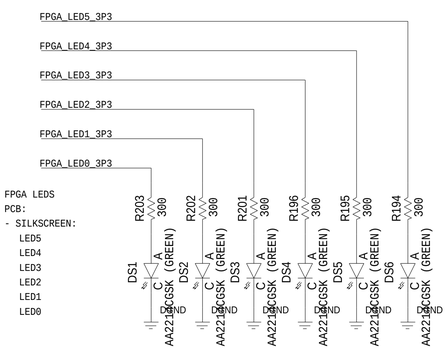




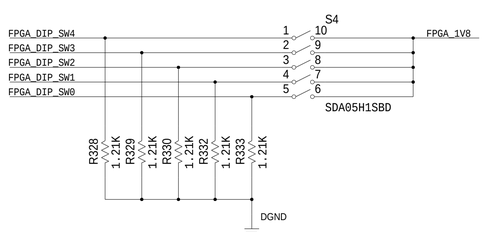


PCB:
- SILKSCREEN:
  - FPGA POWER GOOD
  - PLACE NEAR FPGA

FPGA LEDS
PCB:
- SILKSCREEN:
  - LED5
  - LED4
  - LED3
  - LED2
  - LED1
  - LED0



FPGA DIP SWITCHES



ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE: D	SCALE: <SCALE>
<PTD_ENGINEER>	SHEET 22 OF 23	

OTHER COMMENTS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

MECHANICAL COMPONENTS:

PCB BOARD STANDOFFS:

STANDOFFS:
- ETTINGER - 05.03.123 - SPACER, M3X12-NI
- FARNELL STOCK CODE: 1466772
- QTY: 6

SCREWS:
- DURATOOL - M36 PRA2MCS100- - SCREW, POZI PAN, S/S, A2, M3X6
- FARNELL STOCK CODE: 1420032
- QTY: 12

RUBBER BUMPER:
- KEYSTONE - 720 - RECESSED BUMPERS, RUBBER
- FARNELL STOCK CODE: 1651664
- QTY: 6

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW: <DESIGN_VIEW>

DRAWING NO.: HSC 13052

REV: B

PTD ENGINEER: <PTD_ENGINEER>

SIZE: D

SCALE: <SCALE>