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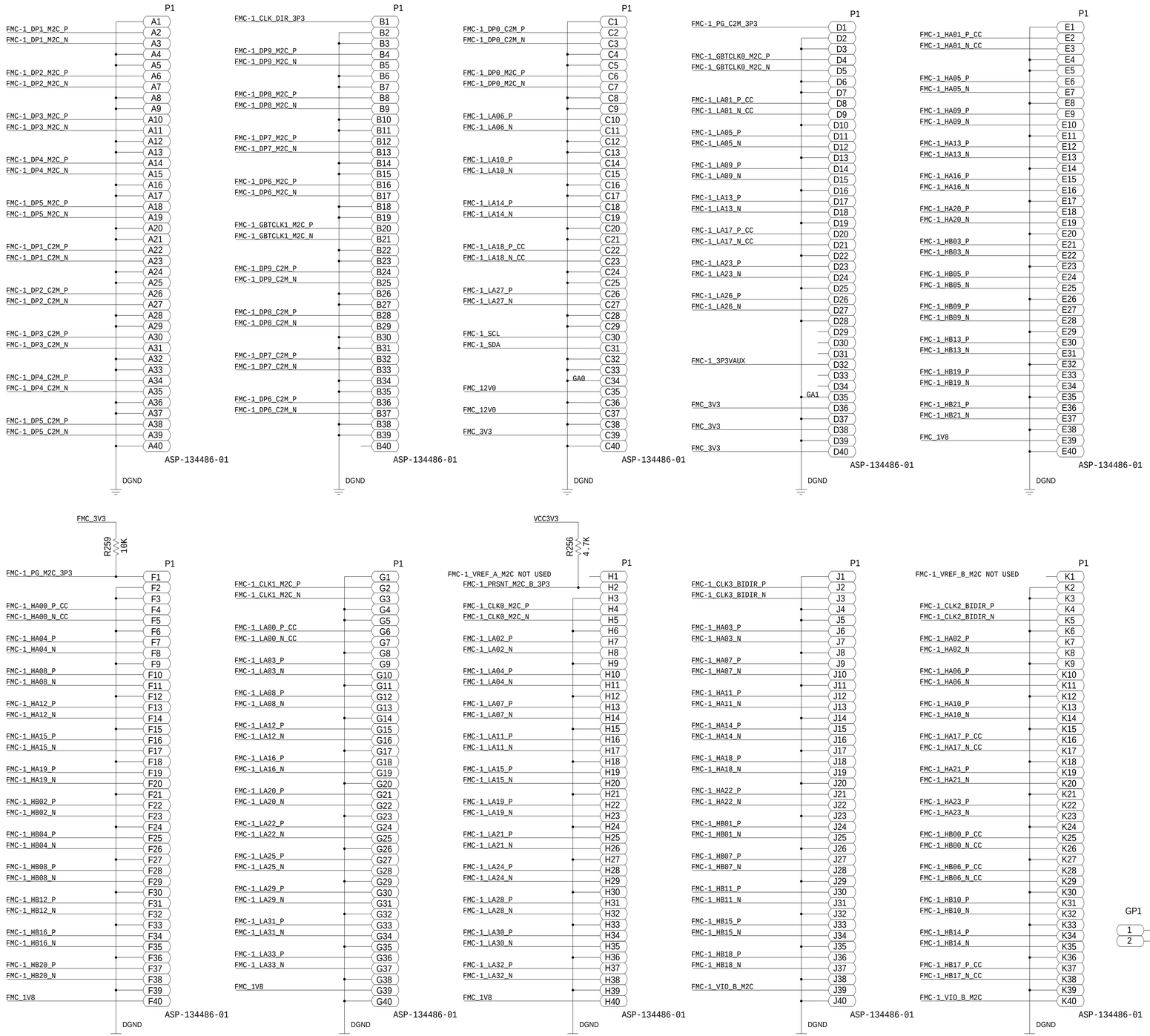
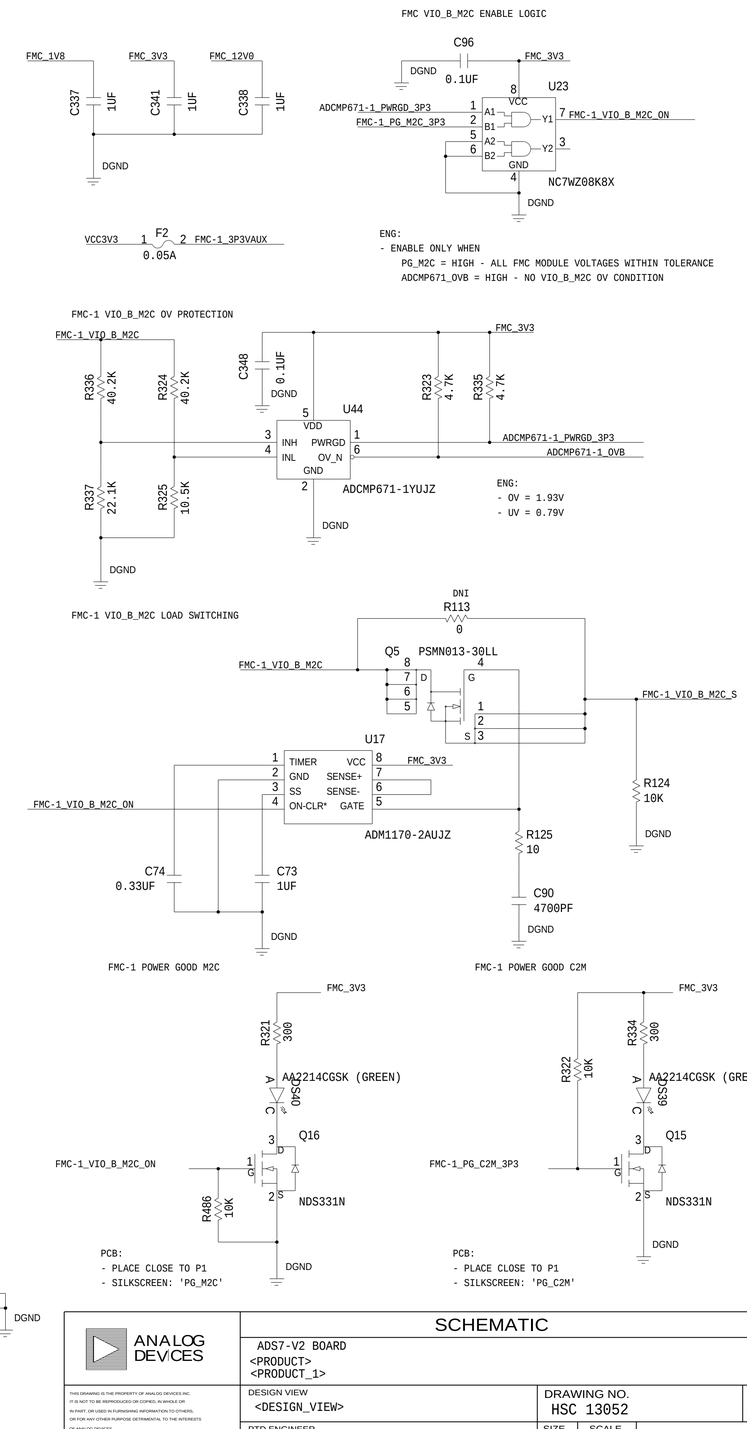
RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

FMC CONNECTOR

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





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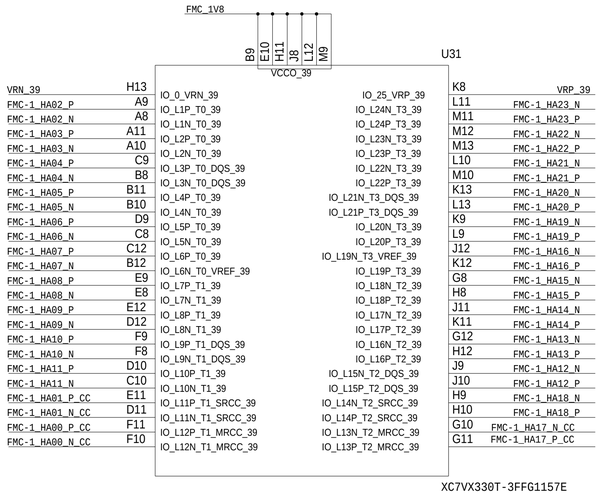
SCHEMATIC

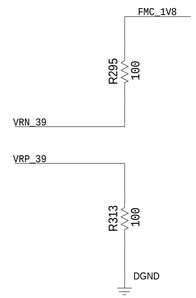
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

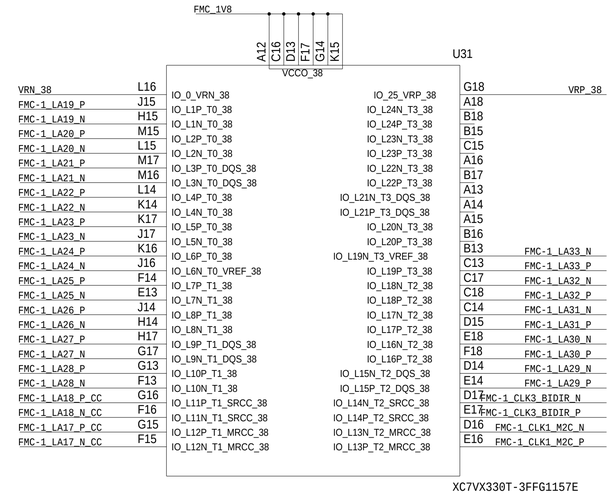
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 2 OF 23
<PTD_ENGINEER>	D / <SCALE>	

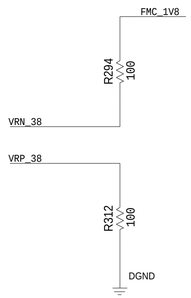
FMC BANKS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

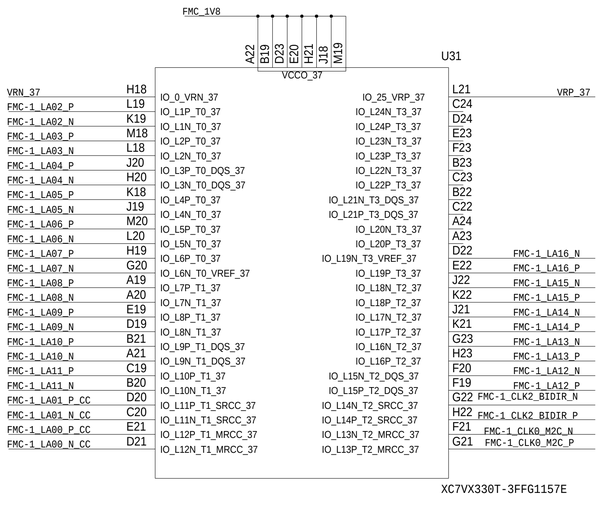


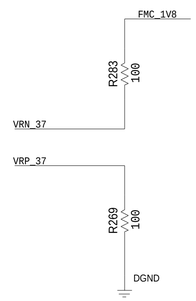


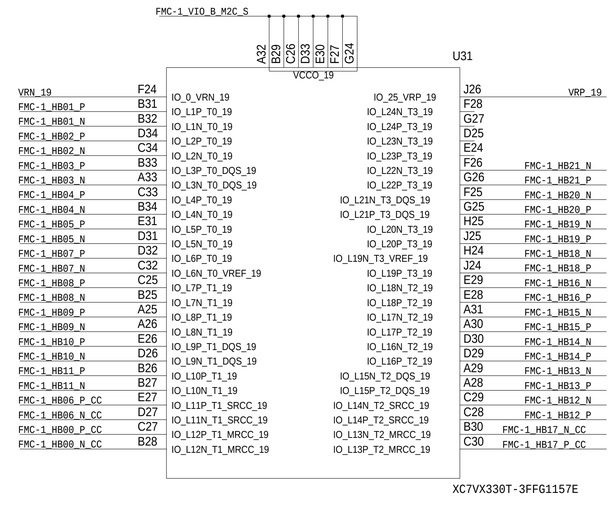


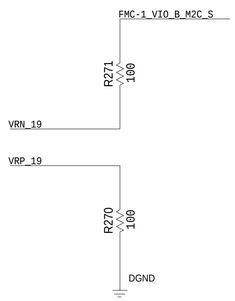


PCB:
- HA, HB AND LA BUS SIGNALS CAN BE MOVED WITHIN THE BANK, EXCEPT FOR SIGNALS GOING TO _MRCC AN_SRCC IOS
- DIFFERENTIAL PAIRS SHALL BE KEPT TOGETHER AND CONNECT TO APPROPRIATE P AND N PIN ON FPGA









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SCHEMATIC

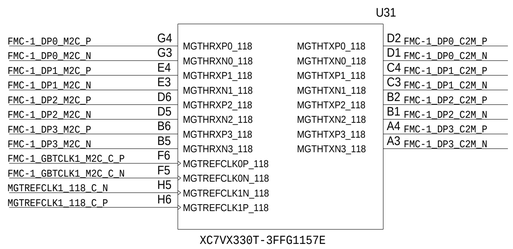
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

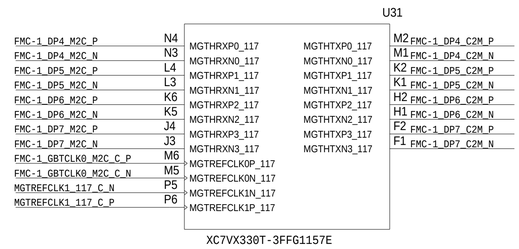
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE	SCALE
<PTD_ENGINEER>	D	<SCALE>

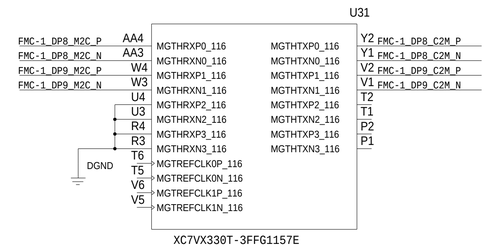
SHEET 3 OF 23

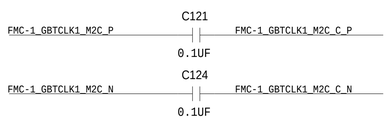
FMC MGT BANKS

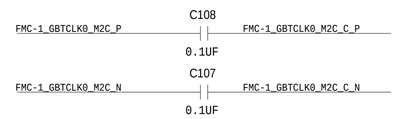
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

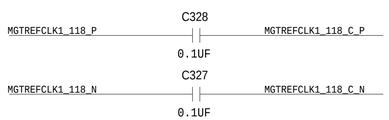


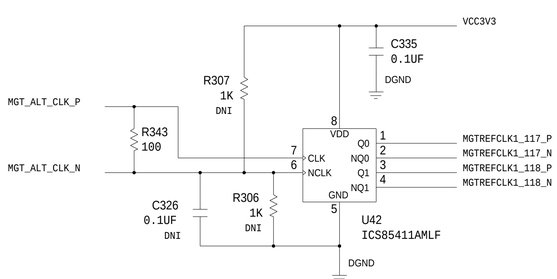


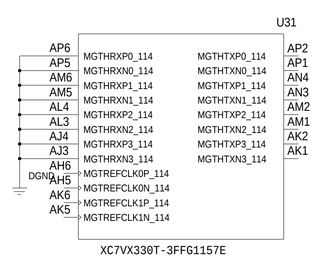


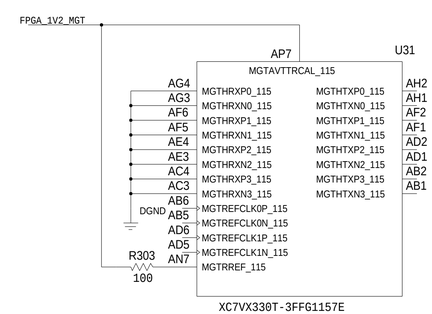












TRACE LENGTH FROM THE RESISTOR PINS TO THE FPGA PINS MGTRREF AND MGTAVTTRCAL MUST BE EQUAL IN LENGTH AND HAVE THE SAME GEOMETRY

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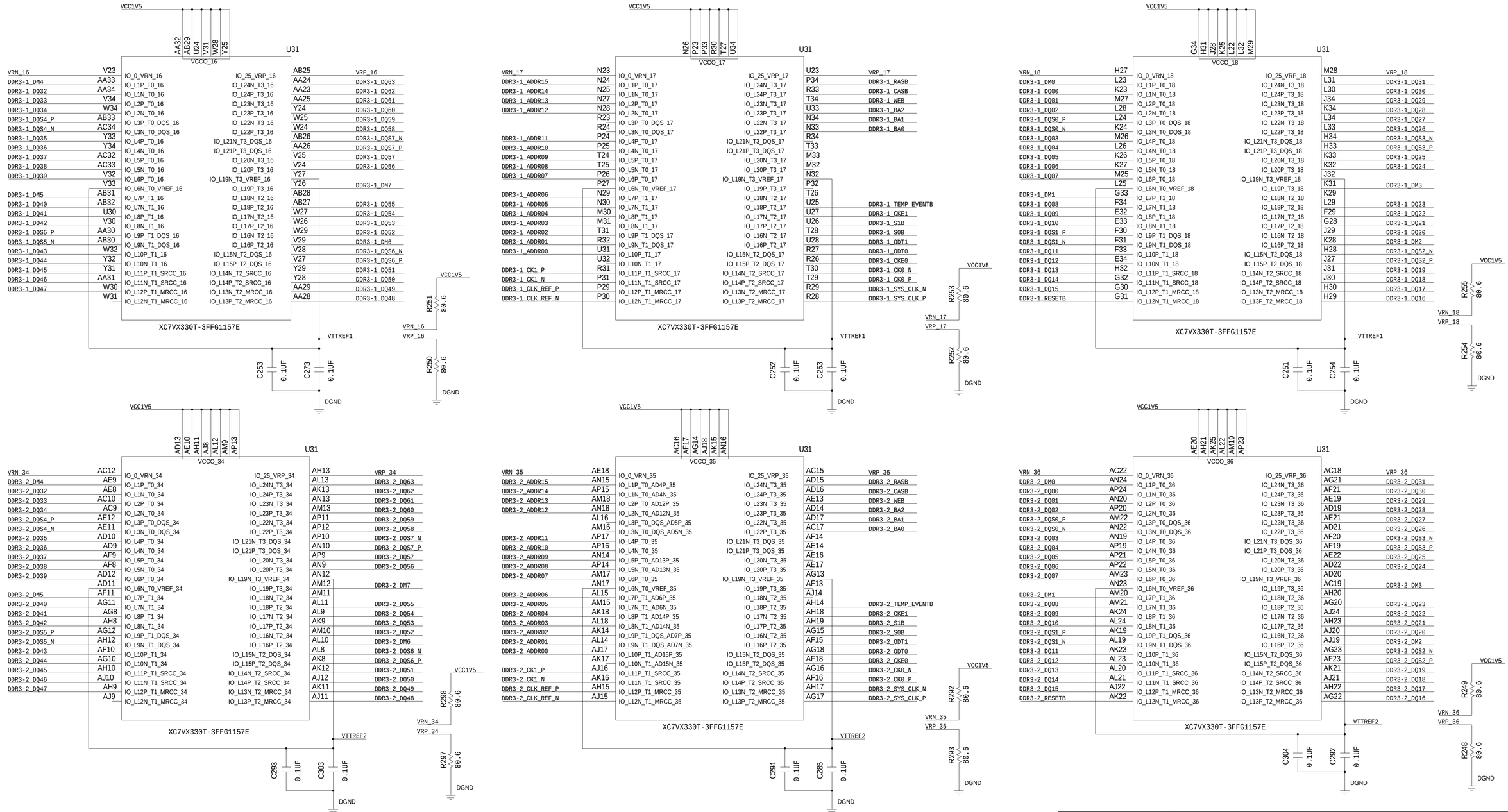
SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 4 OF 23
<PTD_ENGINEER>	D / <SCALE>	

DDR3-1 AND DDR3-2 BANKS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



PCB:
- ALL DQ AND DM NETS IN A BYTE GROUP MUST BE MATCHED TO THEIR ASSOCIATED DQS NETS
- IT IS RECOMMENDED THAT THE TRANSMISSION LINE OF A DQ/DM NET BE MATCHED TO ITS ASSOCIATED DQS NET WITHIN +-5 PS
- ALL ADDR, CMD, AND CONTROL SIGNALS MUST BE MATCHED TO THE CK CLOCK SIGNAL WITHIN +- 5 PS
- PLACE VTTREF DECOUPLING CAPS AS CLOSE AS POSSIBLE TO RELEVANT FPGA PINS
- VRN/VRP TRACES SHOULD BE MATCHED AND SHOULD BE AS SHORT AS POSSIBLE

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ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
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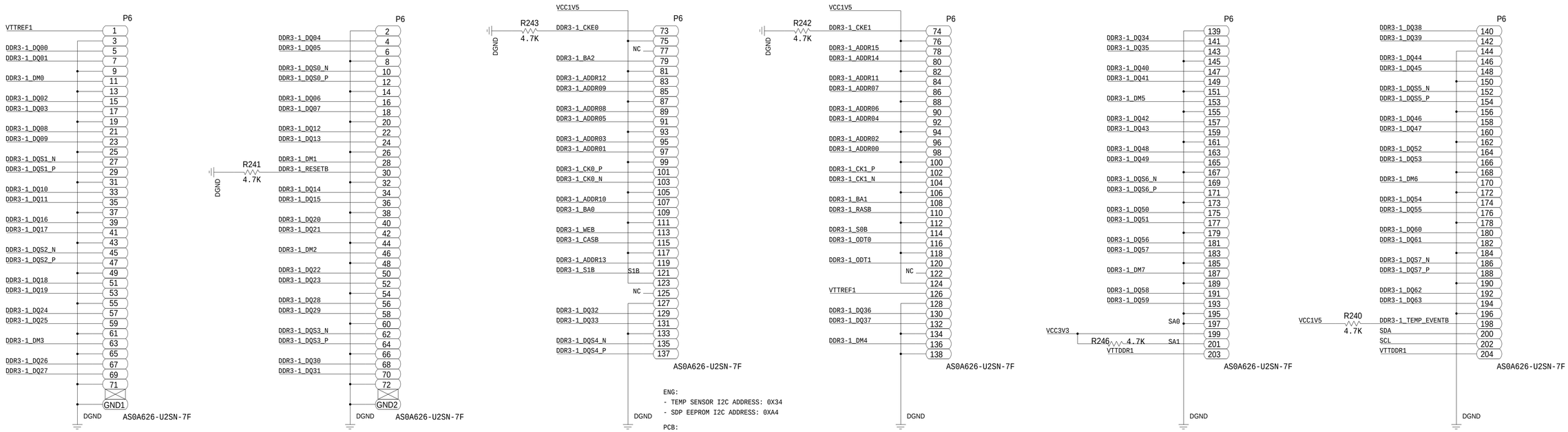
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE D / SCALE <SCALE>	SHEET 5 OF 23
<PTD_ENGINEER>		

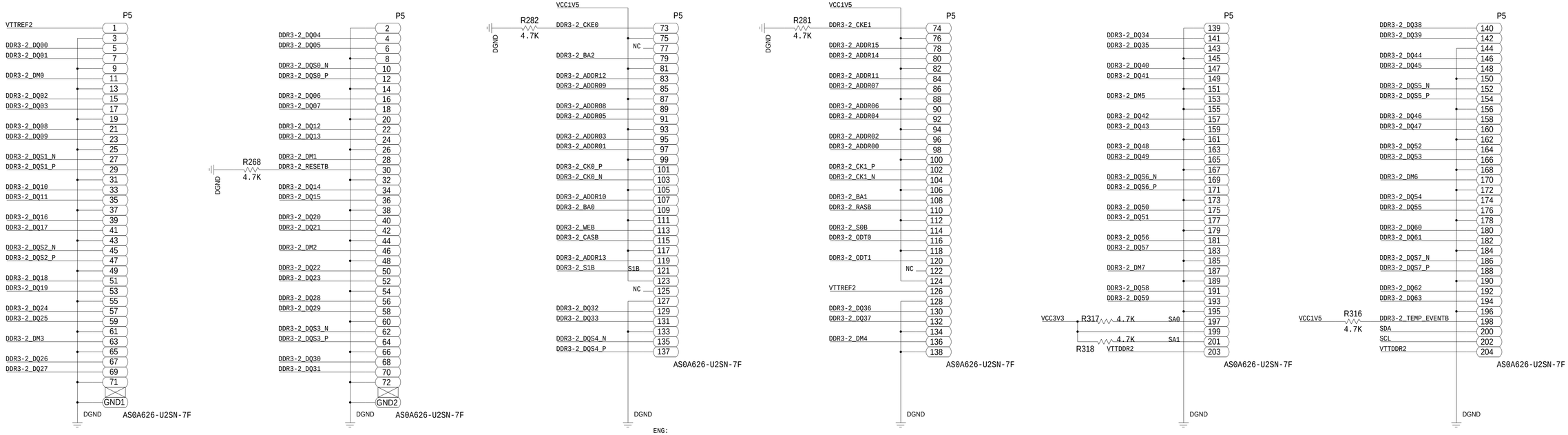
DDR3-1 AND DDR3-2 SODIMM

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ENG:
- TEMP SENSOR I2C ADDRESS: 0X34
- SDP EEPROM I2C ADDRESS: 0XA4

PCB:
- P6 SILKSCREEN: 'SODIMM-1' - PLACE ABOVE THE CONNECTOR



ENG:
- TEMP SENSOR I2C ADDRESS: 0X36
- SDP EEPROM I2C ADDRESS: 0XA6

PCB:
- P5 SILKSCREEN: 'SODIMM-2' - PLACE ABOVE THE CONNECTOR

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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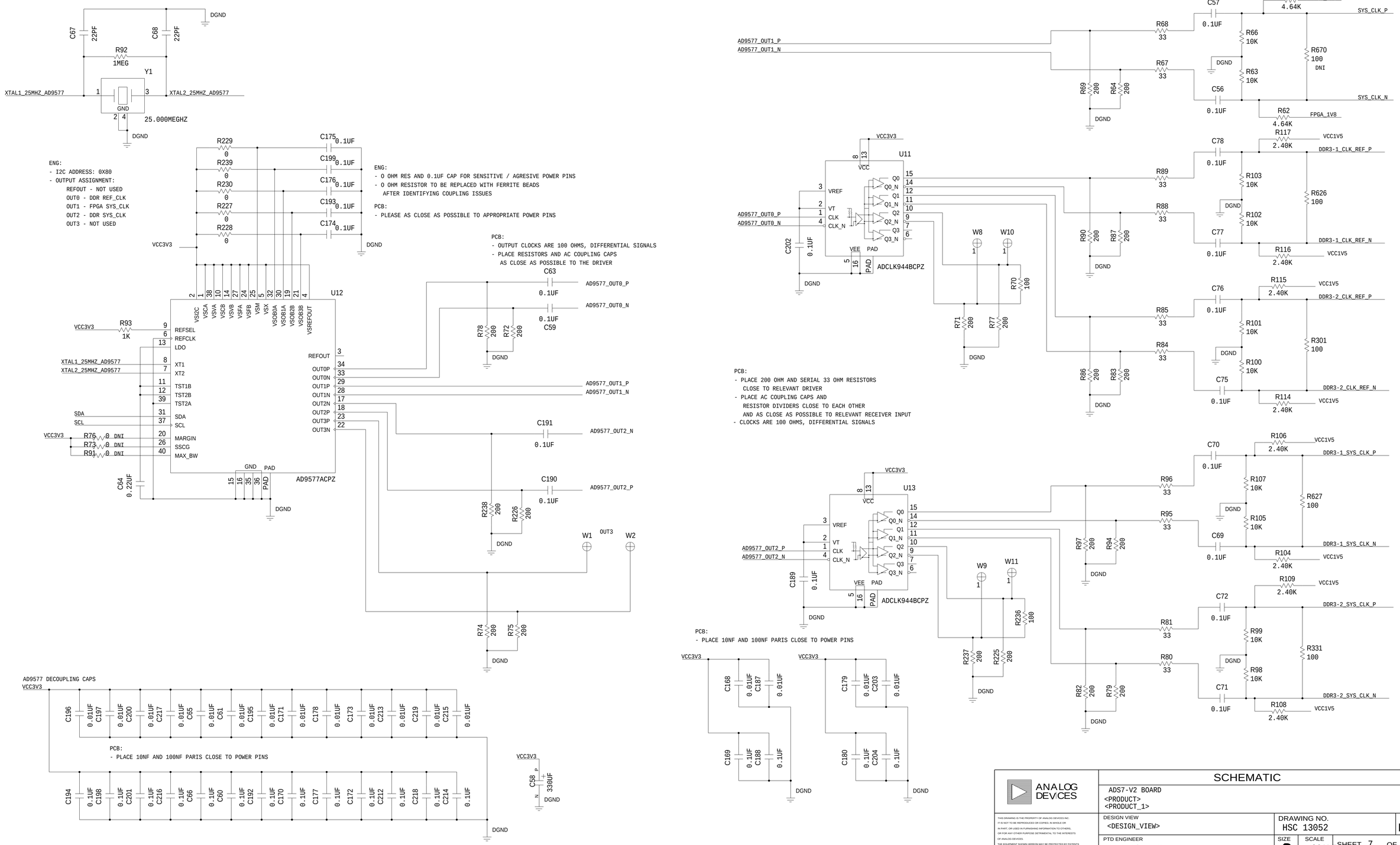
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE D / SCALE <SCALE>	SHEET 6 OF 23
<PTD_ENGINEER>		

DDR3 CLOCKING

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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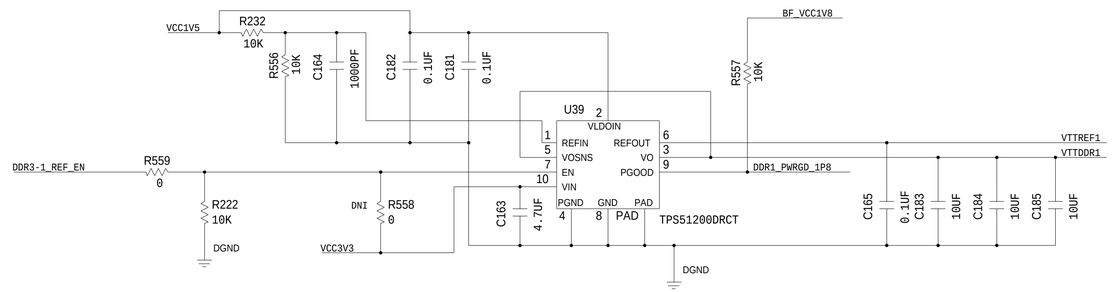
SCHEMATIC

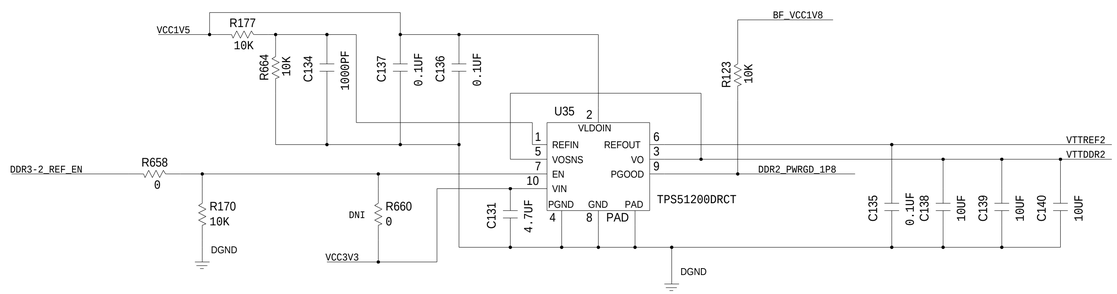
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 7 OF 23
<PTD_ENGINEER>	D / <SCALE>	

DDR3 REFERENCE VOLTAGES

DDR-1 AND DDR-2 VTTREF - 0.75V
DDR-1 AND DDR-2 VTTDDR - 0.75V





REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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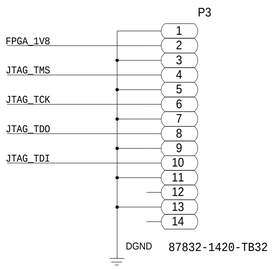
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 8 OF 23

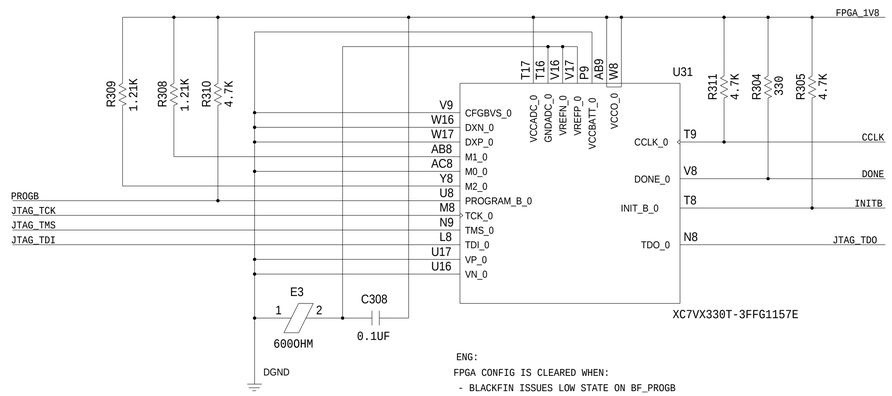
FPGA CONFIGURATION AND MISC BANKS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

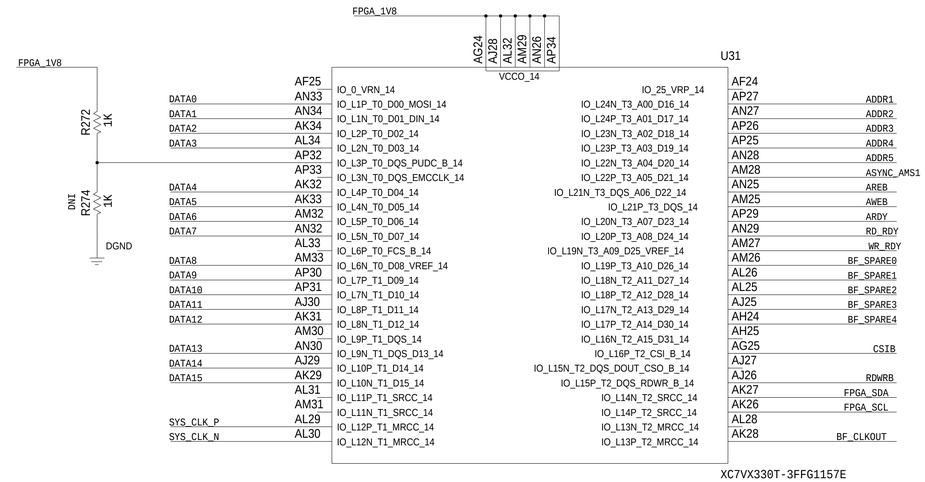
JTAG CONNECTOR



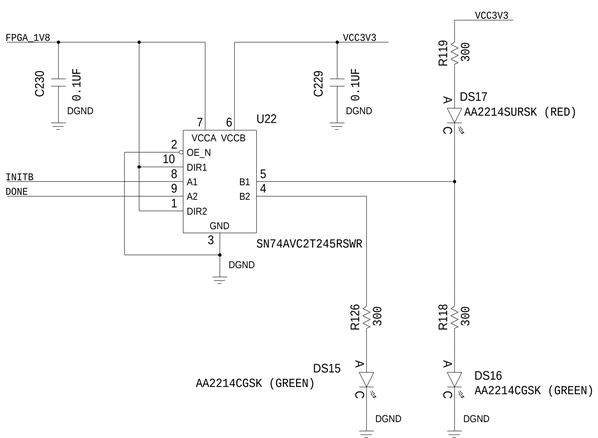
PCB:
- SILKSCREEN: 'FPGA JTAG'



ENG:
FPGA CONFIG IS CLEARED WHEN:
- BLACKFIN ISSUES LOW STATE ON BF_PROGB

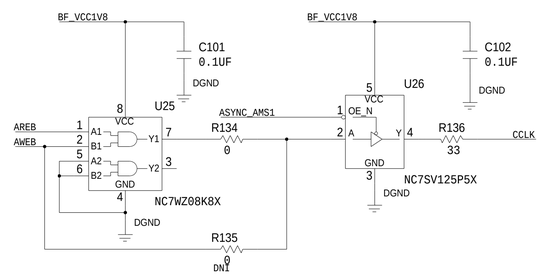


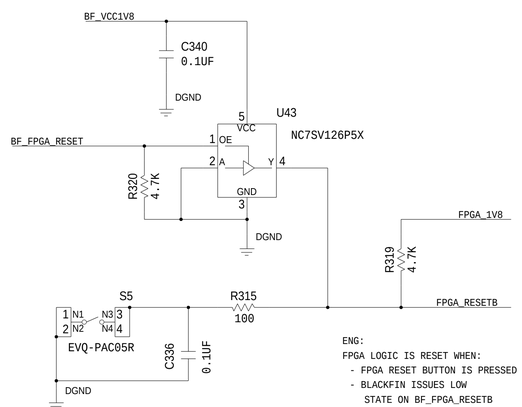
FPGA CONFIG SIGNALS LEVEL TRANSLATION



PCB:
- PLACE RED AND GREEN DS24 AND DS25 LED NEXT TO EACH OTHER
- DS24, DS25 SILKSCREEN: 'FPGA INITB'
- DS 23 SILKSCREEN: 'FPGA DONE'

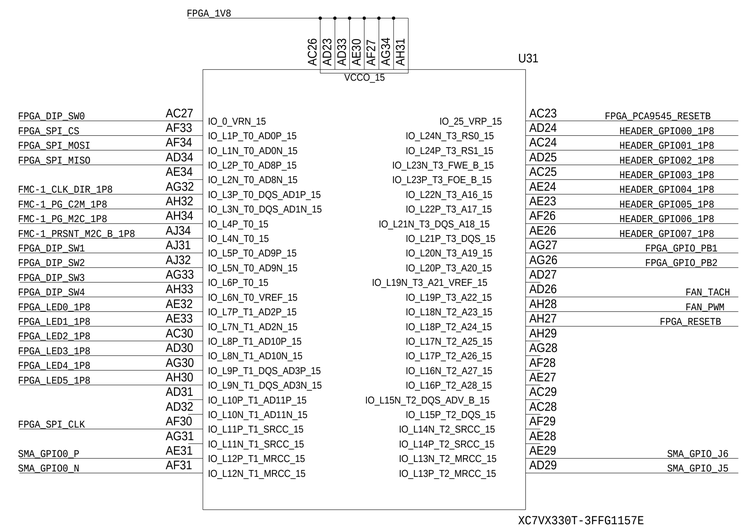
BLACKFIN FPGA CONFIG CLOCK BUFFER WITH 3-STATE OUTPUT





ENG:
FPGA LOGIC IS RESET WHEN:
- FPGA RESET BUTTON IS PRESSED
- BLACKFIN ISSUES LOW
STATE ON BF_FPGA_RESETB

FPGA RESET GENERATION
PCB:
- PLACE CLOSE TO BF527
- SILKSCREEN: 'FPGA RESETB'



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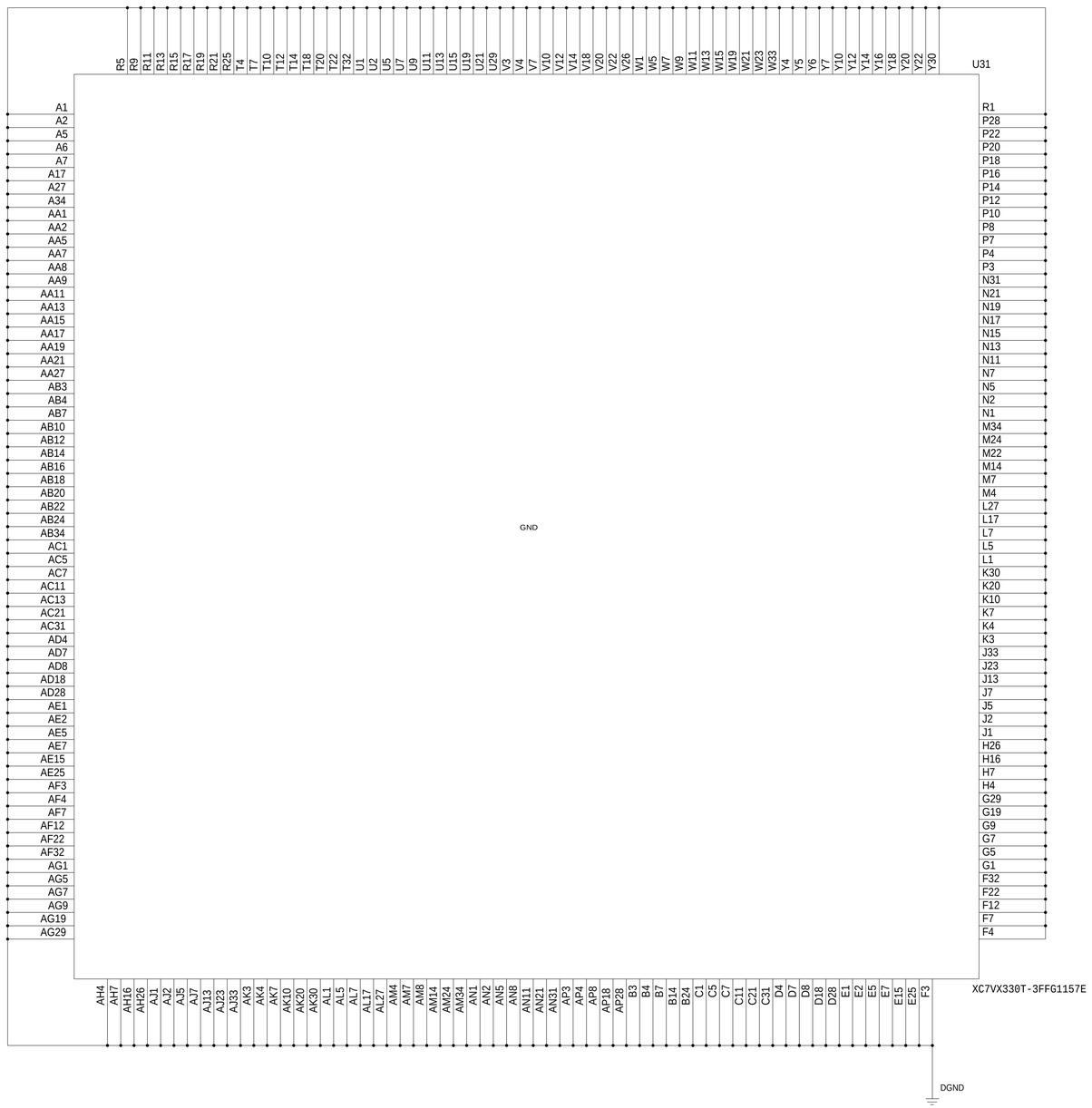
SCHEMATIC

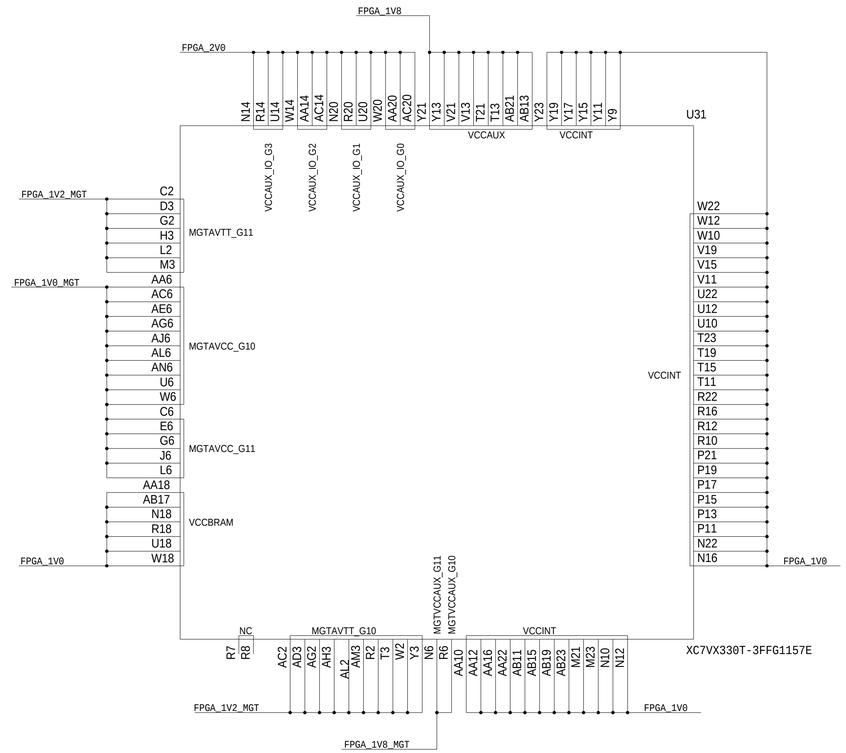
ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 9 OF 23

FPGA POWER AND GROUND

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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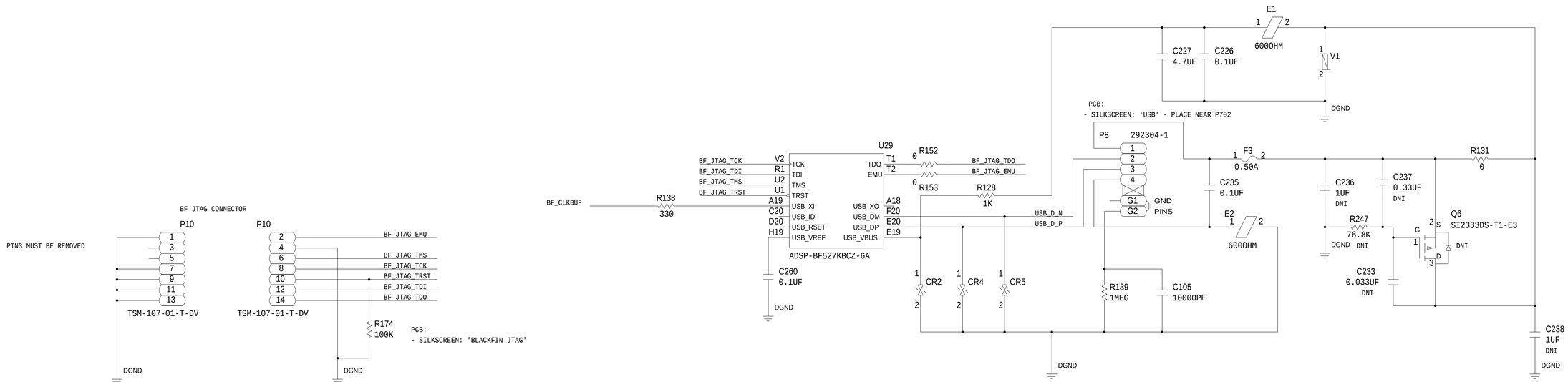
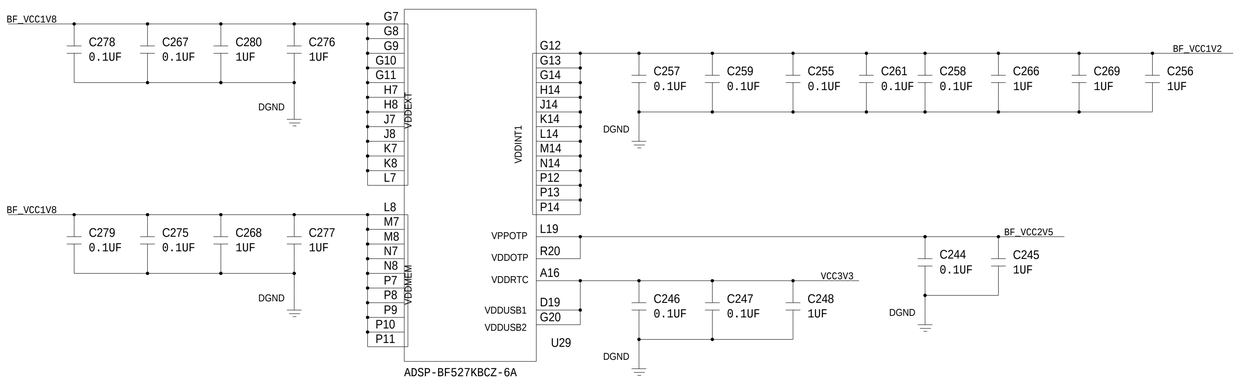
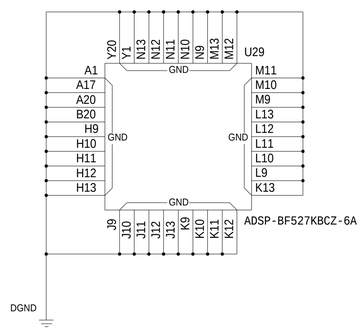
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE	SCALE
<PTD_ENGINEER>	D	<SCALE>

BLACKFIN

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED







ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE	SCALE
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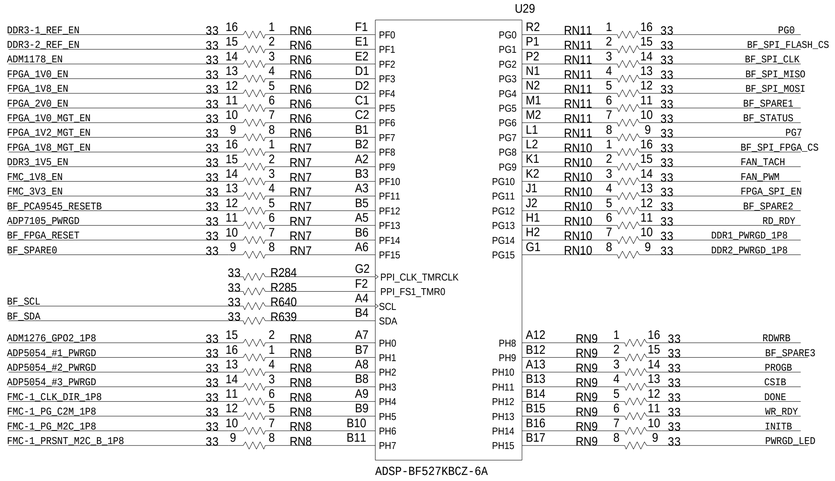
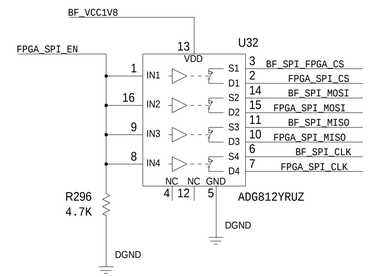
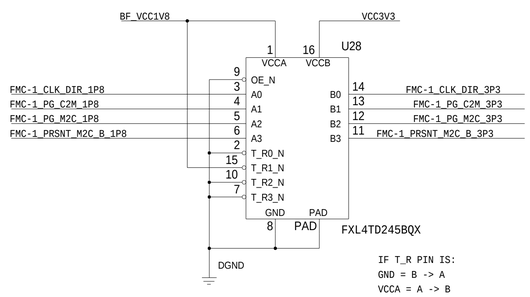
BLACKFIN IO

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

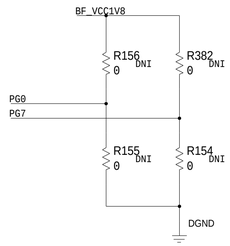


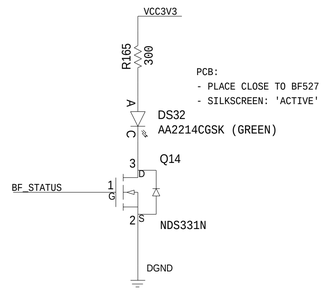


ADG812 SWITCHES CLOSE WHEN IN PIN GOES HIGH



IF T_R PIN IS:
GND = B -> A
VCCA = A -> B





PCB:
- PLACE CLOSE TO BF527
- SILKSCREEN: 'ACTIVE'

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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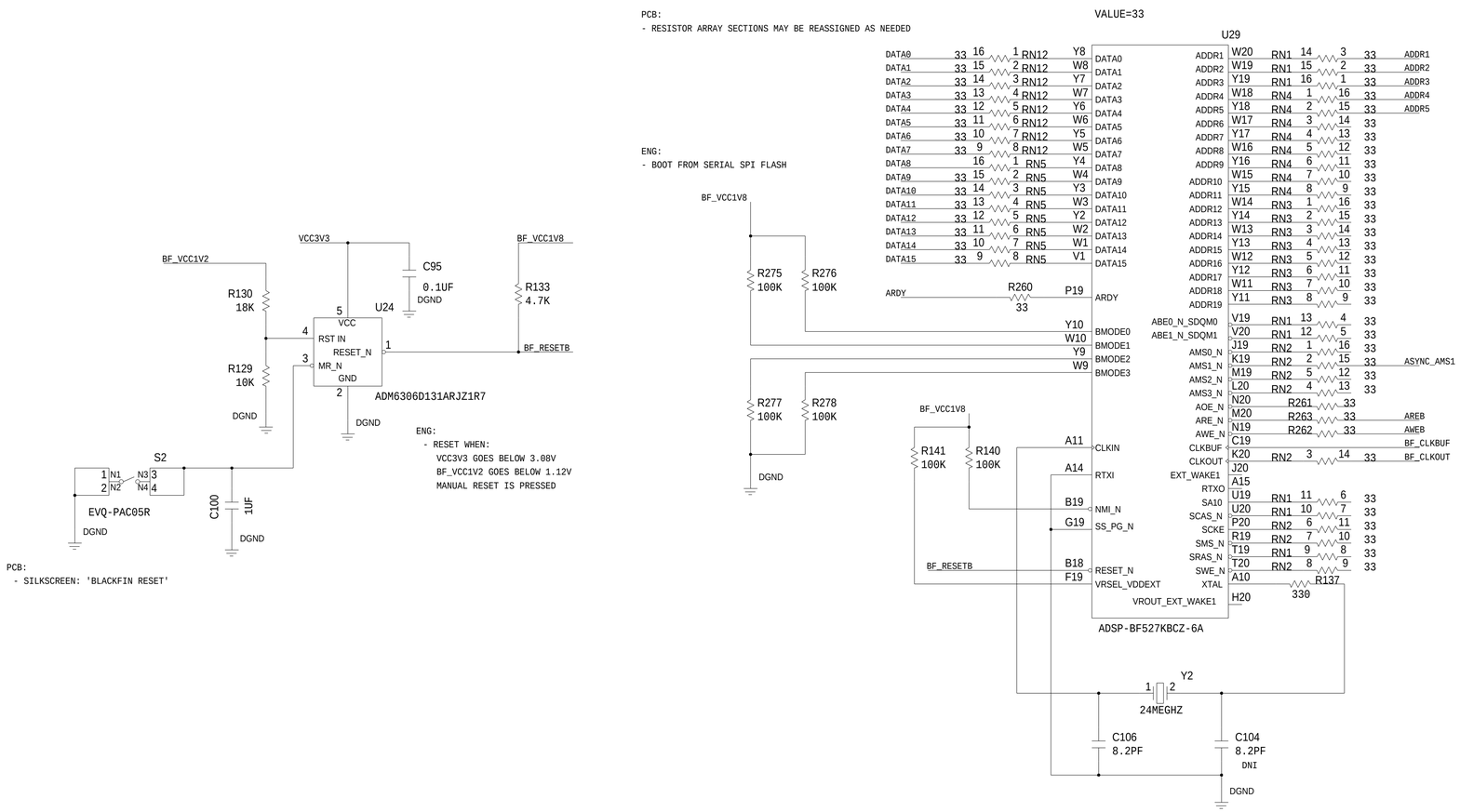
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 12 OF 23

BLACKFIN MEMORIES AND RESET

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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SCHEMATIC

ADS7-V2 BOARD
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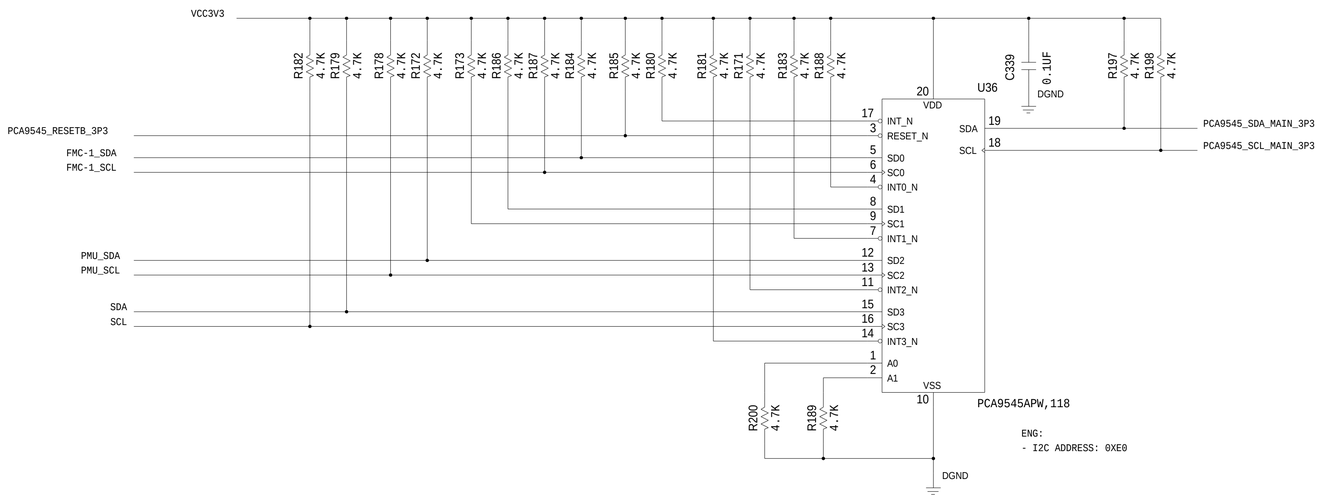
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 13 OF 23
<PTD_ENGINEER>	D / <SCALE>	

I2C MUX

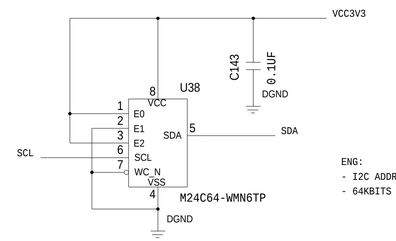
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



PCA9545APW,118

ENG:
- I2C ADDRESS: 0XE0

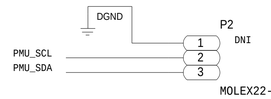
I2C EEPROM



M24C64-WMN6TP

ENG:
- I2C ADDRESS: 0XAA
- 64KBITS

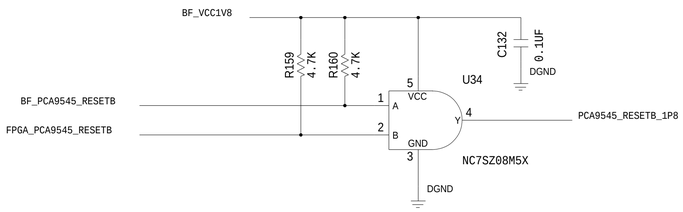
PMU I2C HEADER



MOLEX22-23-2031

PCB
- SILKSCREEN: 'PMU I2C' - PLACE ABOVE THE CONNECTOR

PCA9545 RESET GENERATION



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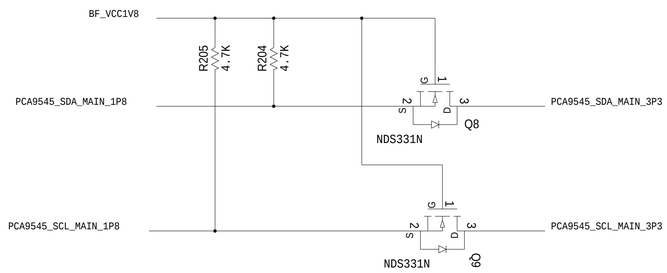
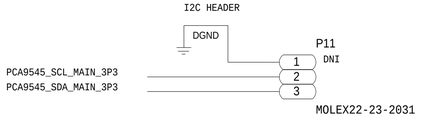


NDS331N

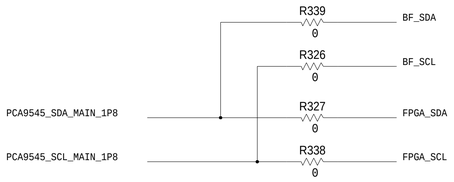
NDS331N

I2C HEADER



MOLEX22-23-2031

PCB
- SILKSCREEN: 'I2C' - PLACE ABOVE THE CONNECTOR



I2C MAP:

DEVICE	ADDRESS (8-BIT FORMAT -> I2C ADDRESS BYTE + R/W BIT)			
PCA9545APW	0XE0			
	BUS 3	BUS 2	BUS 1	BUS0
ADM1276		0X40		
ADM1178		0XE4		
ADM1293		0X22,0X24,0X26 0X82,0X84,0X86 0X88,0X8A,0X8C		
AD9577	0X80			
DDR3 MEM TEMP SENSOR	0X34, 0X36			
DDR3 SPD EEPROM	0XA4, 0XA6			
AD5258	0X30			
RTC-8564	0XA2			
ADS7-V1 EEPROM	0XAA			
FMC EEPROM				0XA0
FMC DEVICES				0X??

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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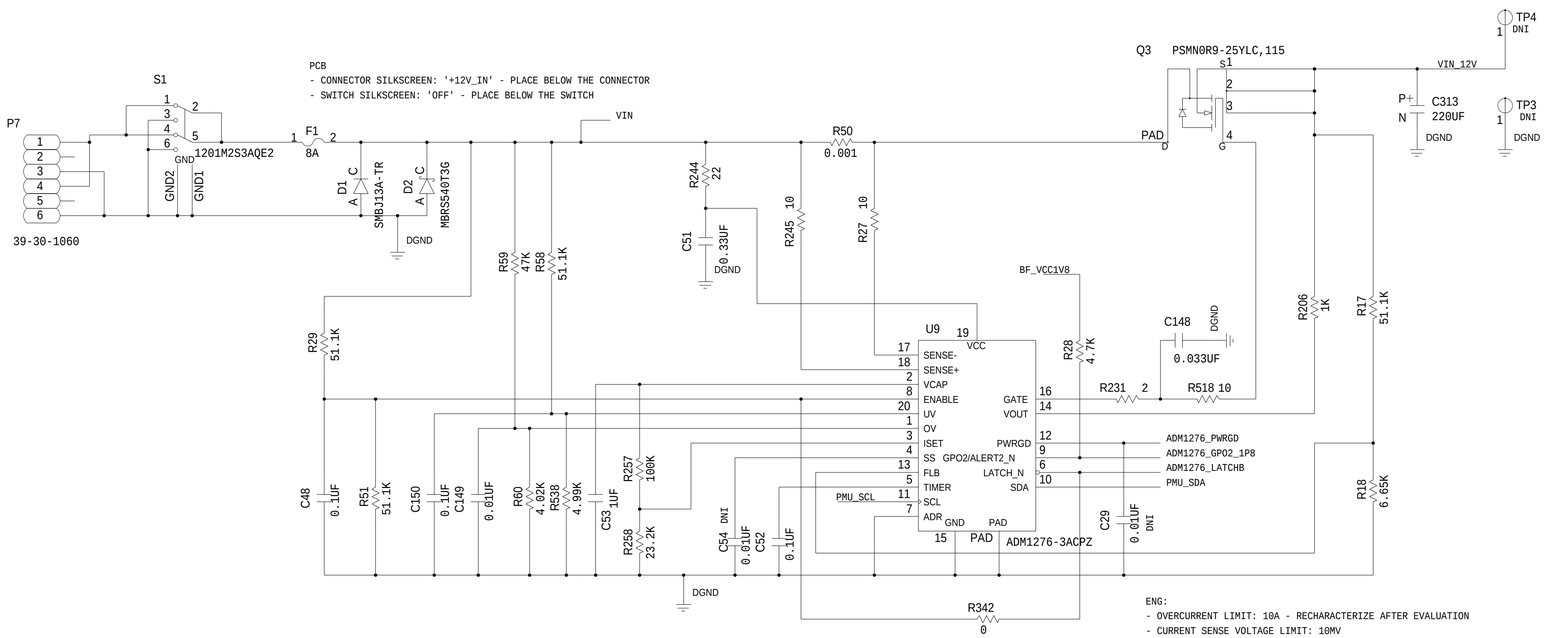
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 14 OF 23
<PTD_ENGINEER>	D / <SCALE>	

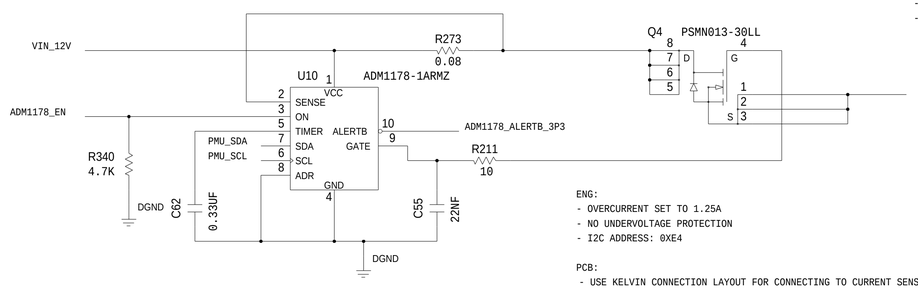
POWER INPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



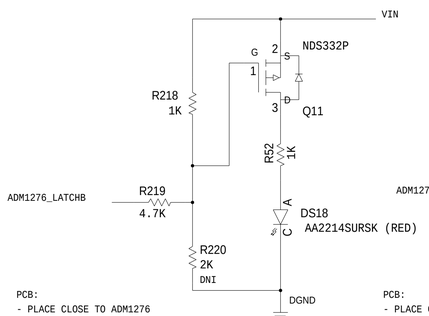
ENG:
- OVERCURRENT LIMIT: 10A - RECHARACTERIZE AFTER EVALUATION
- CURRENT SENSE VOLTAGE LIMIT: 10MV
- OV = 12.692V, UV = 11.24V
- SOFT-START = 1MS
- T INIT = 7.5MS
- I2C ADDRESS: 0X40
- NO AUTO-RETRY

PCB:
- PLACE POWER INPUT CONNECTOR NEXT TO POWER ON/OFF SWITCH
- SILK SCREEN INFORMATION:
  '+12V_IN' - BELOW P4 CONNECTOR
  'OFF' - BELOW S2 SWITCH

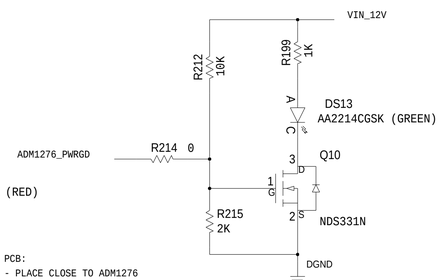


ENG:
- OVERCURRENT SET TO 1.25A
- NO UNDERVOLTAGE PROTECTION
- I2C ADDRESS: 0XE4

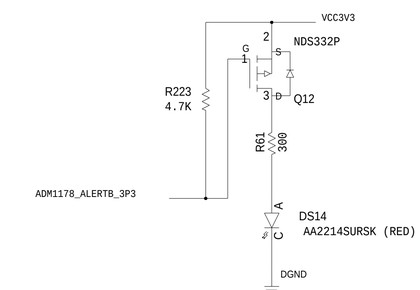
PCB:
- USE KELVIN CONNECTION LAYOUT FOR CONNECTING TO CURRENT SENSE RESISTOR



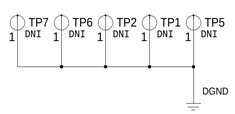
PCB:
- PLACE CLOSE TO ADM1276
- SILKSCREEN: 'LATCHB'



PCB:
- PLACE CLOSE TO ADM1276
- SILKSCREEN: '12V_VIN'



PCB:
- PLACE CLOSE TO ADM1276
- SILKSCREEN: 'FMC_12V OVERCURRENT'



ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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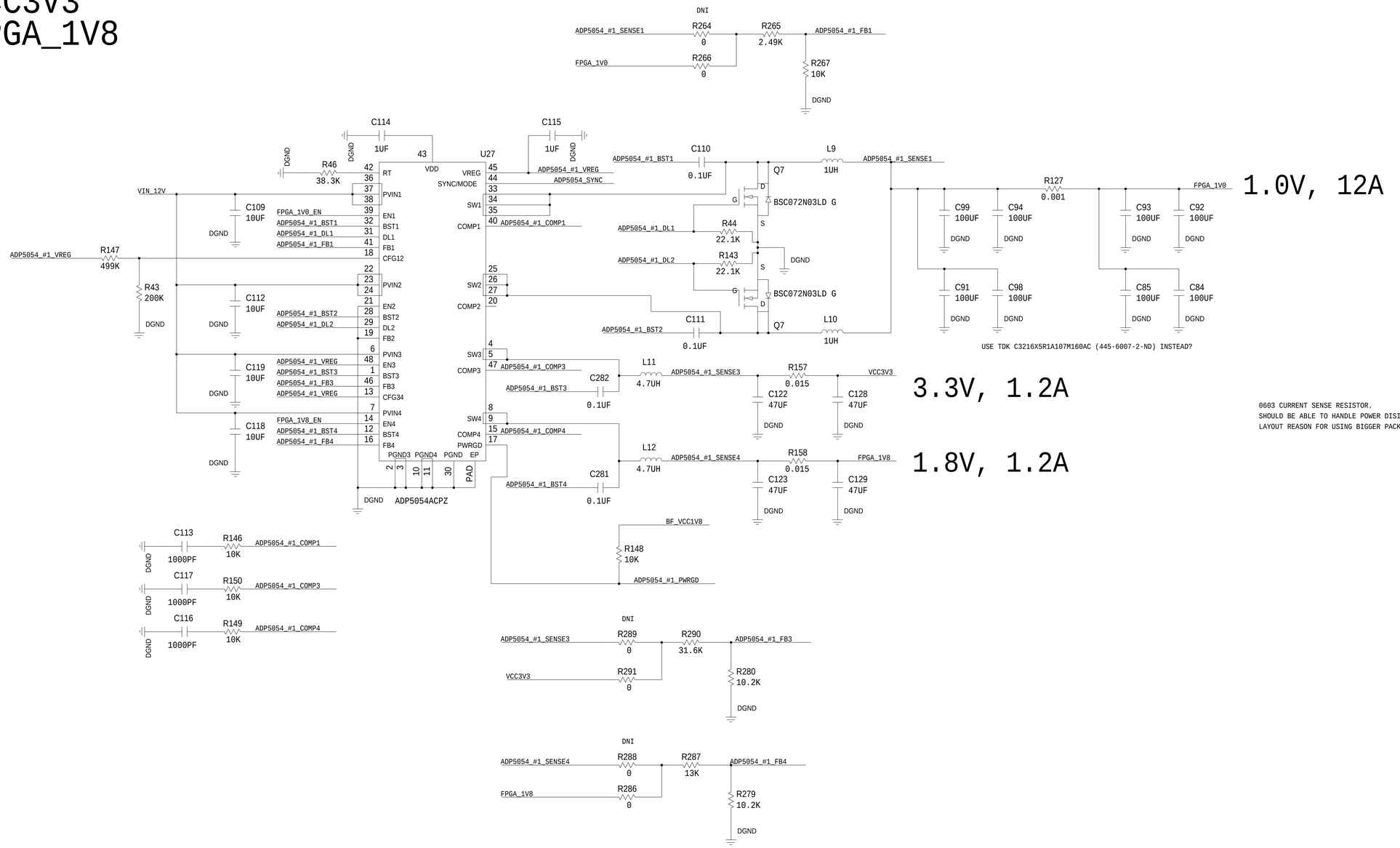
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 15 OF 23

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER ADP5054#1

FPGA_1V0
VCC3V3
FPGA_1V8



0603 CURRENT SENSE RESISTOR.
SHOULD BE ABLE TO HANDLE POWER DISIPATION.
LAYOUT REASON FOR USING BIGGER PACKAGE?

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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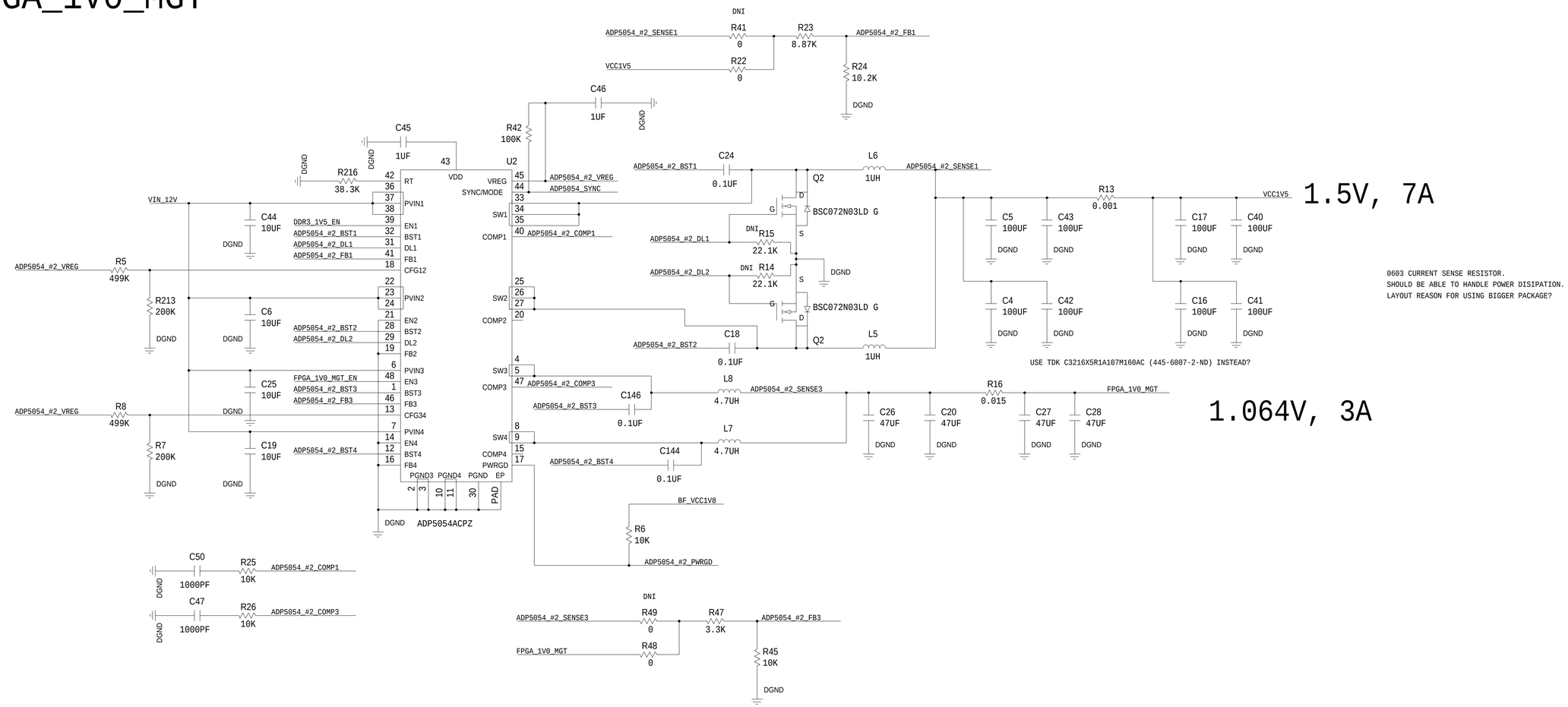
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 16 OF 23
<PTD_ENGINEER>	D / <SCALE>	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER ADP5054#2

VCC1V5

FPGA_1V0_MGT



0603 CURRENT SENSE RESISTOR.
SHOULD BE ABLE TO HANDLE POWER DISIPATION.
LAYOUT REASON FOR USING BIGGER PACKAGE?

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

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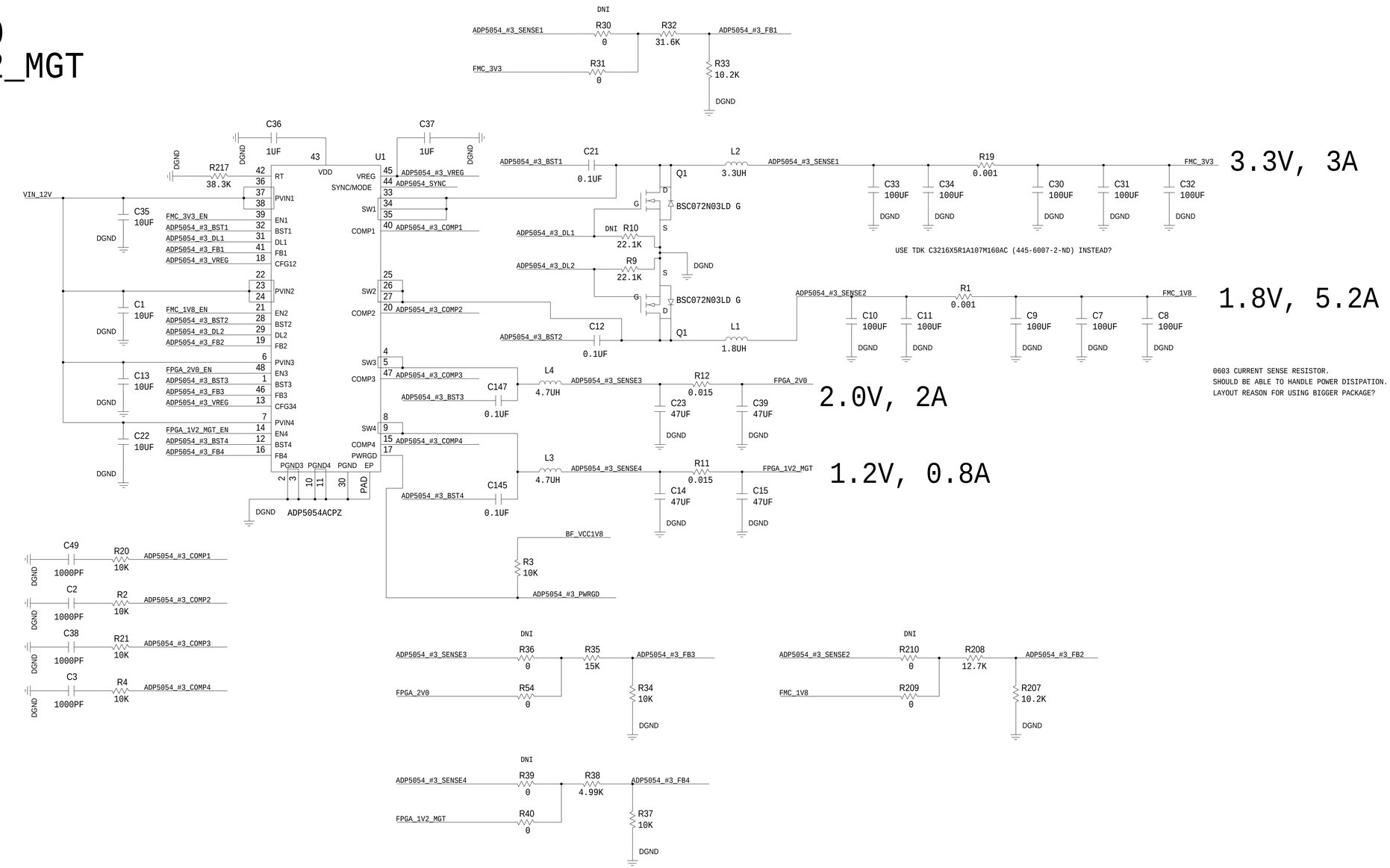
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 17 OF 23

POWER ADP5054#3

FMC_3V3
FMC_1V8
FPGA_2V0
FPGA_1V2_MGT



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
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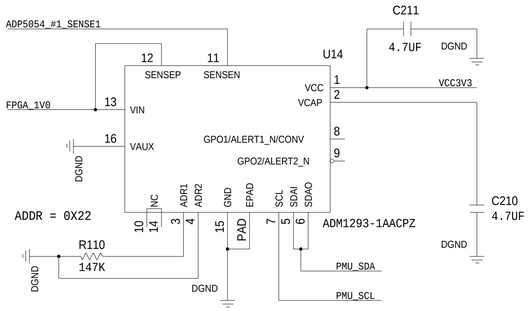
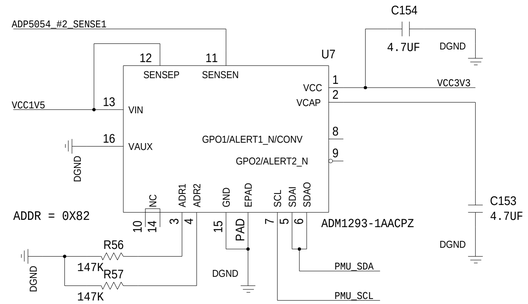
DESIGN VIEW <DESIGN_VIEW>
DRAWING NO. HSC 13052
REV B
PTD ENGINEER <PTD_ENGINEER>
SIZE D
SCALE <SCALE>
SHEET 18 OF 23

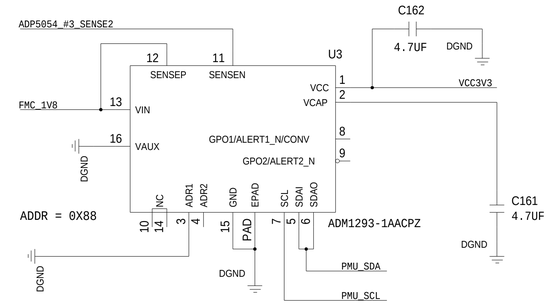
POWER MEASUREMENT

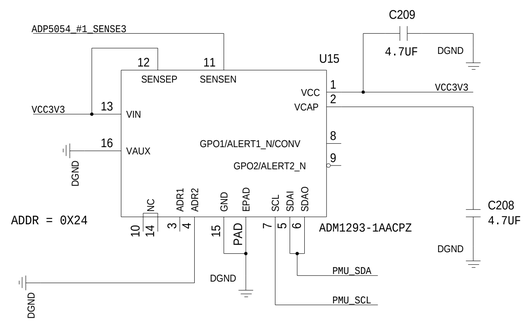
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

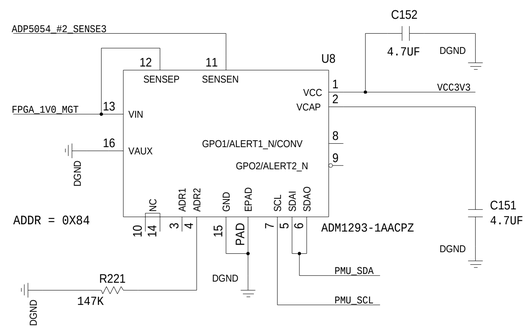
ADM1293 ADDRESSES:
00 = ADR PIN TIED TO GROUND
01 = ADR PIN TIED TO GROUND THROUGH 147K RESISTOR
10 = ADR PIN NOT CONNECTED
11 = ADR PIN TIED TO VCAP

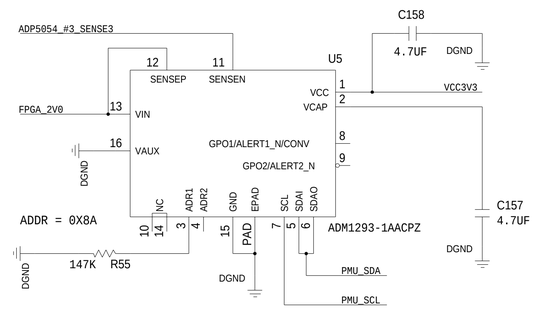


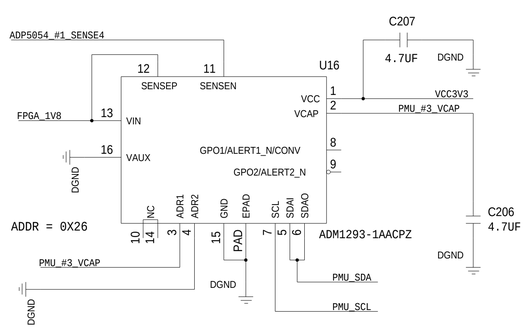


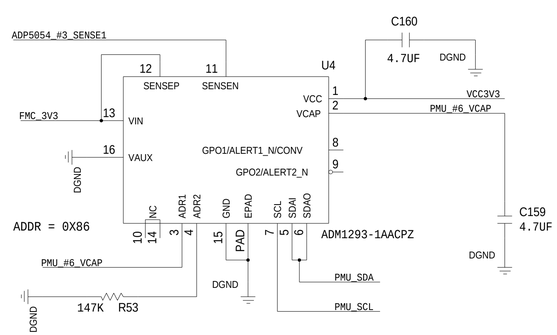


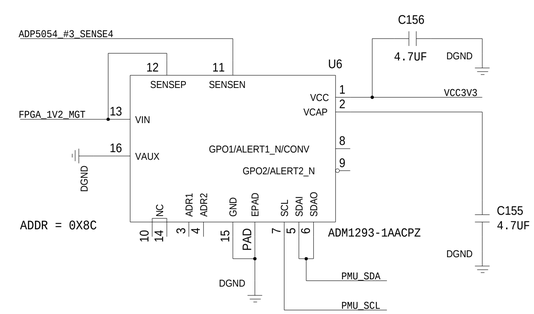












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SCHEMATIC

ADS7-V2 BOARD
<PRODUCT>
<PRODUCT_1>

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE / SCALE	SHEET 19 OF 23
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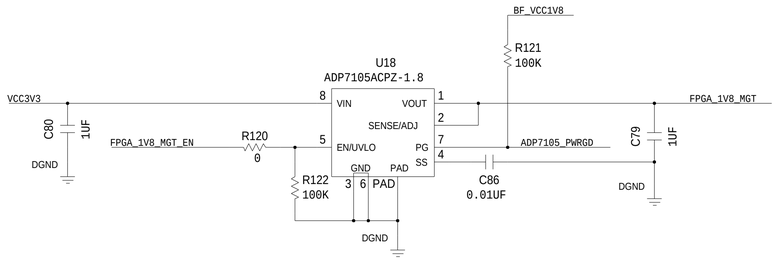
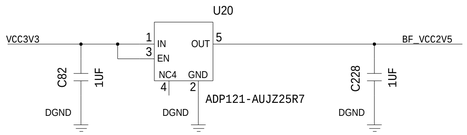
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER - LINEAR



1.8V, 0.5A



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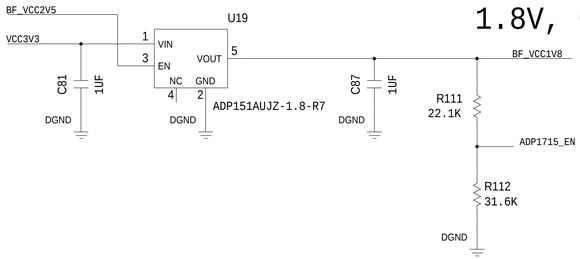
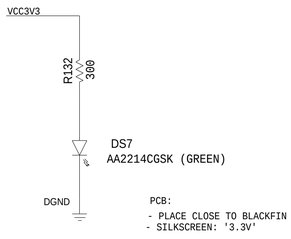
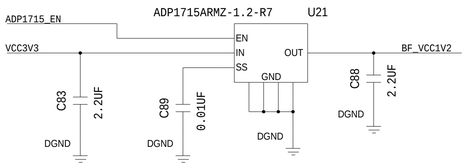


1.8V, 0.2A, BLACKFIN





1.2V, 0.5A, BLACKFIN

ANALOG DEVICES

SCHEMATIC

ADS7-V2 BOARD
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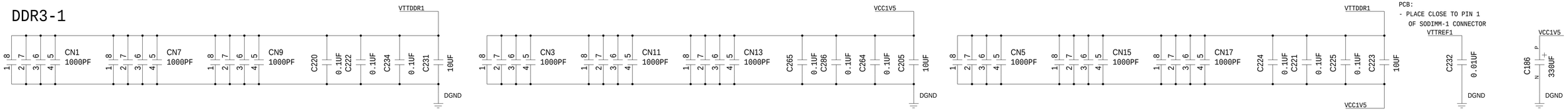
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 20 OF 23

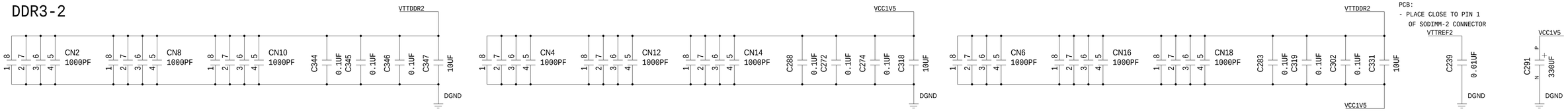
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DECOUPLING CAPS

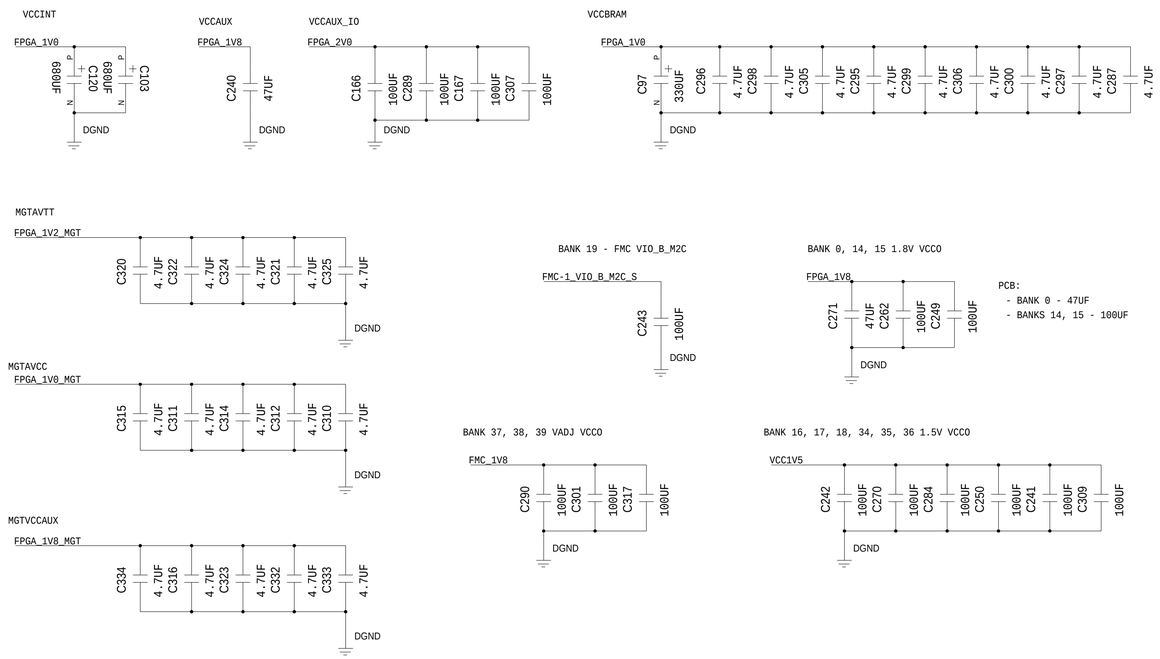
DDR3-1



DDR3-2



FPGA



ANALOG DEVICES

SCHEMATIC			
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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 13052		REV B
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 21 OF 23

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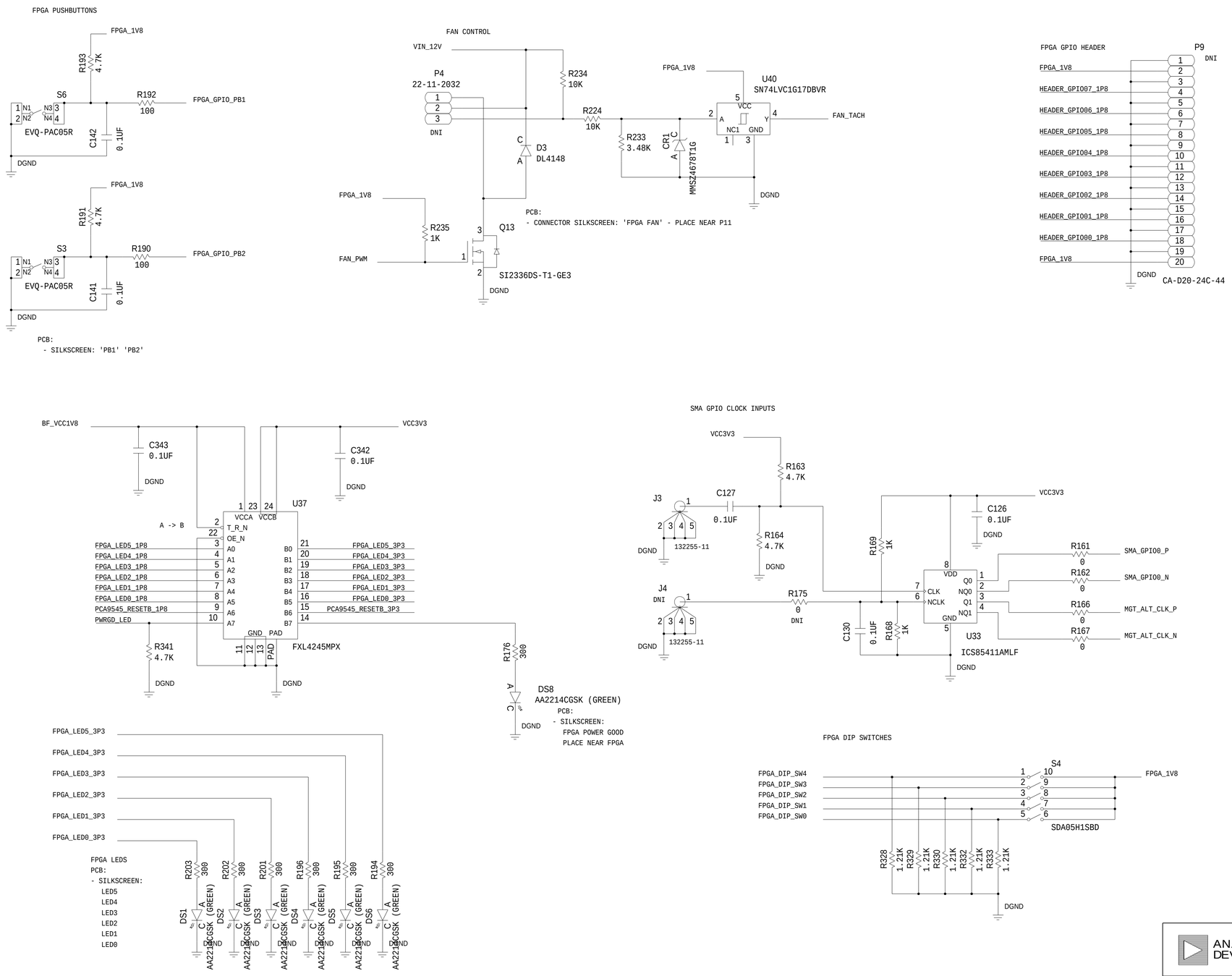
FAN CONTROL, FPGA GPIO, BUTTONS, RTC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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ADS7-V2 BOARD
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DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 13052	B
PTD ENGINEER	SIZE D / SCALE <SCALE>	SHEET 22 OF 23
<PTD_ENGINEER>		

OTHER COMMENTS

MECHANICAL COMPONENTS:

PCB BOARD STANDOFFS:

STANDOFFS:
- ETTINGER - 05.03.123 - SPACER, M3X12-NI
- FARNELL STOCK CODE: 1466772
- QTY: 6

SCREWS:
- DURATOOL - M36 PRA2MCS100- - SCREW, POZI PAN, S/S, A2, M3X6
- FARNELL STOCK CODE: 1420032
- QTY: 12

RUBBER BUMPER:
- KEYSTONE - 720 - RECESSED BUMPERS, RUBBER
- FARNELL STOCK CODE: 1651664
- QTY: 6

REVISIONS			
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DESIGN VIEW <DESIGN_VIEW>

DRAWING NO. HSC 13052

REV B

PTD ENGINEER <PTD_ENGINEER>

SIZE D

SCALE <SCALE>