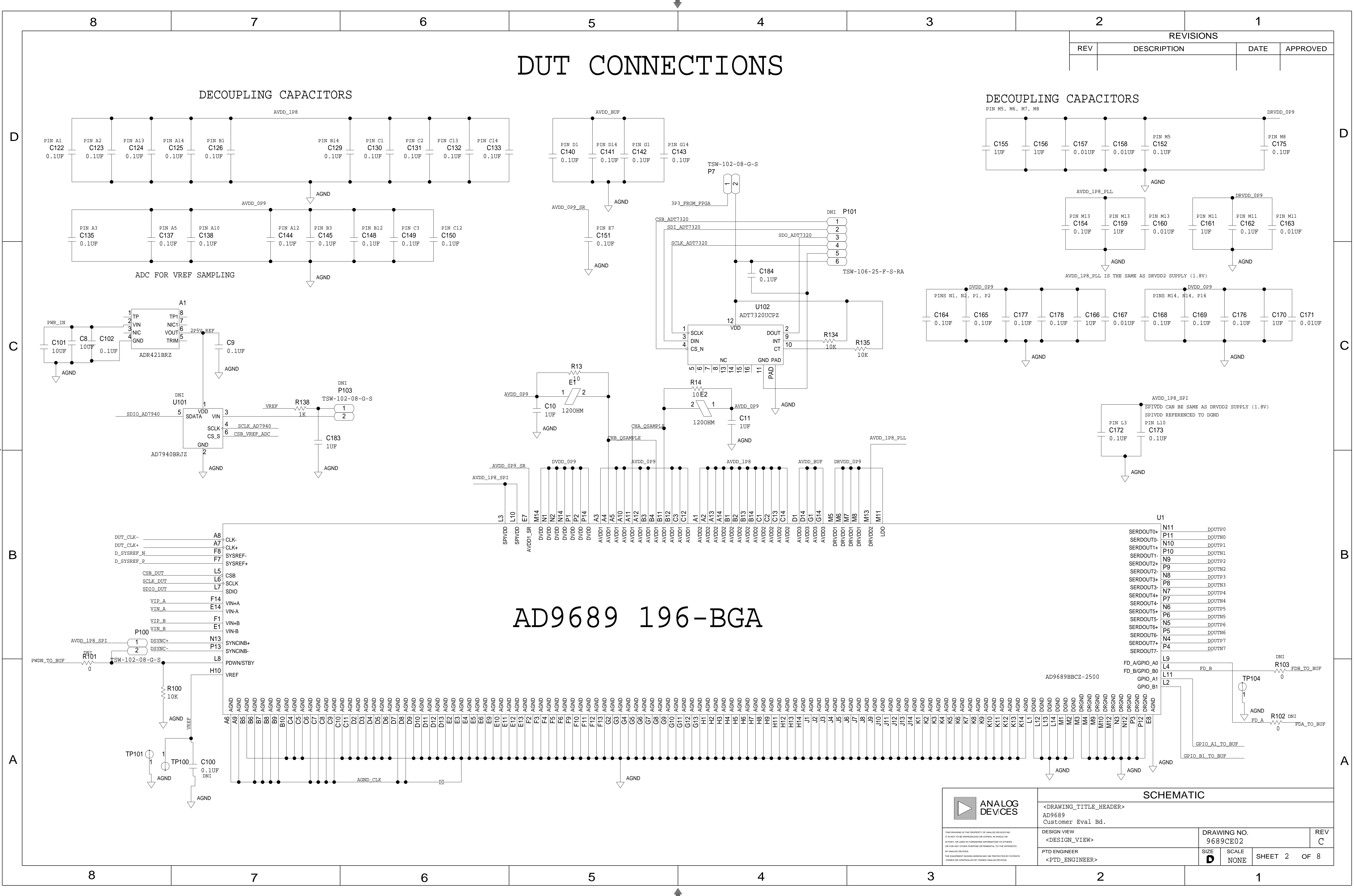


DUT CONNECTIONS

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AD9689 196-BGA

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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE NONE	SHEET 2 OF 8

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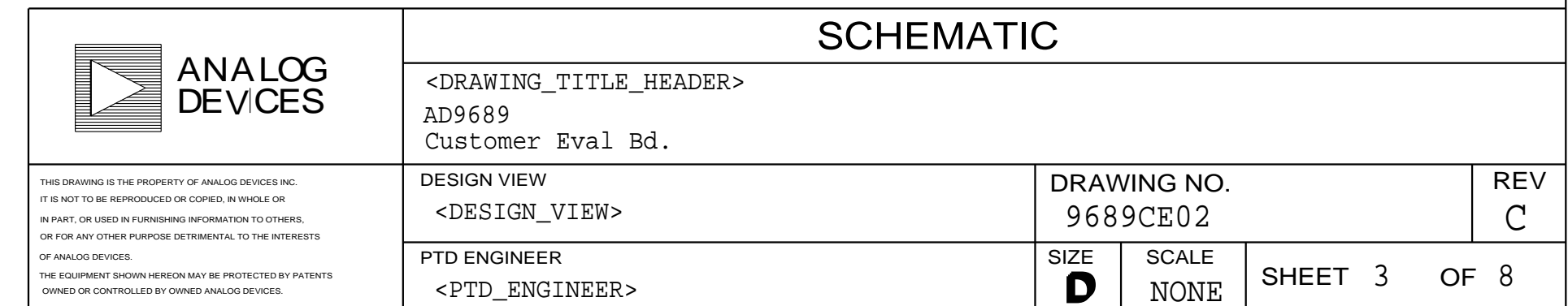
Diagram illustrating the clock distribution network for the T200 TCM1-83X+ device, showing connections to three LTI-SASF546GT-P26-X1 drivers (J1, J201, J2) and the DUT.

Components and Connections:

- Drivers (J1, J201, J2):** LTI-SASF546GT-P26-X1. Each driver has pins 1 (DNI), 2 (AGND_CLK), 3 (AGND_CLK), 4 (AGND_CLK), and 5 (AGND_CLK).
- T200 (TCM1-83X+):** The central device with pins 1 (DNI), 2 (DNI), 3 (DNI), 4 (DNI), 5 (DNI), and 6 (NC).
- Capacitors:**
 - C1 (0.1uF) connects DNI pin 1 to SHARE PADS.
 - C2 (0.1uF) connects DNI pin 1 to SHARE PADS.
 - C204 (0.1uF) connects DNI pin 2 to SHARE PADS.
 - C205 (0.1uF) connects DNI pin 2 to SHARE PADS.
 - C15 (0.1uF) connects DNI pin 2 to AGND.
- Resistors:**
 - R23 (49.9 ohms) connects DNI pin 2 to DUT_CLK+.
 - R22 (49.9 ohms) connects DNI pin 2 to DUT_CLK-.
 - R222 (100 ohms) connects DUT_CLK+ to DUT_CLK-.
- SHARE PADS:** A common connection point for the capacitors C1, C2, C204, and C205.
- DUT:** The target device with pins DUT_CLK+ and DUT_CLK-.

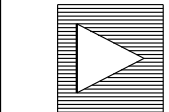
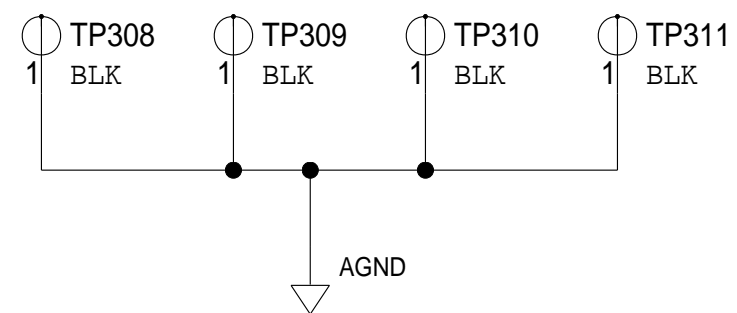
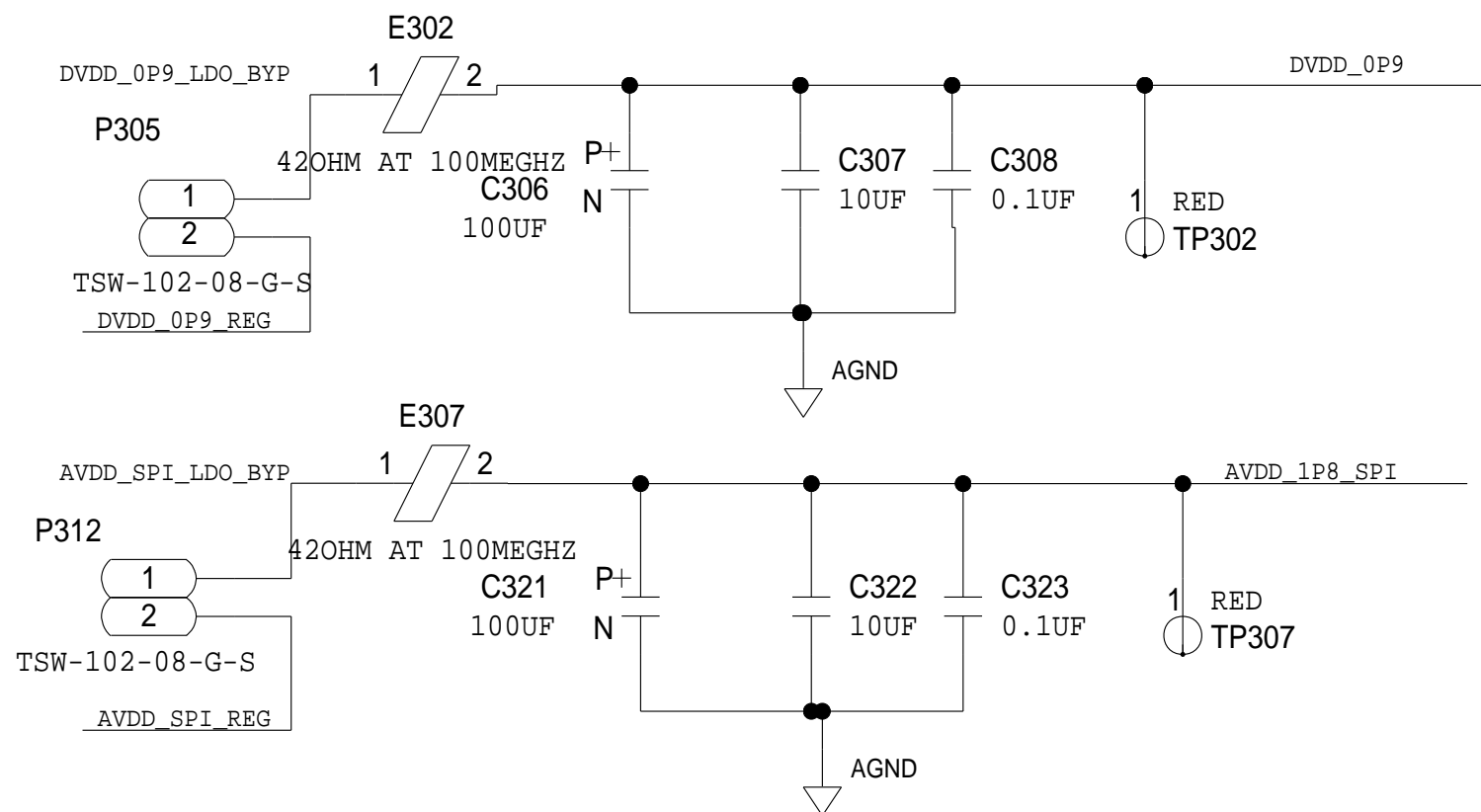
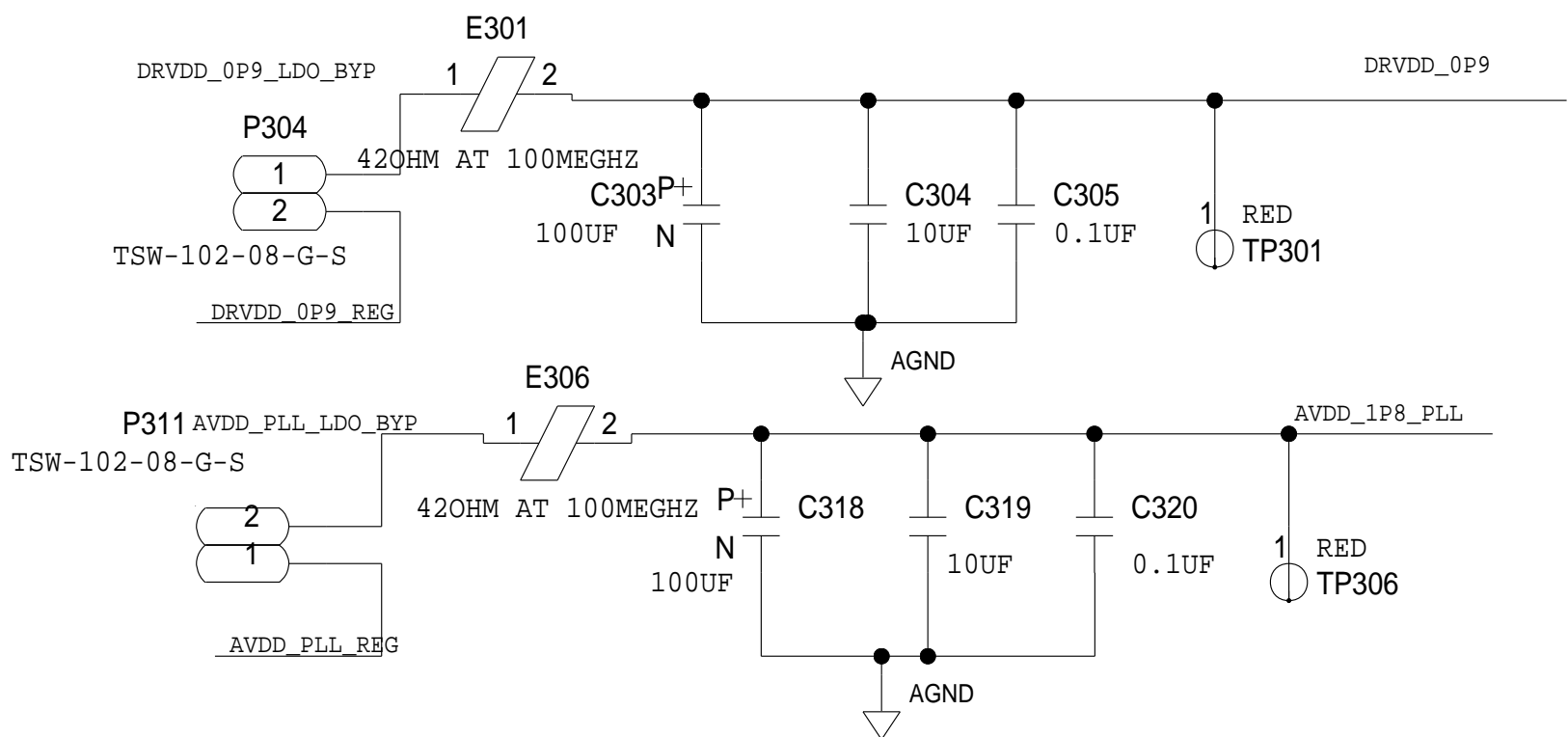
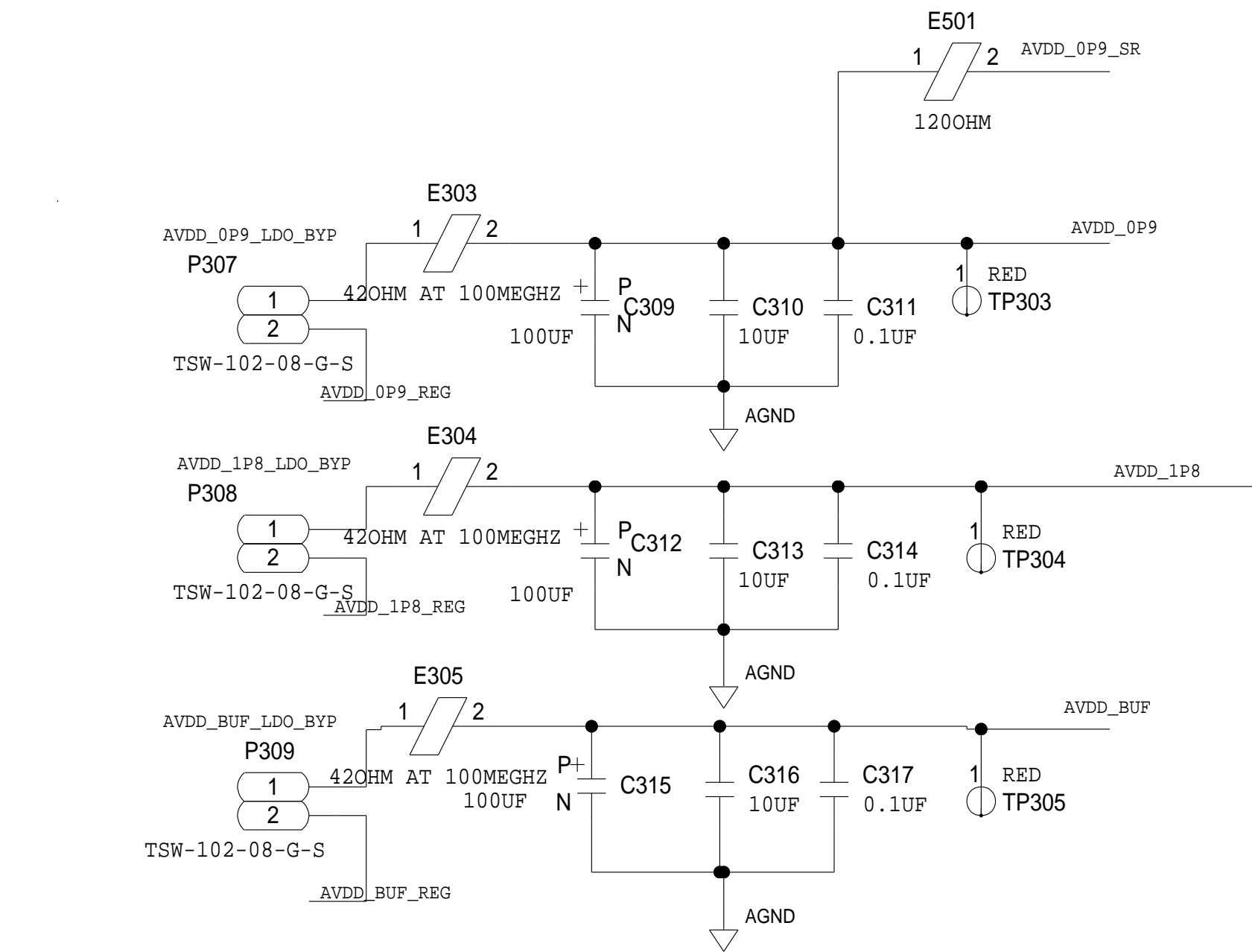
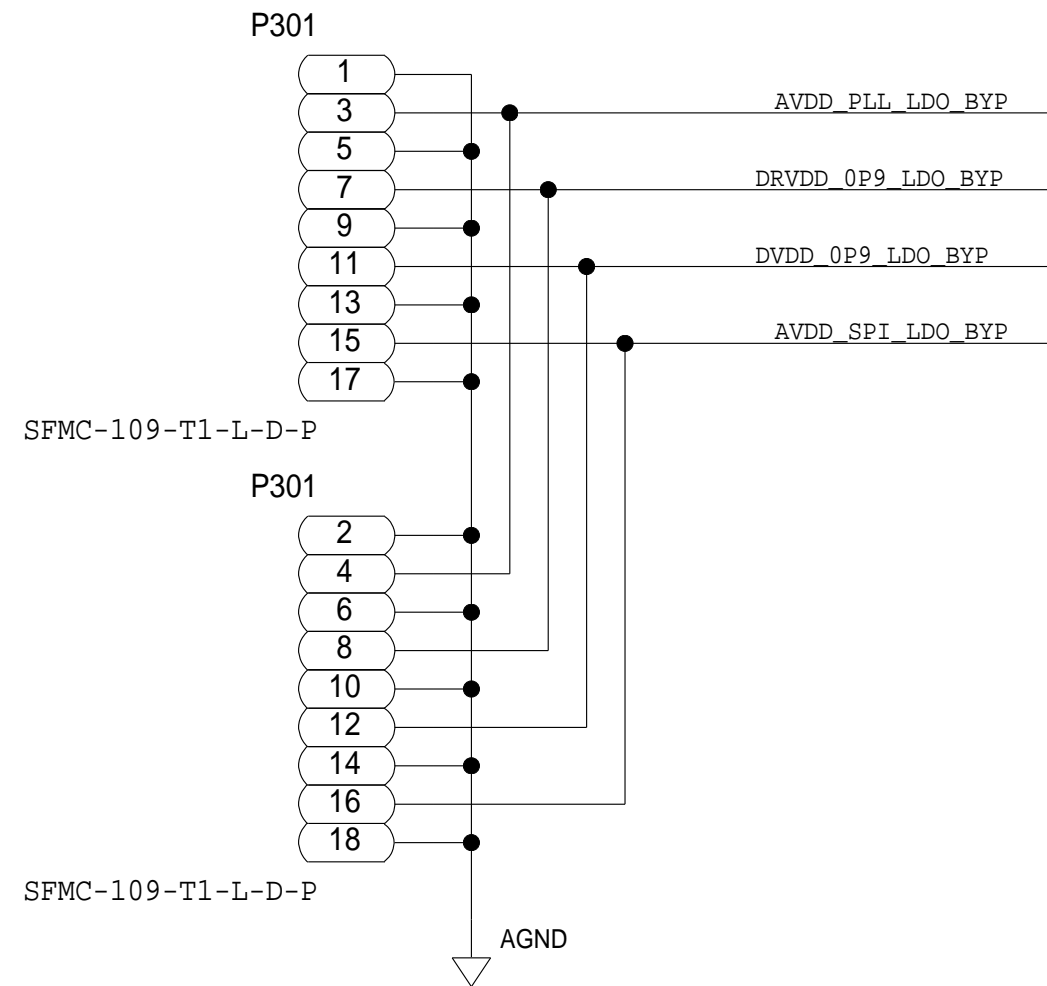
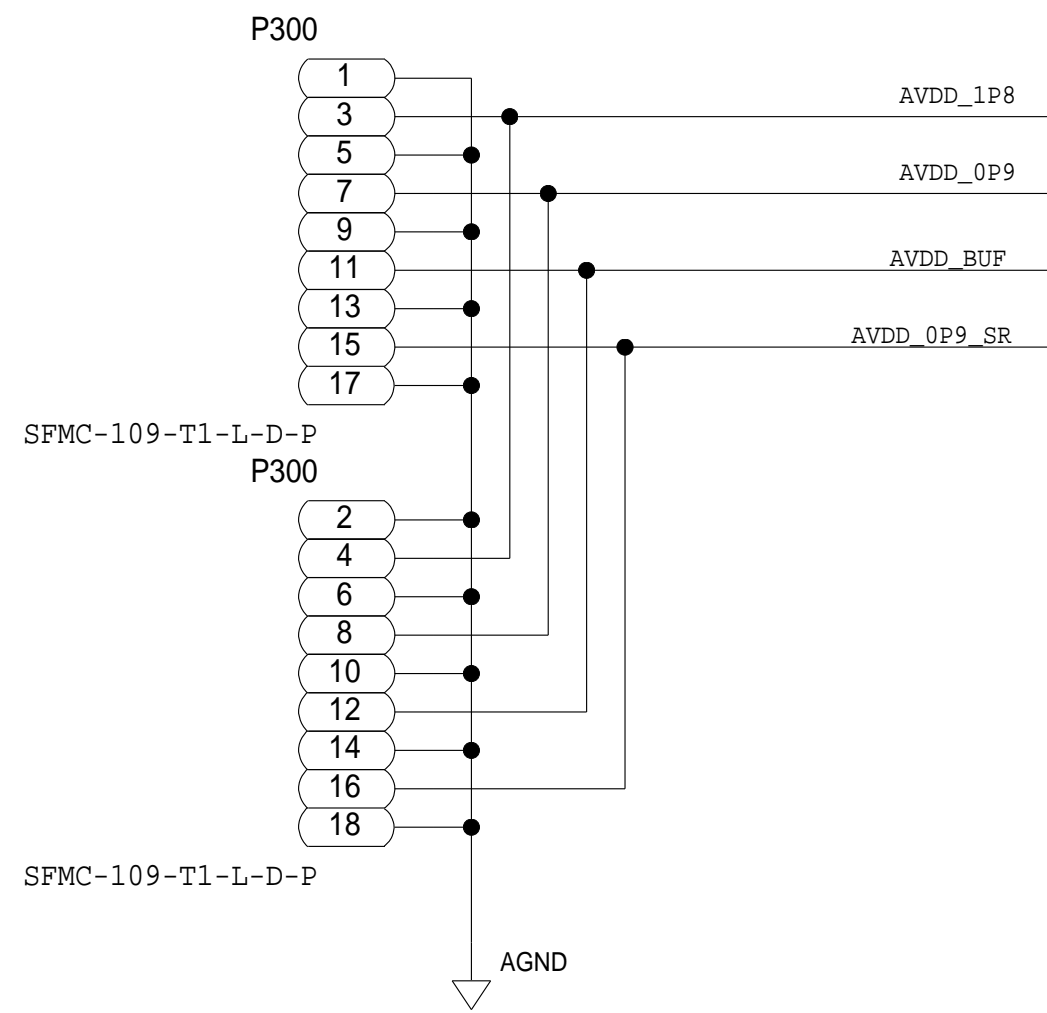
[illegible]

The diagram shows a DSYNC circuit. On the left, two input lines from an FPGA are labeled "FROM FPGA", "SYNC_TO_DUT+", and "SYNC_TO_DUT-". These lines connect to two resistors, R213 and R214, which are both labeled with a value of 0. R213 connects to a node labeled "DSYNC+", and R214 connects to a node labeled "DSYNC-". These nodes are connected to two circular connectors at the top and bottom. The top connector is labeled "DNI", "TP200", and "YEL". The bottom connector is labeled "YEL", "TP201", and "DNI". A resistor labeled R215 with a value of 100 is connected between the "DSYNC+" and "DSYNC-" nodes.



AD9689 POWER CONNECTIONS

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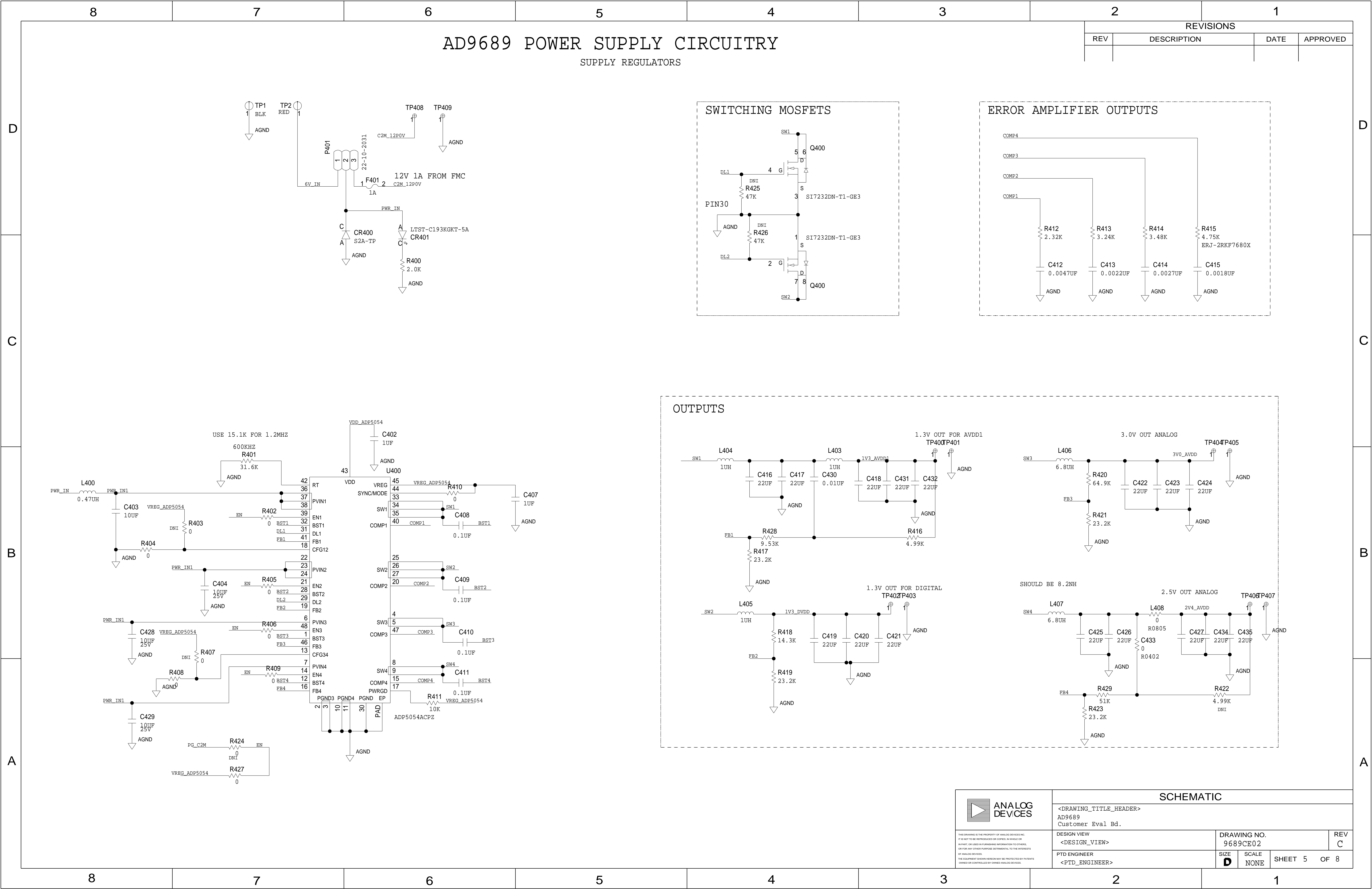
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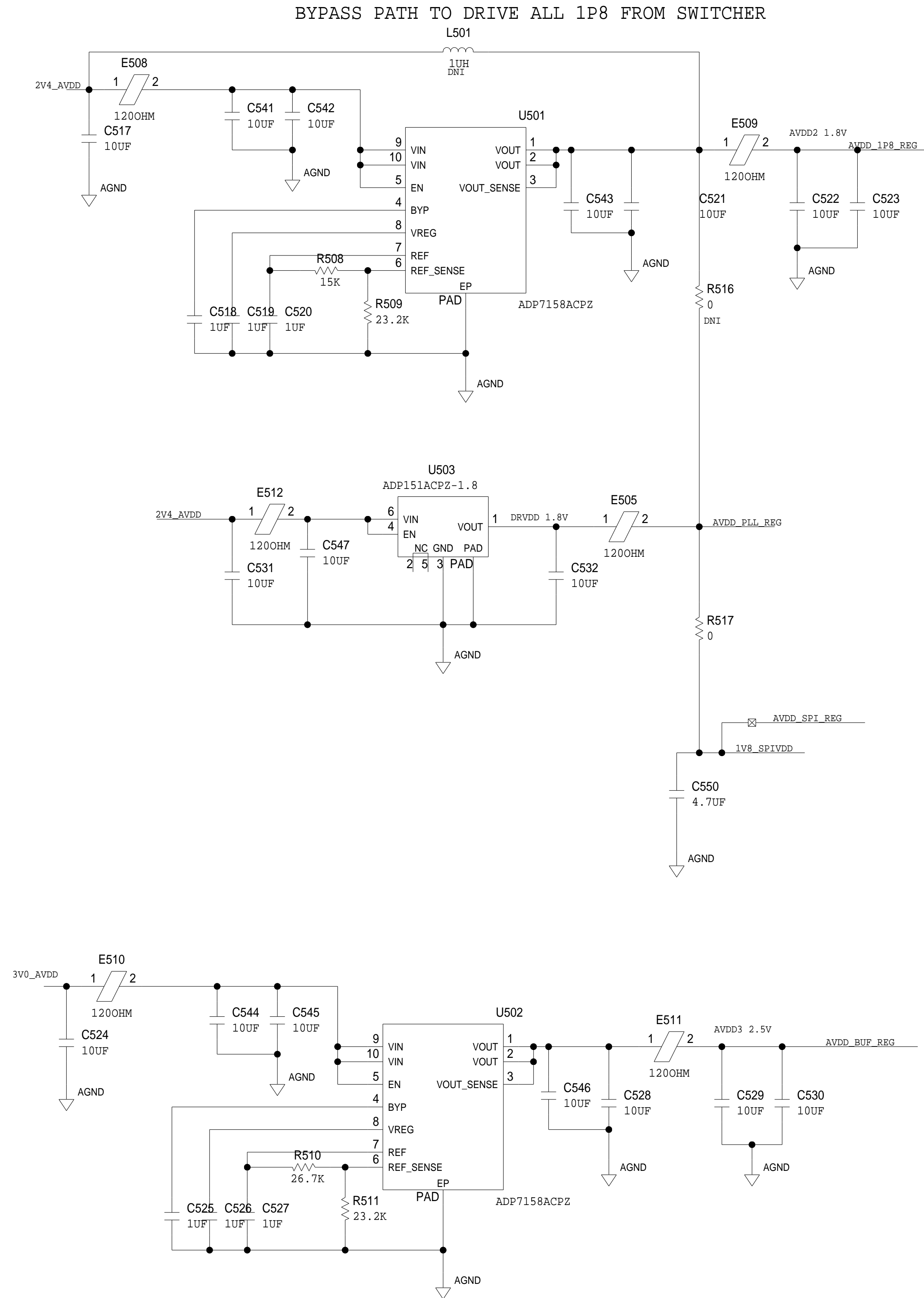
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SHEET 4 OF 8



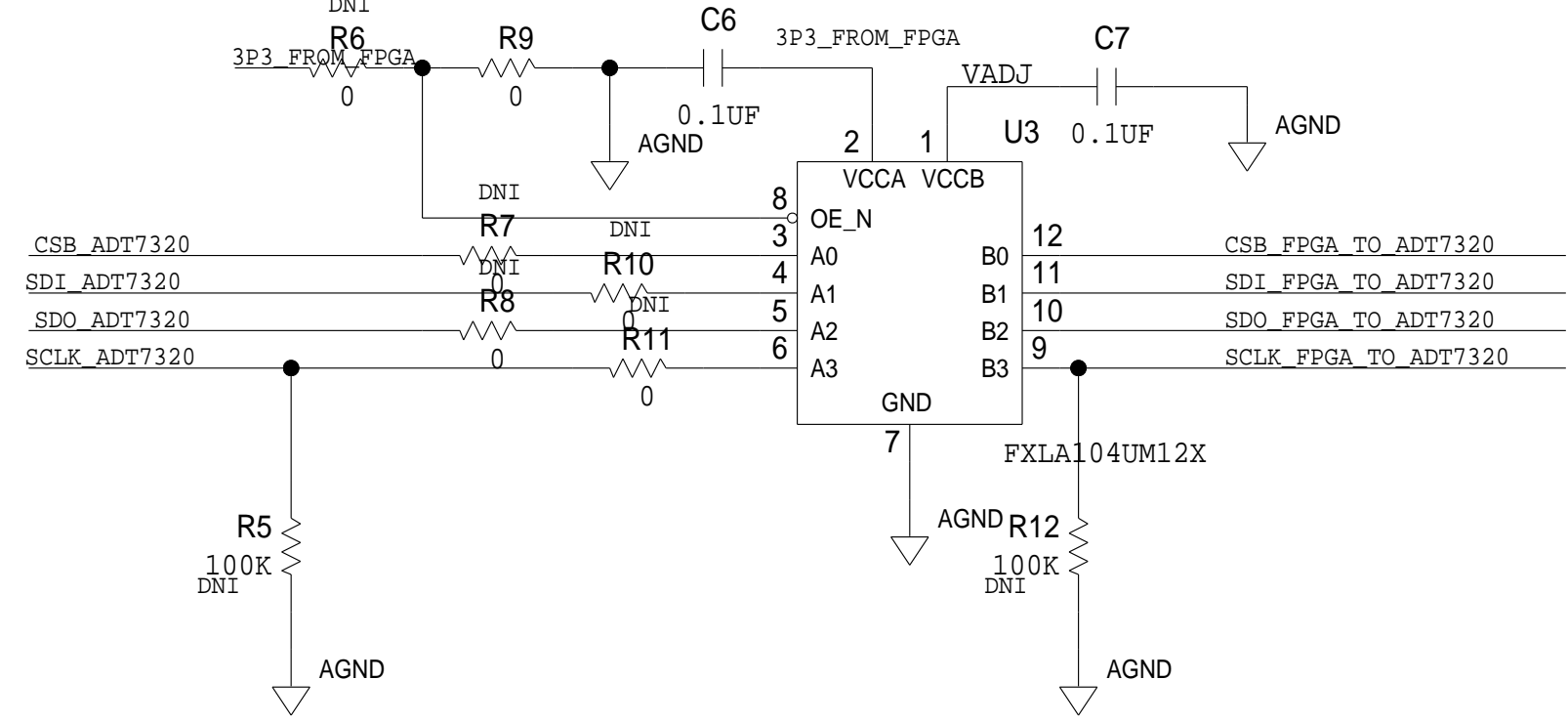
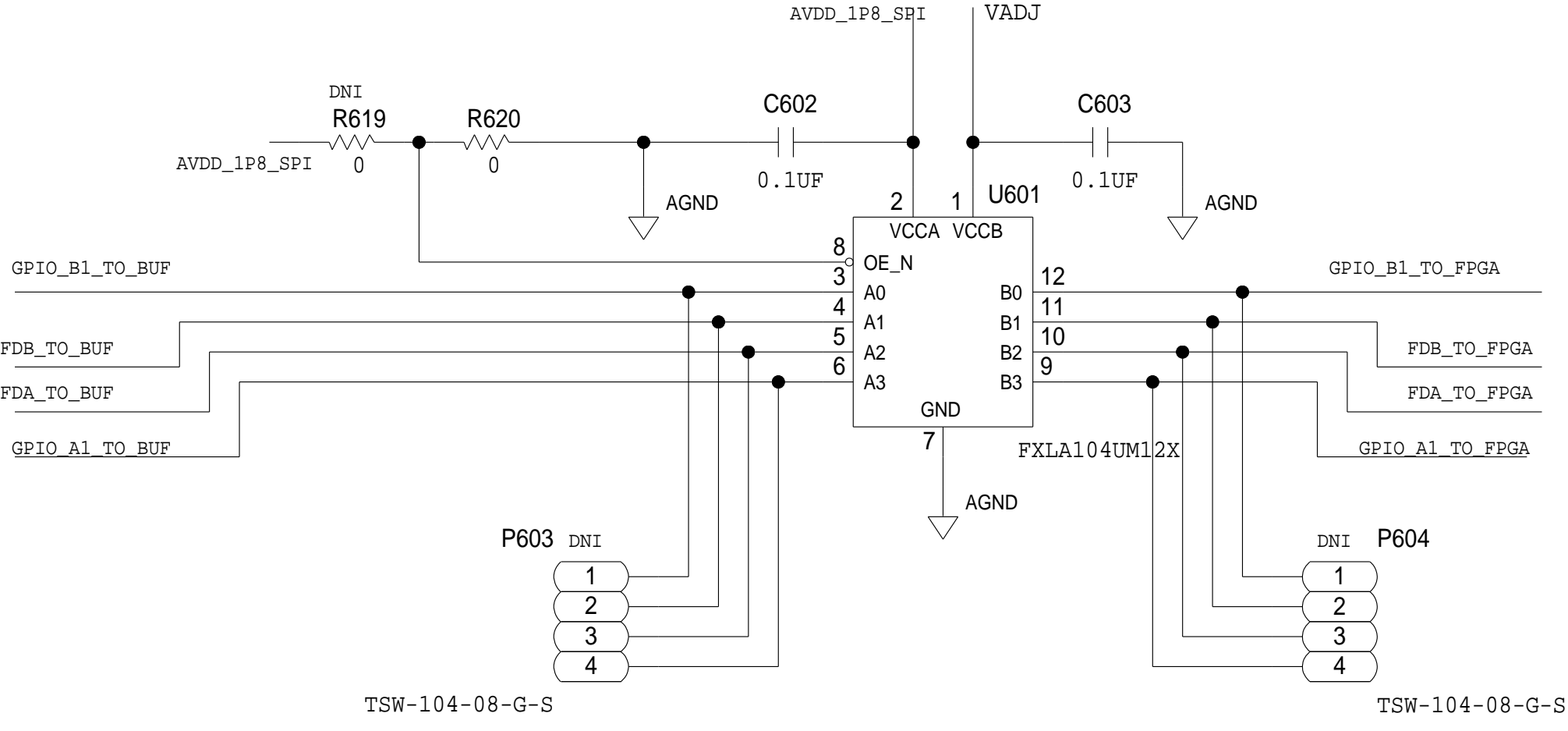
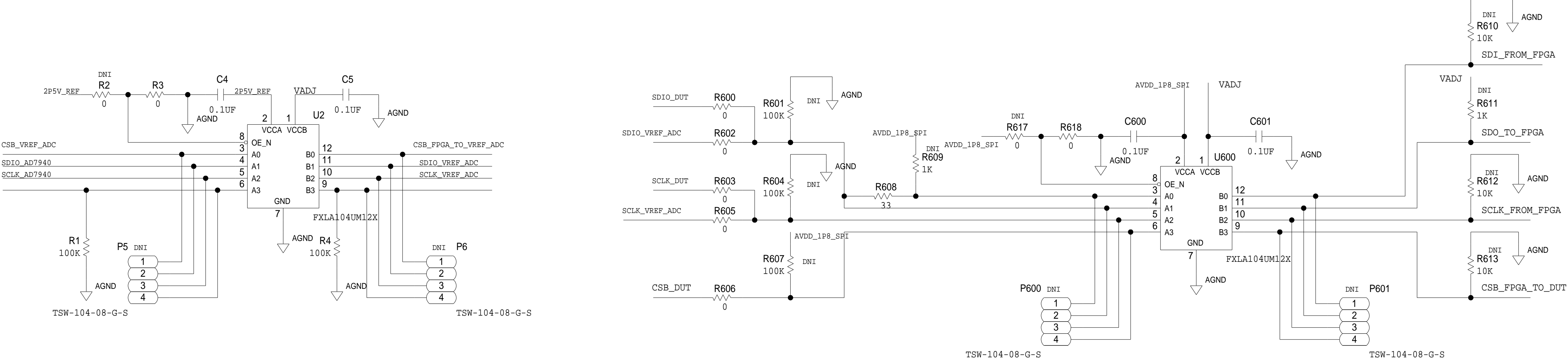
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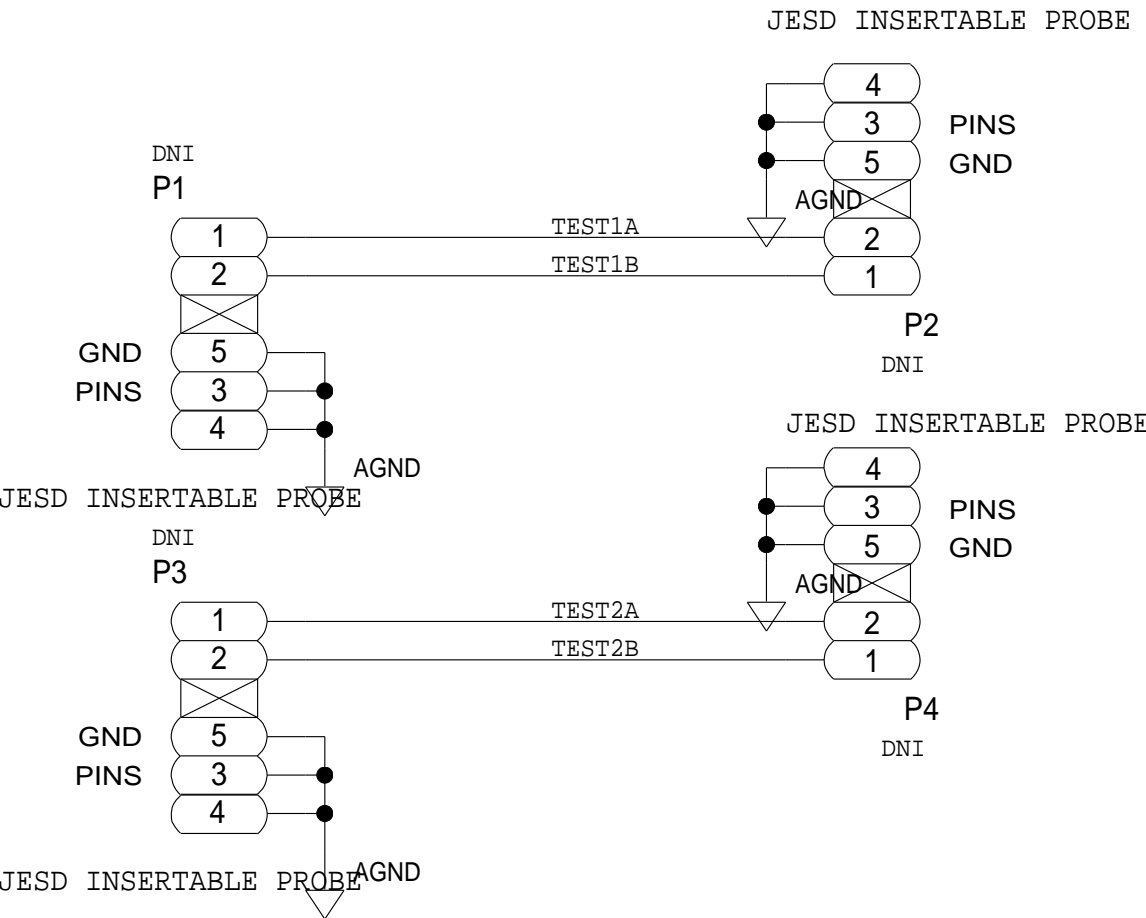
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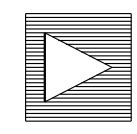
AD9689 SPI/BUFFER CIRCUIT

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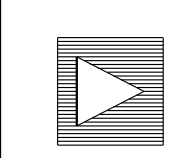
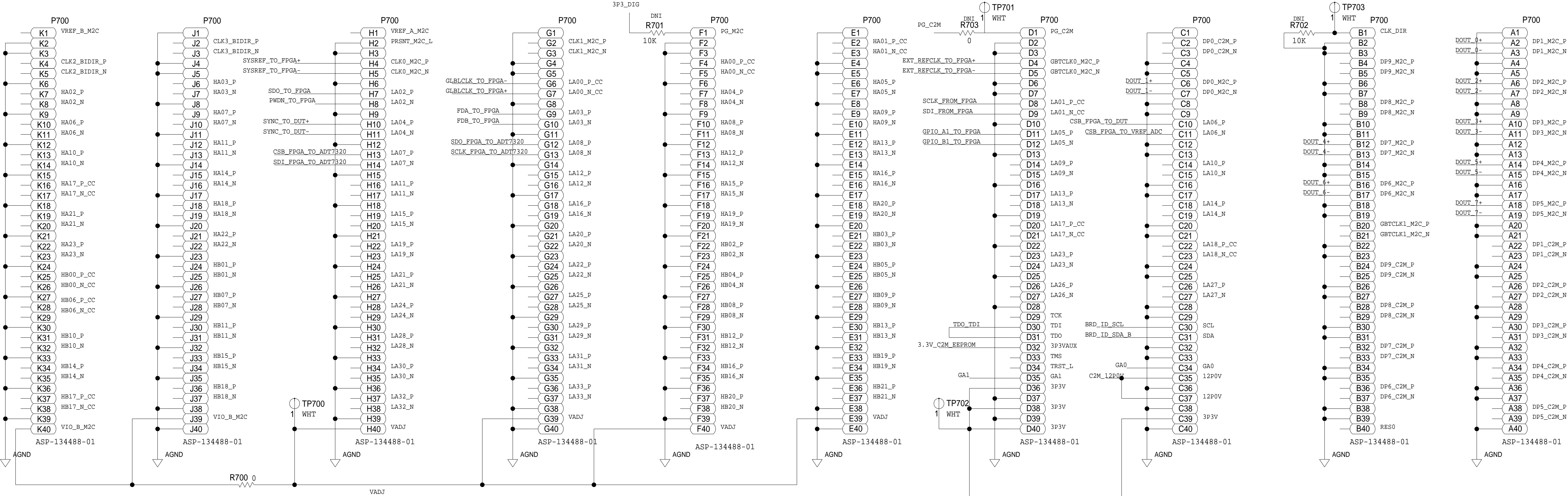
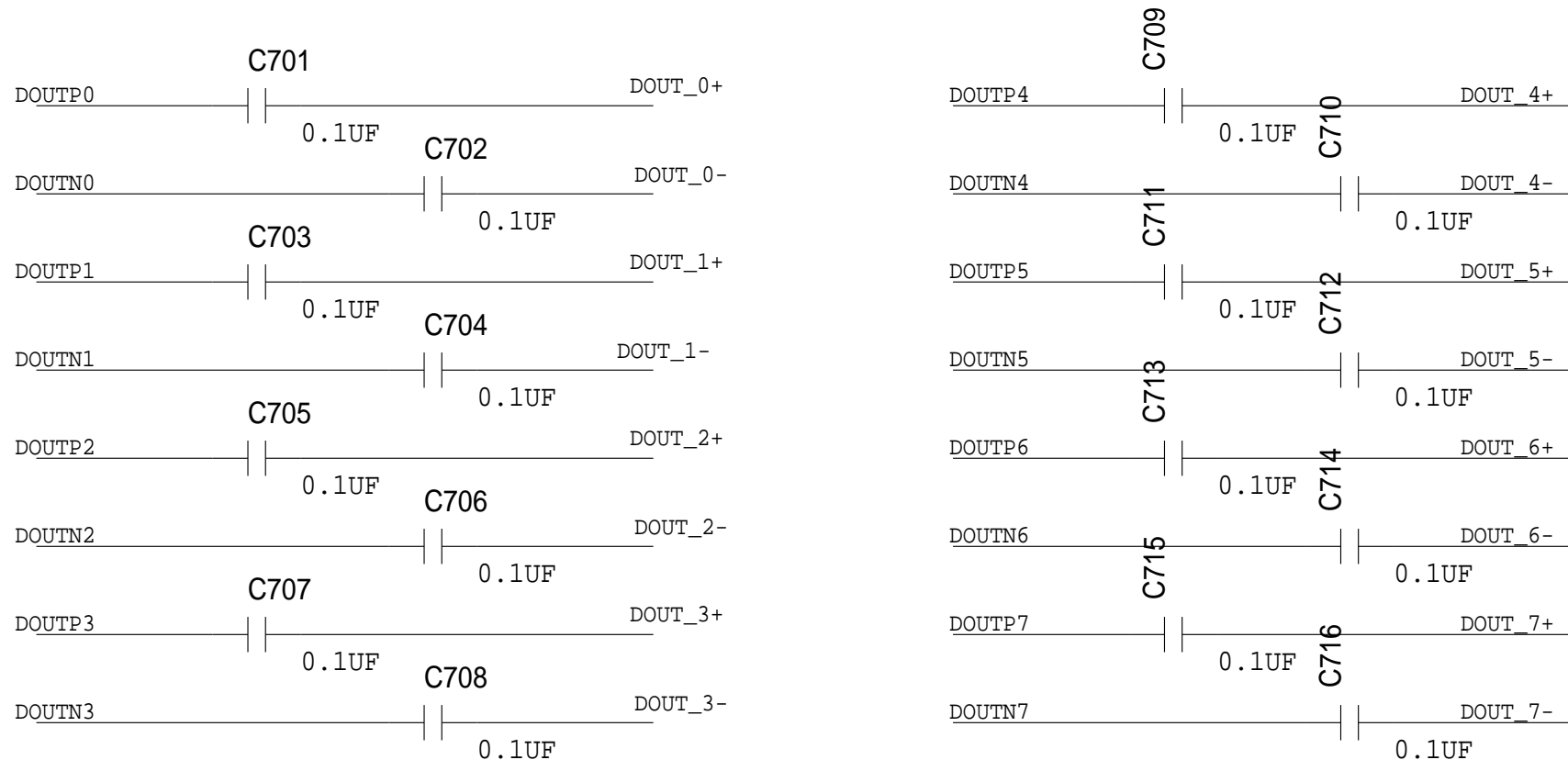
TEST TRACES



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AD9689 FMC CONNECTIONS

PLACE AS CLOSE TO DUT AS POSSIBLE



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