ADAR1000 Silicon Errata

Preliminary V0; 26 June 2020

Note on Chip Addressing

For problems #1 and #2 below: Using the ADDR1 and ADDR0 pins to set the hardware address of each individual chip, the user can connect the SCLK, CSB, SDIO, and SDO lines of up to four chips together. The ADDR1 and ADDR0 values correspond to the Bits[14:13] of the SPI address header (shown in Table 11 in the datasheet), respectively. The SPI problems below use the following:

Chip Index	Address Bits[14:13]	ADDR1 Pin	ADDR0 Pin
Chip 0	0b00	Low	Low
Chip 1	0b01	Low	High
Chip 2	0b10	High	Low
Chip 3	0b11	High	High

SPI Problems

1) **Unintentional Write All (broadcast) Command** to all Chips (0, 1,2,3) on SPI bus (see Chip Addressing section in datasheet for more information) when Writing to Chip 0, Reg 0x00
    a. Problem Description: When writing to the Register 0x00 of Chip 0, an unintentional Write All command is also done to Register 0x00 to Chips 1, 2, and 3. Thus any data that was intended for Chip 0 only, is also written to Reg 0x00 of Chips 1, 2, and 3. Note this problem is only when writing to Reg 0x00; this problem does not manifest itself with other registers.
    b. Example of Problem(s):

Soft Reset:

Command Type	**16-bit Address Payload**	**8-bit MOSI Data Payload**	**8-bit MISO Data Payload**	**Comments**
Write	0x0000	0x81	n/a	Intent: soft reset for Chip 0; Actuality: All chips on bus were reset.

Tri-State Example:

Command Type	**16-bit Address Payload**	**8-bit MOSI Data Payload**	**8-bit MISO Data Payload**	**Comments**
Write	0x0000	0x18	n/a	Intent: activate only Chip 0 SDO; Actuality: All Chips' SDO pins on SPI bus were activated

    c. Problem Workaround: After writing to Chip 0, Reg 0x00, individually write to the remaining Chips on the SPI bus - Chips 1, 2 and/or 3 - the desired data to be in their respective Register 0x00; applies to LSB first, Address Ascension and SDO activate; **does not apply to soft reset, see below.**

d. Examples of Workaround:

Soft Reset Example:

Do not perform a soft reset to Chip 0 unless you want all chips on the SPI bus to be reset. There is no way to ONLY reset Chip 0 while multiple Chips share a SPI bus.

SDO Activate Example:

Command Type	16-bit Address Payload	8-bit MOSI Data Payload	8-bit MISO Data Payload	Comments
Write	0x0000	0x18	n/a	Chip 0 SDO active; but also Chips 1, 2 and 3 SDO active
Write	0x2000	0x00	n/a	SDO de-activate on Chip 1
Write	0x4000	0x00	n/a	SDO de-activate on Chip 2
Write	0x6000	0x00	n/a	SDO de-activate on Chip 3

2) **SDO Tri-State Problem**: Readback problem when 2 or more chips on are on the same SPI bus

a. Problem Description:

i. **4-wire SPI Protocol**: when SDO is active (Reg 0x00, Bits[4:3] = 0b11), when a readback is initiated to any part on the SPI bus, the chips with SDO pins that are active & not addressed DO NOT go tri-state during the readback, but rather stay in a low state during the read back. This causes the SDO buffers that are on the MISO line to fight each other and prevent the addressed chip to readback properly.

ii. **3-wire SPI Protocol** (less common): when SDO is inactive (Reg 0x00, Bits[4:3] = 0b00), when a readback is initiated to any part on the SPI bus, the chips with SDO pins that are inactive & not addressed, their SDIO pins DO NOT go tri-state during the readback, but rather stay in a low state during the read back. This causes the SDIO buffers that are on the shared line to fight each other and prevent the addressed chip to readback properly.

b. Examples of Problem:

Chips 1, 2 and 3 on SPI bus; Chip 0 not on SPI bus (4-wire SPI Protocol)

Command Type	16-bit Address Payload	8-bit MOSI Data Payload	8-bit MISO Data Payload	Comments
Write	0x2000	0x18	n/a	Activate SDO pin of Chip 1
Write	0x4000	0x18	n/a	Activate SDO pin of Chip 2
Write	0x400A	0xAA	n/a	Write 0xAA to Chip 2 Scratchpad register
Write	0x6000	0x18	n/a	Activate SDO pin of Chip 3
Read	0xC00A	n/a	Data Corrupted	Attempted Chip 2 readback from Scratchpad register cannot be accomplished because both Chip 1 and Chip 3's SDO pin is pulling the MISO line low

Chips 0, 1, 2, and 3 on SPI bus (4-wire SPI Protocol)

Command Type	**16-bit Address Payload**	**8-bit MOSI Data Payload**	**8-bit MISO Data Payload**	**Comments**
Write	0x0000	0x18	n/a	Activate SDO pin of Chip 0; also actives SDO pin on Chips 1, 2, and 3 (see **Unintentional Write All command** above)
Write	0x2000	0x18	n/a	Activate SDO pin of Chip 1; redundant write*
Write	0x4000	0x18	n/a	Activate SDO pin of Chip 2; redundant write*
Write	0x400A	0xAA	n/a	Write 0xAA to Chip 2 Scratchpad register
Write	0x6000	0x18	n/a	Activate SDO pin of Chip 3; redundant write*
Read	0xC00A	n/a	Data Corrupted	Attempted Chip 2 readback from Scratchpad register cannot be accomplished because Chip0, Chip 1 and Chip 3's SDO pin is pulling the MISO line low

*Included for illustration purposes. Also, the user should never rely on the **Unintentional Write All Command** bug to write to all chips' Reg 0x00; if a Write All to Reg 0x00 is required, the proper bit coding of Bits[14:11]= 0b0001 is highly recommended.

c. Problem Workaround:

i. **4-wire SPI Protocol**: Keep parts in 3-wire SPI mode by disabling the SDO pin (Reg 0x00, Bits[4:3] = 0b00). When wanting to readback from Chips 1, 2 or 3, Write to their respective Reg 0x00 and set Bits[4:3] = 0b11. When readback is finished, de-activate the Chip's SDO pin.

For a Chip 0 readback, after enabling its SDO pin and before a readback is done, 3 subsequent writes to Chips 1, 2 and 3 are required to disable their SDO pins. See **Unintentional Write All** problem above.

ii. **3-wire SPI Protocol**: Keep parts in 4-wire SPI mode by activating the SDO pins (Reg 0x00, Bits[4:3] = 0b11). When wanting to readback from Chips 1, 2, or 3, Write to their respective Reg 0x00 and set Bits[4:3] = 0b00. When readback is finished, active the Chip's SDO pin.

For a Chip 0 readback, after disabling its SDO pin and before a readback is done, 3 subsequent writes to Chips 1, 2 and 3 are required to enable their SDO pins. See **Unintentional Write All** problem above.

d. Example of Workaround: Want to Readback from Chip 2, when:

Chips 1, 2 and 3 on SPI bus; Chip 0 not on SPI bus (4-wire SPI Protocol)

Command Type	16-bit Address Payload	8-bit MOSI Data Payload	8-bit MISO Data Payload	Comments
Write	0x2000	0x18		Activate SDO pin of Chip 1
Write	0x4000	0x18		Activate SDO pin of Chip 2
Write	0x400A	0xAA		Write 0xAA to Chip 2 Scratchpad register

Write	0x6000	0x18		Activate SDO pin of Chip 3
Write	0x2000	0x00	n/a	De-activate SDO of Chip 1
Write	0x6000	0x00	n/a	De-activate SDO of Chip 3
Read	0xC00A	n/a	0xAA	Attempted Chip 2 readback from Scratchpad register successful
Write	0x4000	0x00	n/a	De-activate SDO of Chip 2 if no more readback required

Chips 0, 1, 2, and 3 are on SPI bus (4-wire SPI Protocol)

Command Type	**16-bit Address Payload**	**8-bit MOSI Data Payload**	**8-bit MISO Data Payload**	**Comments**
Write	0x0000	0x18	n/a	Activate SDO pin of Chip 0; also, actives SDO pin on Chips 1, 2, and 3 (see **Unintentional Write All command**)
Write	0x2000	0x18	n/a	Activate SDO pin of Chip 1; redundant write*
Write	0x4000	0x18	n/a	Activate SDO pin of Chip 2; redundant write*
Write	0x400A	0xAA	n/a	Write 0xAA to Chip 2 Scratchpad register
Write	0x6000	0x18	n/a	Activate SDO pin of Chip 3; redundant write*
Write	0x0000	0x00	n/a	De-activate SDO of Chip 0;
Write	0x2000	0x00	n/a	De-activate SDO of Chip 1; redundant*
Write	0x6000	0x00	n/a	De-activate SDO of Chip 3; redundant*
Write	0x4000	0x18	n/a	Re-activate SDO of Chip 2 since de-activating Chip 0's SDO, de-activated all Chips' SDO
Read	0xC00A	n/a	0xAA	Attempted Chip 2 readback from Scratchpad register successful
Write	0x4000	0x00	n/a	De-activate SDO of Chip 2 if no more readback required

*Included for illustration purposes. Also, the user should never rely on the **Unintentional Write All Command** bug to write to all chips' Reg 0x00; if a Write All to Reg 0x00 is required, the proper bit coding of Bits[14:11]= 0b0001 is highly recommended.