The following is an errata & clarity list for the ADAR1000 Revision A datasheet. These corrections and additions will be integrated into the Revision B datasheet.

1) RAM is undefined upon a power cycle; it needs to be re-written on every power cycle. However, upon a soft reset (Reg. 0x00) data stored in RAM is unaffected.

2) To fetch a beam position from memory, for all 4 Tx/Rx channels at once, perform the following steps:

   - Set BEAM_RAM_BYPASS low in Reg 0x038
   - Perform a) or b), but not both:
     a) **For loading all 4 Tx/Rx channels at once**:

     Write the desired 7-bit beam position (0 through 120) into register 0x039 (receive) or 0x03A (transmit) and assert the fetch bit high (bit 7)

     b) **For loading specific beam positions to individual channels**:
     In Register 0x38 assert TX_CHX_RAM_BYPASS for Tx channels and/or RX_CHX_RAM_BYPASS for Rx channels, then write to the desired 7-bit beam position into registers 0x3D to 0x40 for the Rx channels and 0x41 to 0x44 and assert the fetch bit high in each register.
   - Provide at least 6 additional clock cycles on SCLK to load the new data from RAM
   - Pulse the TX_LOAD/RX_LOAD pin or LDTX_OVERRIDE/LDRX_OVERRIDE bit for the new data to take effect

3) To fetch a bias setting from memory, perform the following steps:

   - Set BIAS_RAM_BYPASS low in Reg 0x038
   - Write the desired 3-bit bias setting (0 through 6 maps to bias settings 1 through 7) into register 0x051 (receive) or 0x052 (transmit) and assert the fetch bit high (bit 3)
   - Provide at least 6 additional clock cycles on SCLK to load the new data from RAM

4) To step sequentially through the beam positions stored in memory, perform the following steps:

   - Load Register 0x04D through Register 0x04E with the desired 7-bit transmit channel start and stop beam position indices
   - Load Register 0x04F through Register 0x050 with the desired 7-bit receive channel start and stop beam position indices
   - Assert high TX_BEAM_STEP_EN & RX_BEAM_STEP_EN in Reg 0x038
   - Provide at least 6 additional clock cycles on SCLK to load the starting beam position from RAM

- Pulse the TX_LOAD/RX_LOAD pin or LDTX_OVERRIDE/LDRX_OVERRIDE bit for the starting beam position to take effect
- Repeat the last 2 steps for the next sequential beam position to take effect

After the stop-beam position has been loaded, the sequence will return to the start beam position and repeat.

5) "Scan_MODE_EN" in Reg 0x38 is Reserved. Keep Bit[7] low.

6) Table 17 error with SW_DRV_TR_MODE_SEL bit polarity in Reg 0x30.

TR_SW_POS & TR_SW_NEG outputs' positions are swapped relative to Table 17 in Revision A datasheet. Revision B will have the following corrections highlighted in yellow:

Table 17. Controlling TR_SW_POS and TR_SW_NEG Output

SW_DRV_EN_TR (Register 0x031, Bit 4)	TR_SOURCE (Register 0x031, Bit 2)[1]	TR (Chip Input)[1]	TR_SPI (Register 0x031, Bit 1)[1]	SW_DRV_TR_MODE_SEL (Register 0x030, Bit 7)[1]	Device Transmit or Receive State[1]	SW_DRV_TR_STATE (Register 0x031, Bit 7)[1]	TR_SW_POS (Chip Output)	TR_SW_NEG (Chip Output)
0	X	X	X	X	X	X	Floating	Floating
1	0	X	0	0	Receive	0	0 V	Floating
1	0	X	0	0	Receive	1	3.3 V	Floating
1	0	X	1	0	Transmit	0	3.3 V	Floating
1	0	X	1	0	Transmit	1	0 V	Floating
1	1	0	X	0	Receive	0	0V	Floating
1	1	0	X	0	Receive	1	3.3V	Floating
1	1	1	X	0	Transmit	0	3.3V	Floating
1	1	1	X	0	Transmit	1	0V	Floating
1	0	X	0	1	Receive	0	Floating	0 V
1	0	X	0	1	Receive	1	Floating	–5 V
1	0	X	1	1	Transmit	0	Floating	–5 V
1	0	X	1	1	Transmit	1	Floating	0 V
1	1	0	X	1	Receive	0	Floating	0 V
1	1	0	X	1	Receive	1	Floating	–5 V
1	1	1	X	1	Transmit	0	Floating	–5 V
1	1	1	X	1	Transmit	1	Floating	0 V

[1] X means don't care.

7) Table 20 errors:

a. Change Register 0x401 write data to 0x02

b. Tx Vector Modulator I & Q vector addresses for channels 2, 3 and 4 are incorrect. Corrections highlighted in yellow. Table 20 (partial) should read:

0x01C	FF	Set Channel 1 attenuator to 0 dB, VGA gain to maximum.
0x020	36	Set Channel 1 vector modulator I input to positive, Magnitude 16.
0x021	35	Set Channel 1 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°
0x01D	FF	Set Channel 2 attenuator to 0 dB, VGA gain to maximum.
0x022	36	Set Channel 2 vector modulator I input to positive, Magnitude 16.
0x 023	35	Set Channel 2 vector modulator Q input to positive, magnitude 15; these two together set phase to 45°.
0x 01E	FF	Set Channel 3 attenuator to 0 dB, VGA gain to maximum.
0x 024	36	Set Channel 3 vector modulator I input to positive, Magnitude 16.
0x 025	35	Set Channel 3 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°.
0x 01F	FF	Set Channel 4 attenuator to 0 dB, VGA gain to maximum.
0x 026	36	Set Channel 4 vector modulator I input to positive, Magnitude 16.
0x 027	35	Set Channel 4 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°.

8) Pin description change for B3, PA_ON pin, to read:

PA Enable Input. Used when device Transmit/Receive control is via the TR Pin; not used with SPI control. While BIAS_CTRL (Bit 6 in Reg 0x30) = 1 & TR_SOURCE (Bit 2 in Reg 0x31) = 1, set this pin to logic high for PA bias voltage outputs to assume the values set by the EXT_PAx_BIAS_ON registers when TR (pin) = 1, and EXT_PAx_BIAS_OFF registers when TR (pin) = 0 (x = 1 to 4). All PA bias voltage outputs take on the corresponding EXT_PAx_BIAS_OFF register values if the PA_ON pin is at logic low. See Table 18. This pin is internally pulled up to the 1.8 V low dropout (LDO) regulator bias voltage with a 100 kO resistor.

9) Register 0x02, DEV_CONFIG, is non-functional for the ADAR1000.

10) ADAR1000 is fabricated on a SiGe BiCMOS process.

11) The Channel Gain Specification is 4 channel coherent gain with 6 dB removed from it. The table below relates the 3 gain specification:

Specification	**Gain (dB)**
Measure Gain	G
4-Channel Coherent Gain	G + 12
Channel Gain	G + 12 -6 -> G + 6

12) Memory Counter information:

c) The Tx and Rx have independent memory counters for beam position advance
d) The Tx beam position can be advanced while device is in Rx mode, and vice versa
e) Multiple beam advances can be performed on the Tx while device is in Rx mode, and vice versa,
f) The TX_LOAD and RX_LOAD pins can be tied together if the user wishes to advance the Tx and Rx memory counters together

13) Register 0x400 information: upper nibble is 2.8V LDO trim control, lower nibble is 1.8V LDO trim control. Trim slope is about 15 mV/LSB and 10 mV/LSB, respectively.

14) Tx equivalent circuit in Figure 82 should have a series AC coupling cap; Tx output ports Ohm out as an open.

15) Table 19 Error in last two rows of "LNA Bias Bits Used Column": EXT_LNA_BIAS_ON and EXT_LNA_BIAS_OFF should be swapped. Updated table shown below:

▪ Table 19. Control of LNA_BIAS Output

LNA_BIAS_OUT_EN (Register 0x030, Bit 4)	BIAS_CTRL (Register 0x030, Bit 6)	TR_SOURCE (Register 0x031, Bit 2)	RX_EN (Register 0x031, Bit 5)	TR (Input to Chip)	LNA Bias Bits Used
0	X	X[1]	X[1]	X[1]	Open circuit (floating)
1	0	0	0	X[1]	EXT_LNA_BIAS_ON
1	0	0	1	X[1]	EXT_LNA_BIAS_ON
1	1	0	0	X[1]	EXT_LNA_BIAS_OFF
1	1	0	1	X[1]	EXT_LNA_BIAS_ON
1	0	1	0	0	EXT_LNA_BIAS_ON
1	0	1	0	1	EXT_LNA_BIAS_ON
1	1	1	0	0	EXT_LNA_BIAS_ON
1	1	1	0	1	EXT_LNA_BIAS_OFF

X means don't care.

16) Table 11 error: There are only 121 beam positions in memory; if indexed from "0", last beam position should be "120"

17) Clarity on the Tx-to-Rx, and Rx-to-Tx programmable delay. The delays only work when using the TR pin & when SCLK applied. The programmed delay does not work when there is no SCLK applied or when using the TR_SPI bit.

18) ADC Mux select bits:

    0: Temp sensor

    1: Detector 1

    2: Detector 2

    3: Detector 3

    4: Detector 4