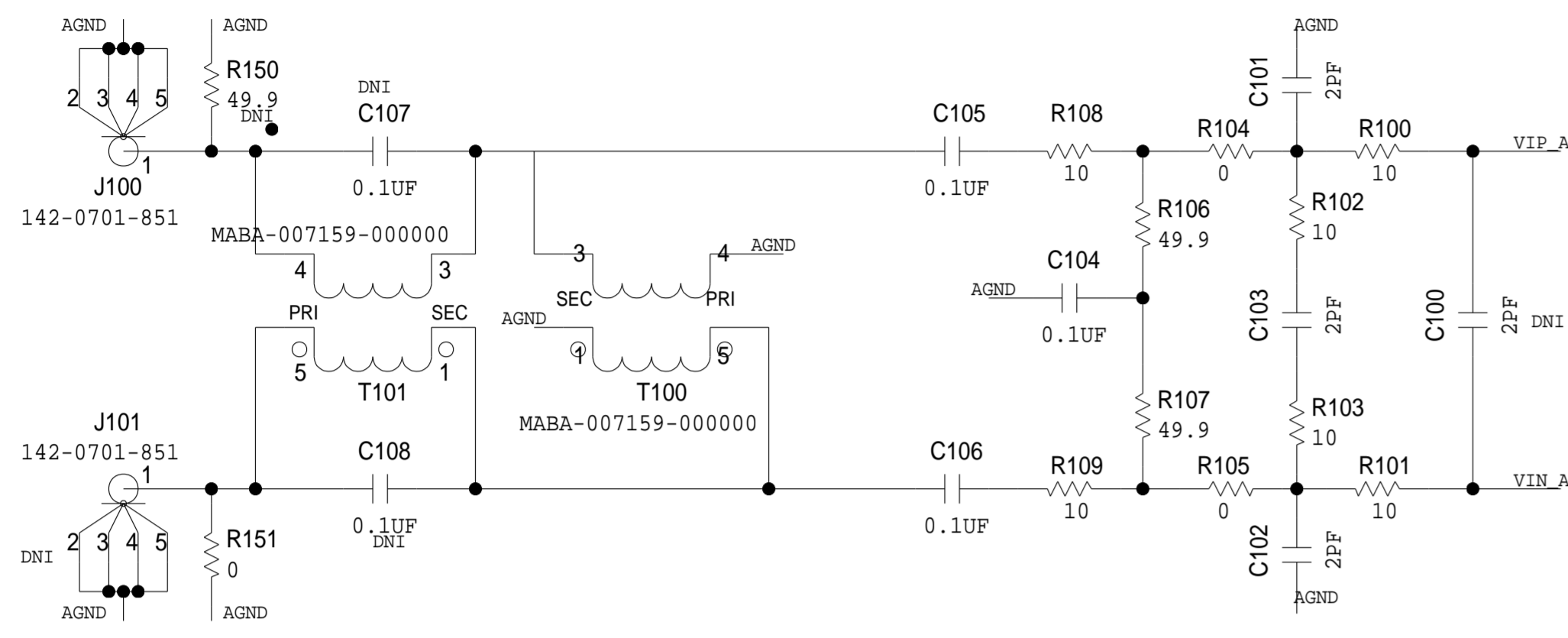


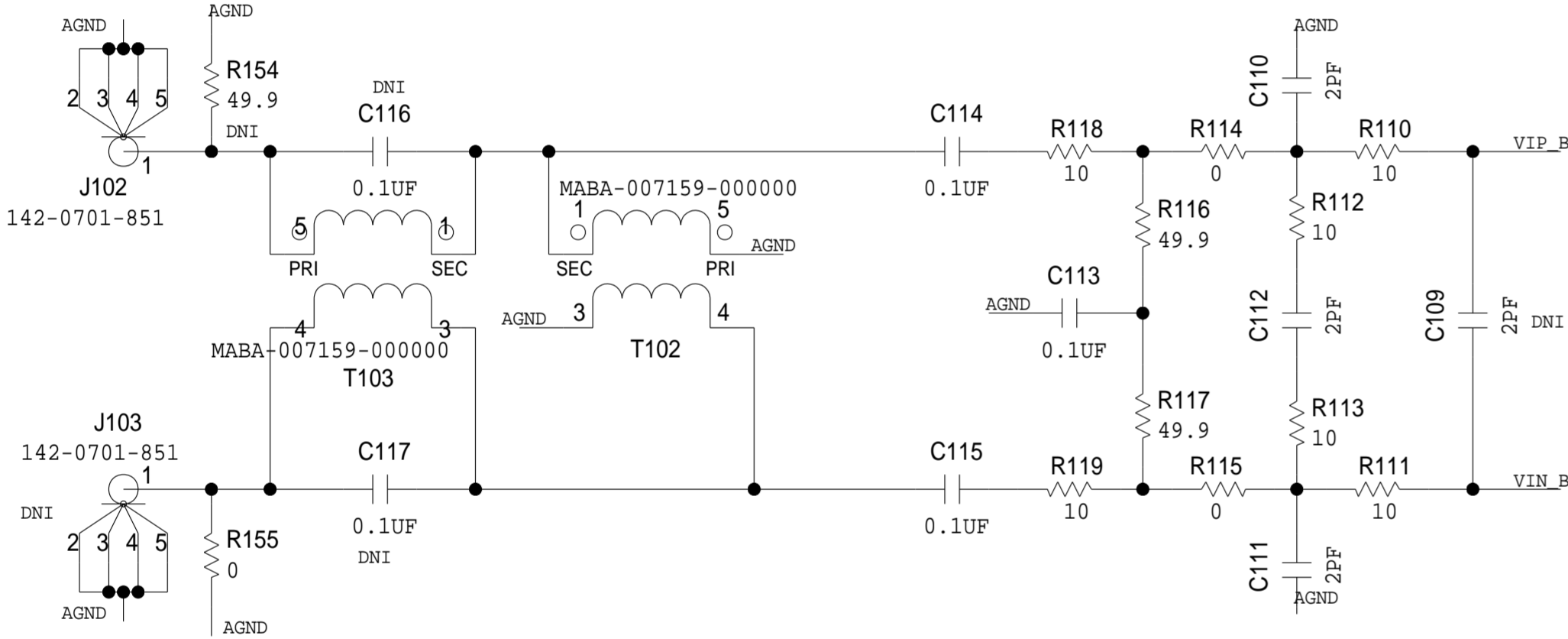
ANALOG INPUTS  
HIGH SFDR VARIANT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

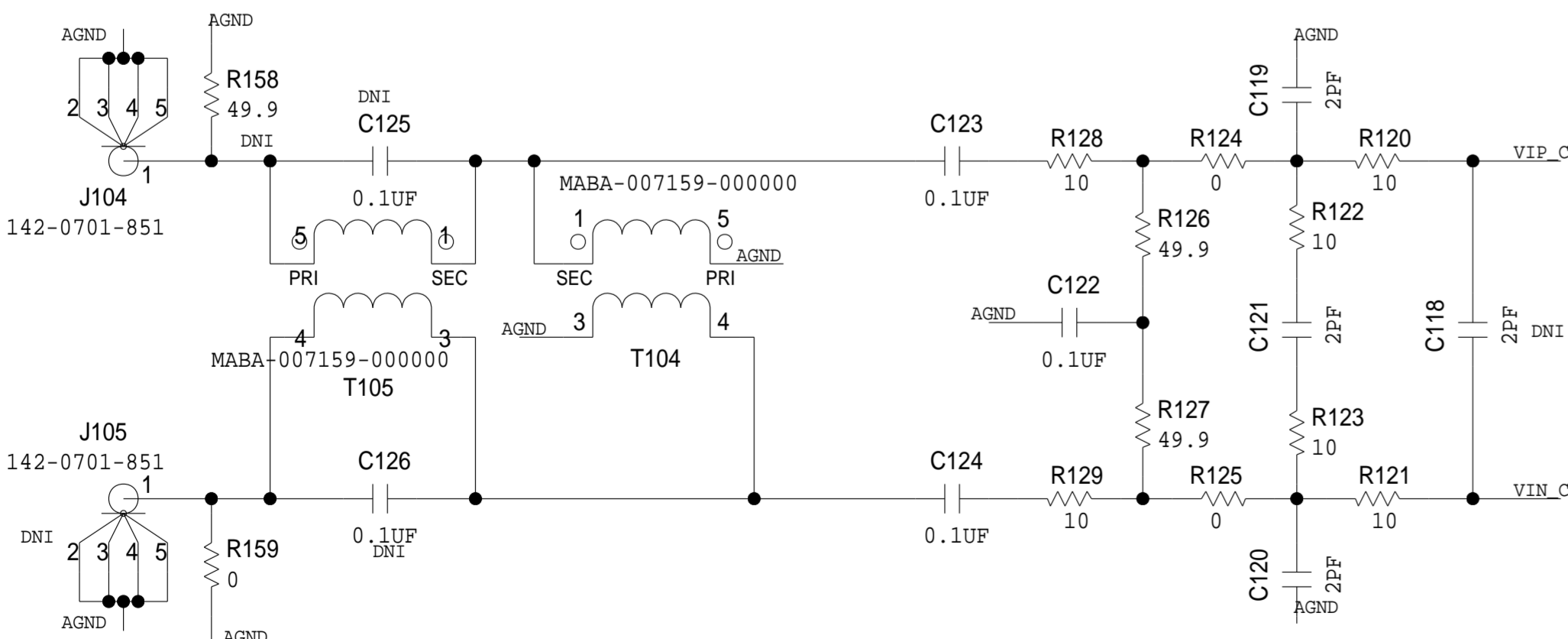
INPUT A



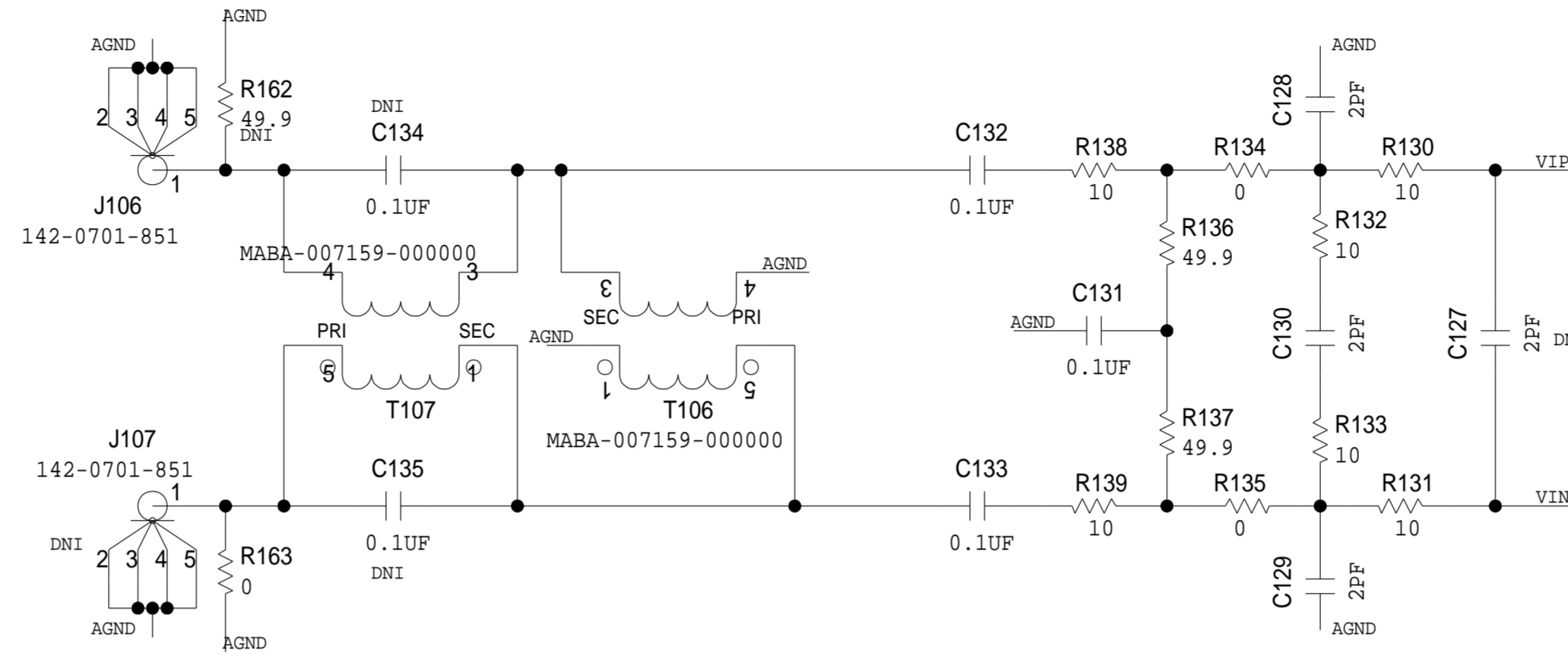
INPUT B



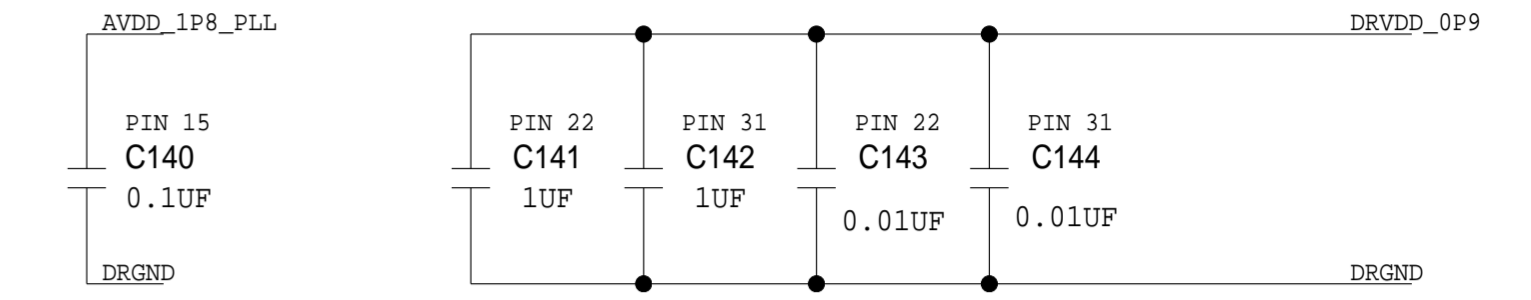
INPUT C



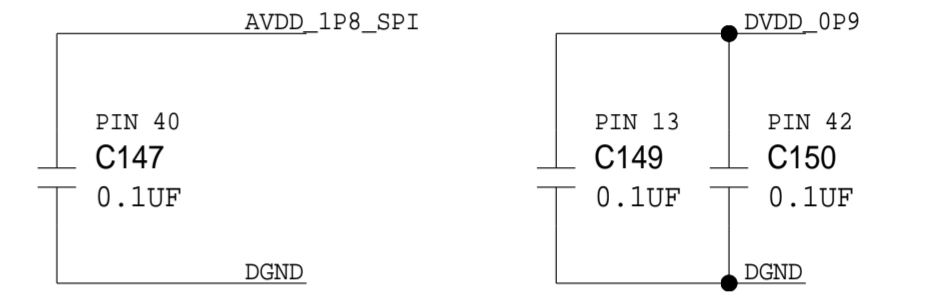
INPUT D



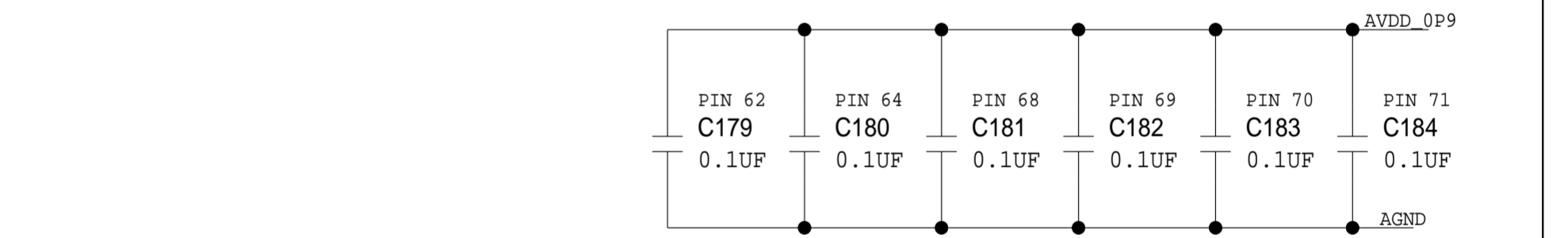
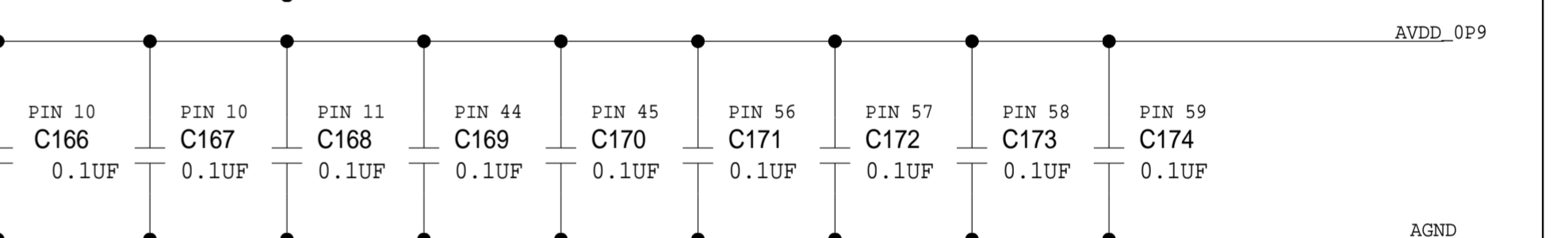
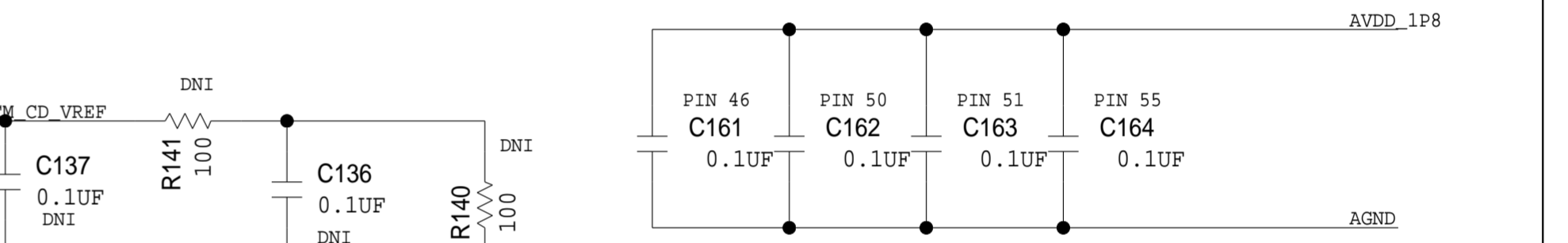
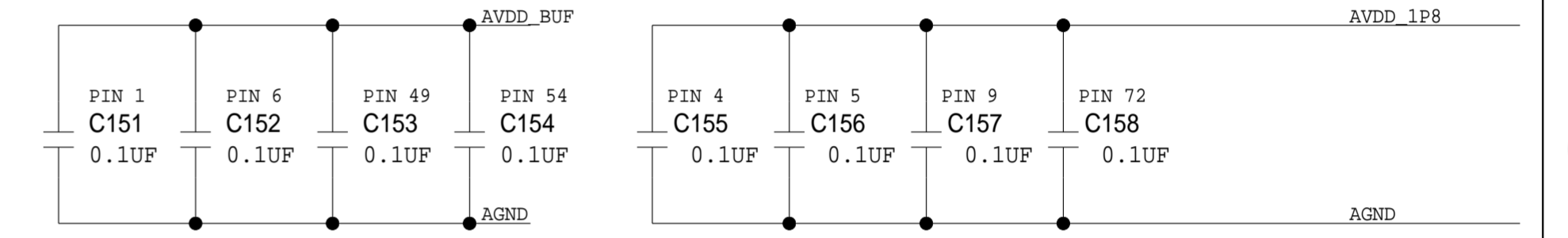
DRIVER DECOUPLING CAPACITORS



DIGITAL DECOUPLING CAPACITORS

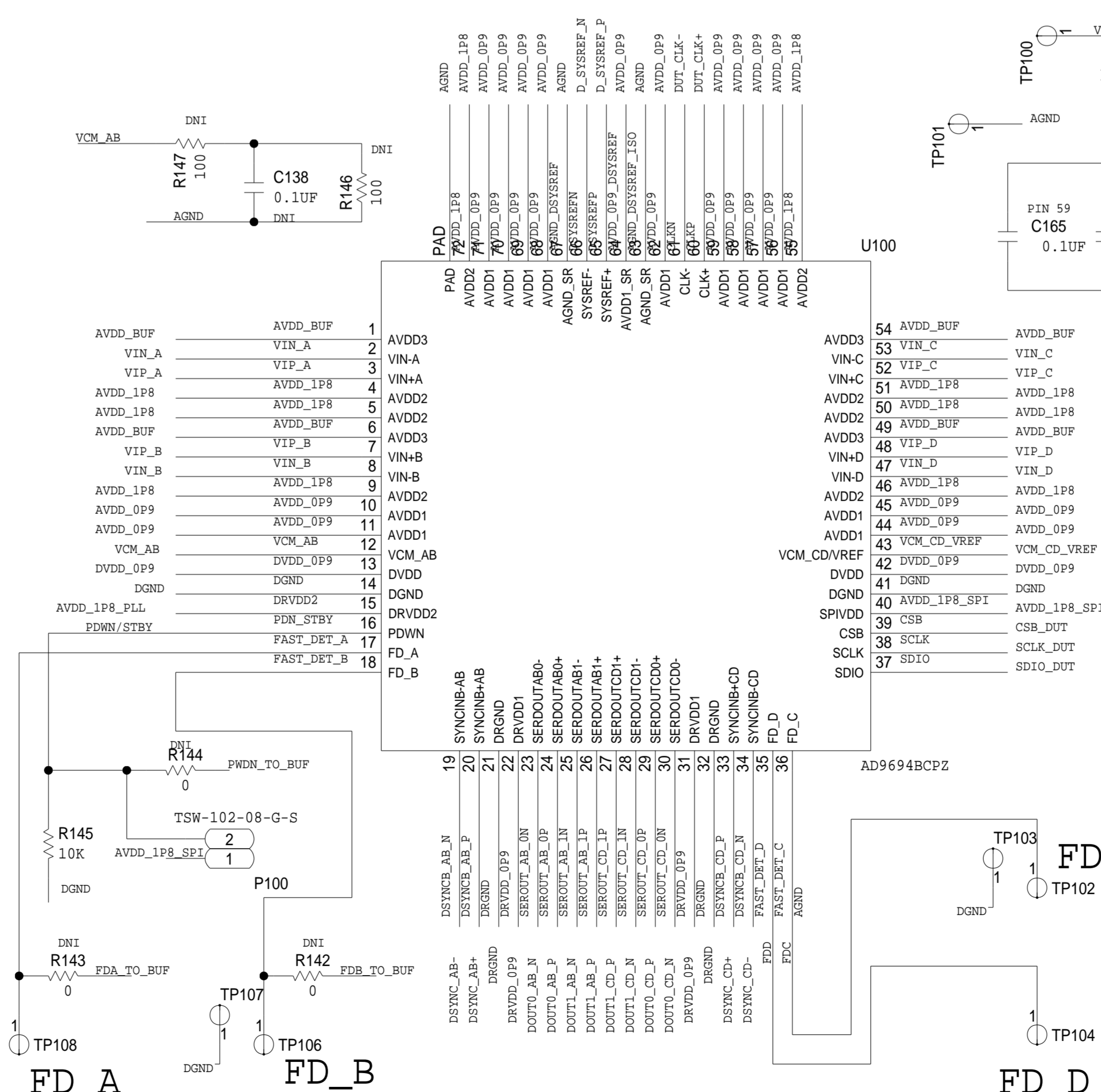


ANALOG DECOUPLING CAPACITORS



- DRVDD\_OP9\_SENSE <math>\rightarrow</math> DRVDD\_OP9
- DRVDD\_OP9\_SENSE <math>\rightarrow</math> DRGND
- DVDD\_OP9\_SENSE <math>\rightarrow</math> DVDD\_OP9
- DGND\_OP9\_SENSE <math>\rightarrow</math> DGND
- AVDD\_OP9\_SENSE <math>\rightarrow</math> AVDD\_OP9
- AGND\_OP9\_SENSE <math>\rightarrow</math> AGND
- AVDD\_IP8\_SENSE <math>\rightarrow</math> AVDD\_IP8
- AGND\_IP8\_SENSE <math>\rightarrow</math> AGND
- AVDD\_BUF\_SENSE <math>\rightarrow</math> AVDD\_BUF
- AGND\_BUF\_SENSE <math>\rightarrow</math> AGND
- AVDD\_IP8\_PLL\_SENSE <math>\rightarrow</math> AVDD\_IP8\_PLL
- DRGND\_IP8\_PLL\_SENSE <math>\rightarrow</math> DRGND
- AVDD\_IP8\_SPI\_SENSE <math>\rightarrow</math> AVDD\_IP8\_SPI
- DGND\_IP8\_SPI\_SENSE <math>\rightarrow</math> DGND

AD9694 DUT



PLACE 10 OHM SERIES R. CLOSE TO DIFF. C. AND CLOSE TO DUT

PLACE 10 OHM SERIES R. CLOSE TO DIFF. C. AND CLOSE TO DUT

PLACE 10 OHM SERIES R. CLOSE TO DIFF. C. AND CLOSE TO DUT

PLACE 10 OHM SERIES R. CLOSE TO DIFF. C. AND CLOSE TO DUT

PLACE 10 OHM SERIES R. CLOSE TO DIFF. C. AND CLOSE TO DUT

PLACE 10 OHM SERIES R. CLOSE TO DIFF. C. AND CLOSE TO DUT

PLACE 10 OHM SERIES R. CLOSE TO DIFF. C. AND CLOSE TO DUT

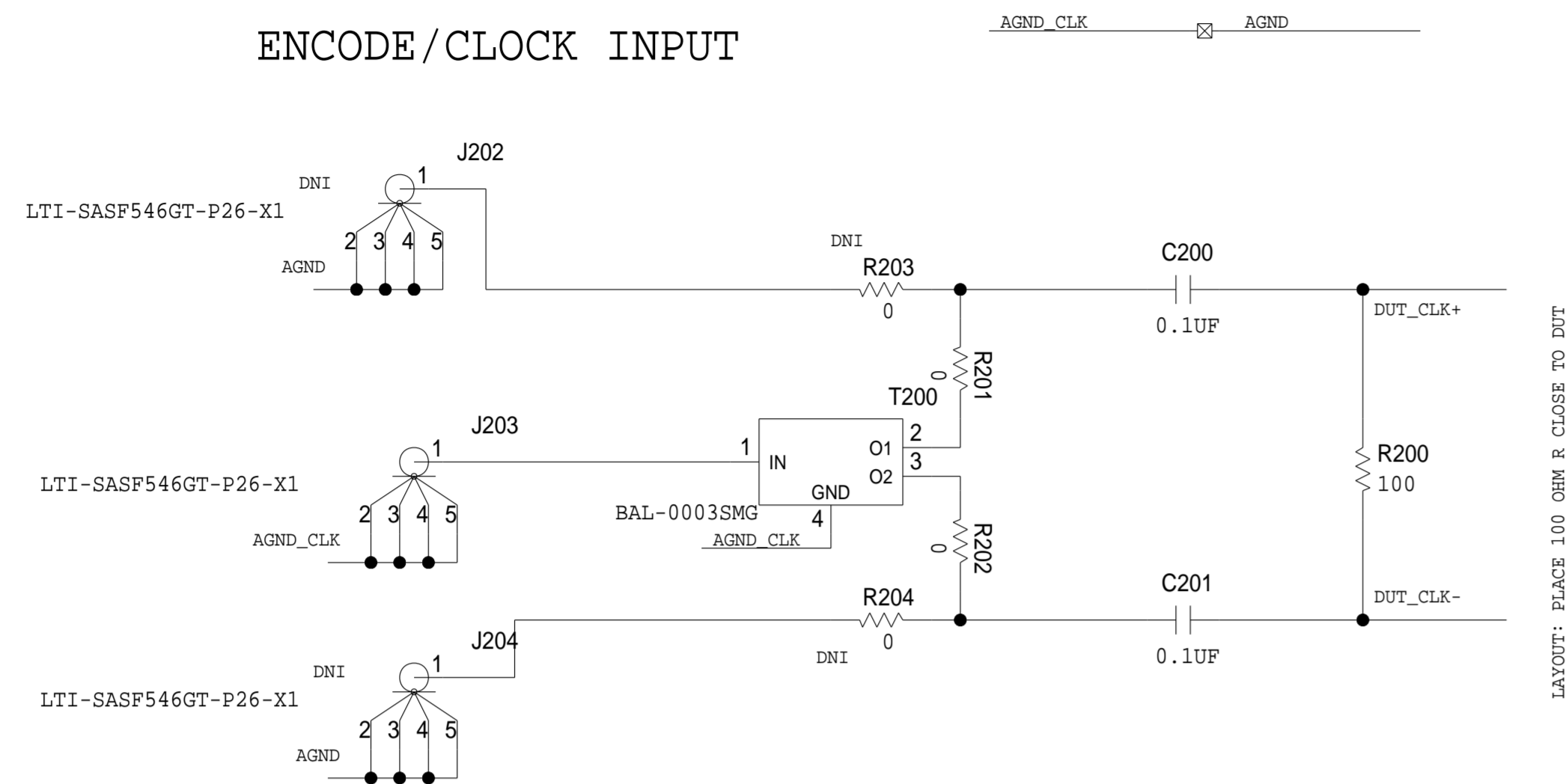
SCHEMATIC			
CUSTOMER EVALUATION BOARD 9694 AD9694			
DESIGN VIEW -	DRAWING NO. 9694CE01	REV A	
PTD ENGINEER J. HARRIS	SIZE D	SCALE NONE	SHEET 1 OF 7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

# AD9694 CLOCK INPUTS

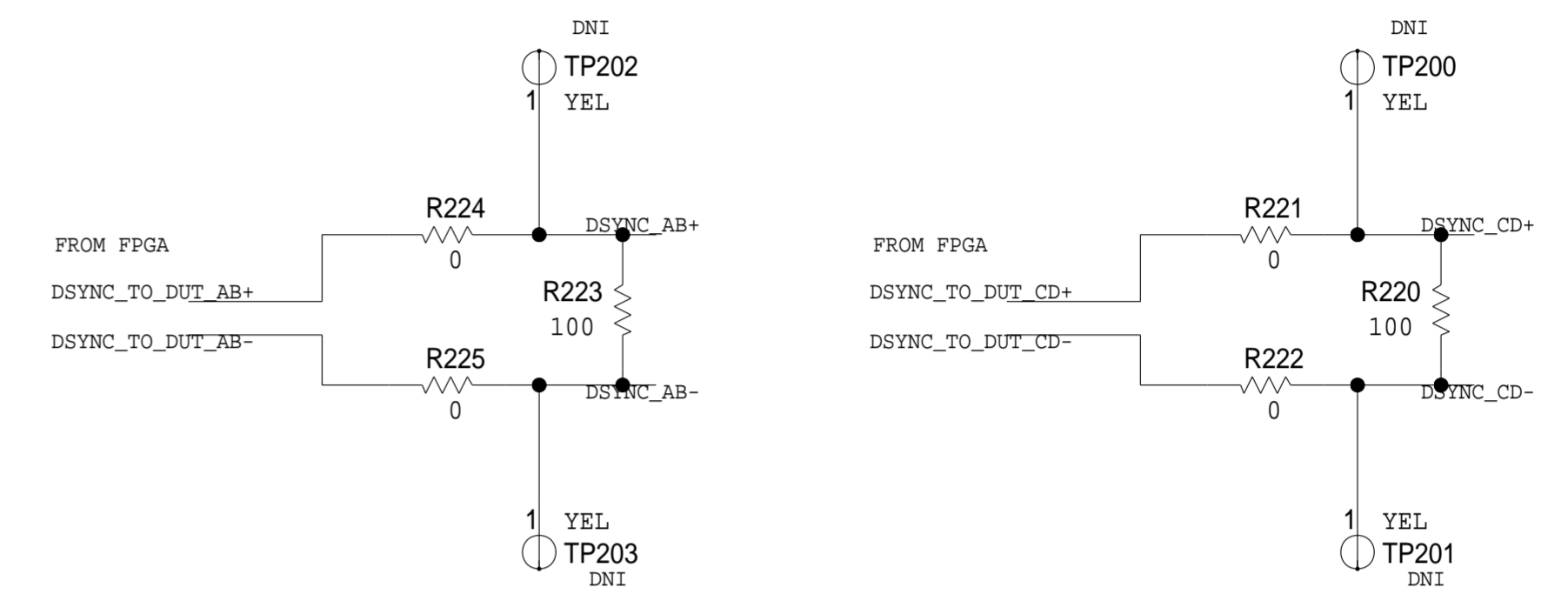
PLACE ON BOTTOM OF BOARD

## ENCODE/CLOCK INPUT

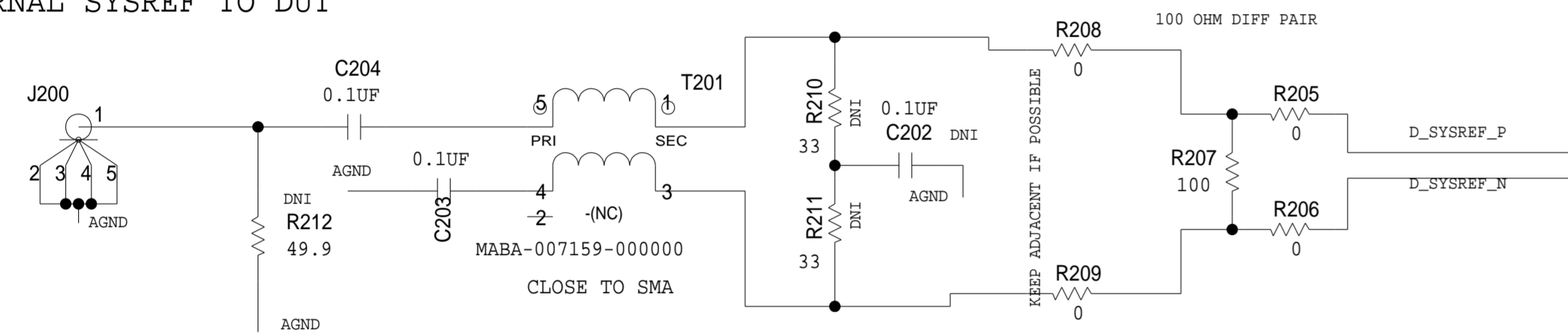


LAYOUT: PLACE 100 OHM R CLOSE TO DUT

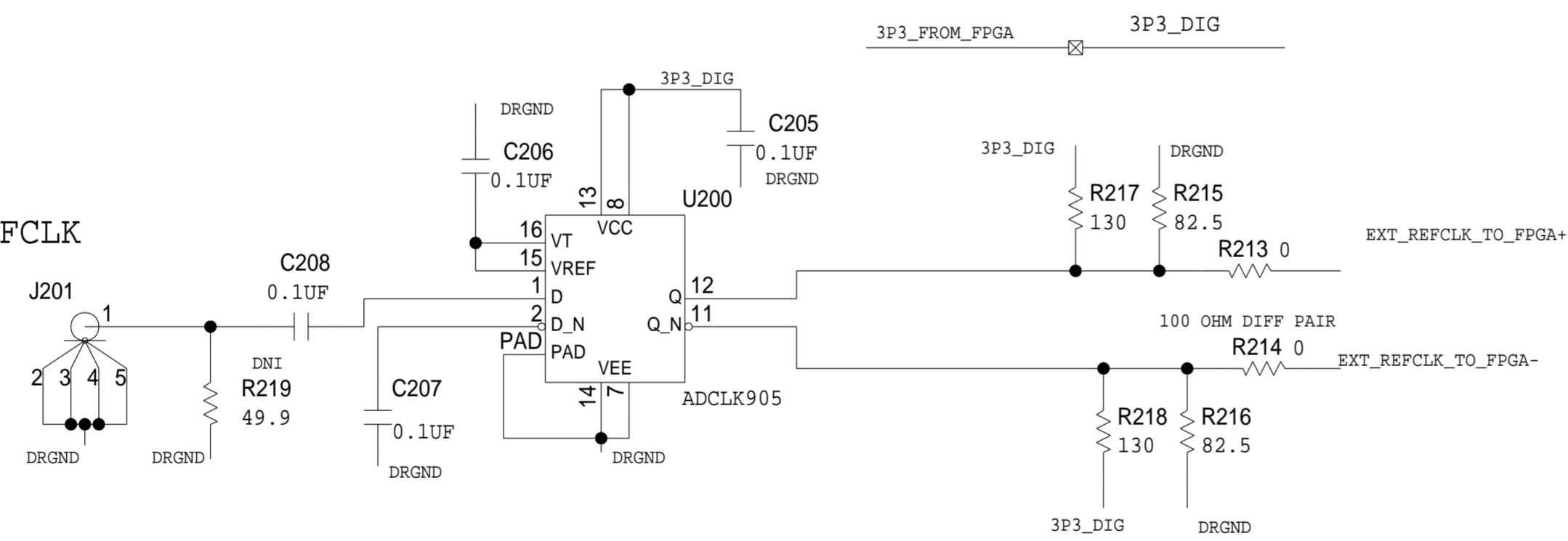
## DSYNC



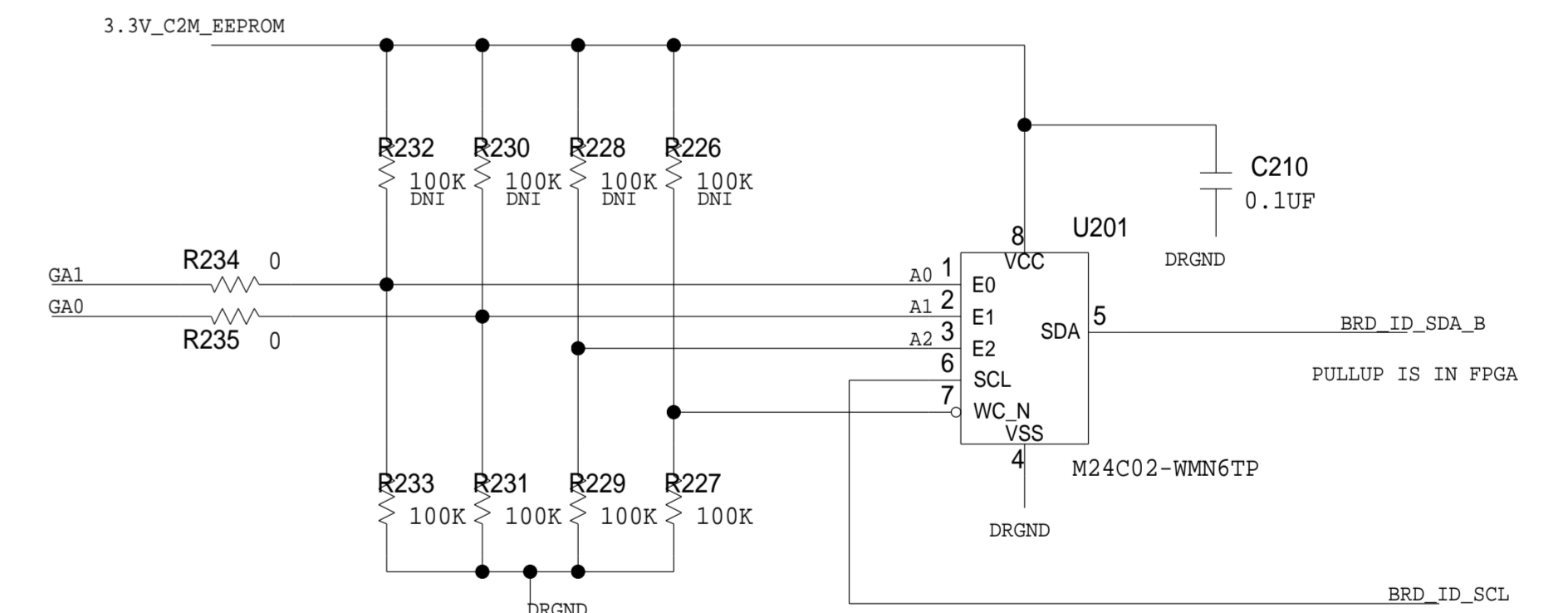
## EXTERNAL SYSREF TO DUT



## EXTERNAL FPGA REFCLK



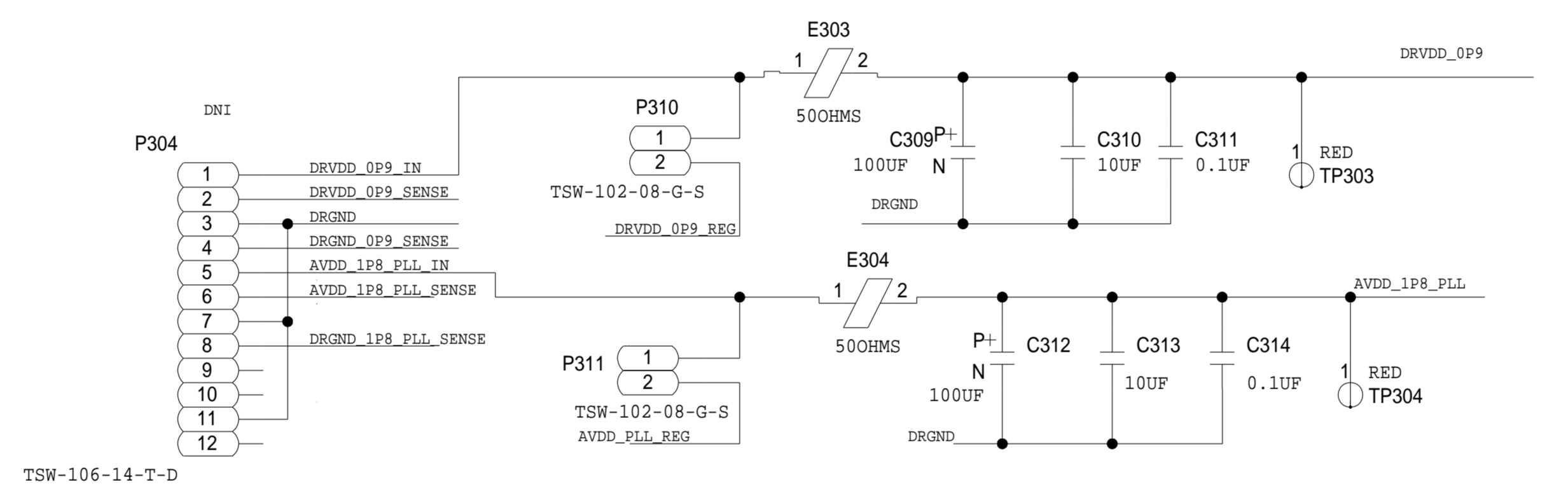
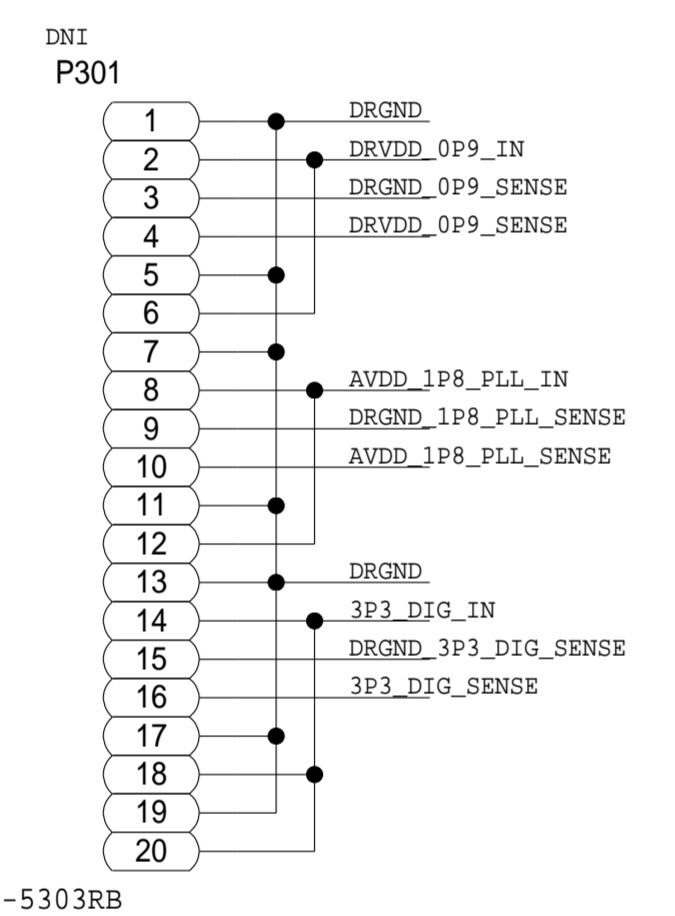
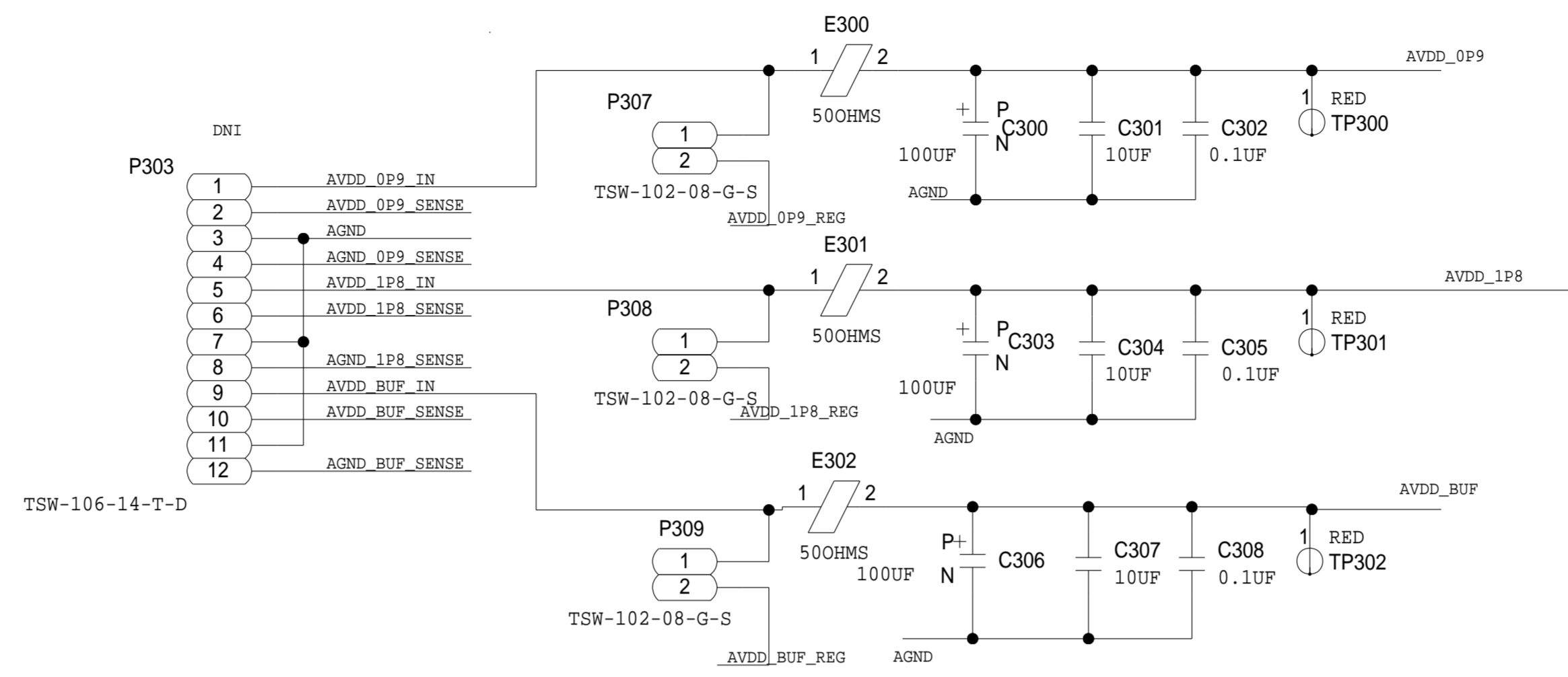
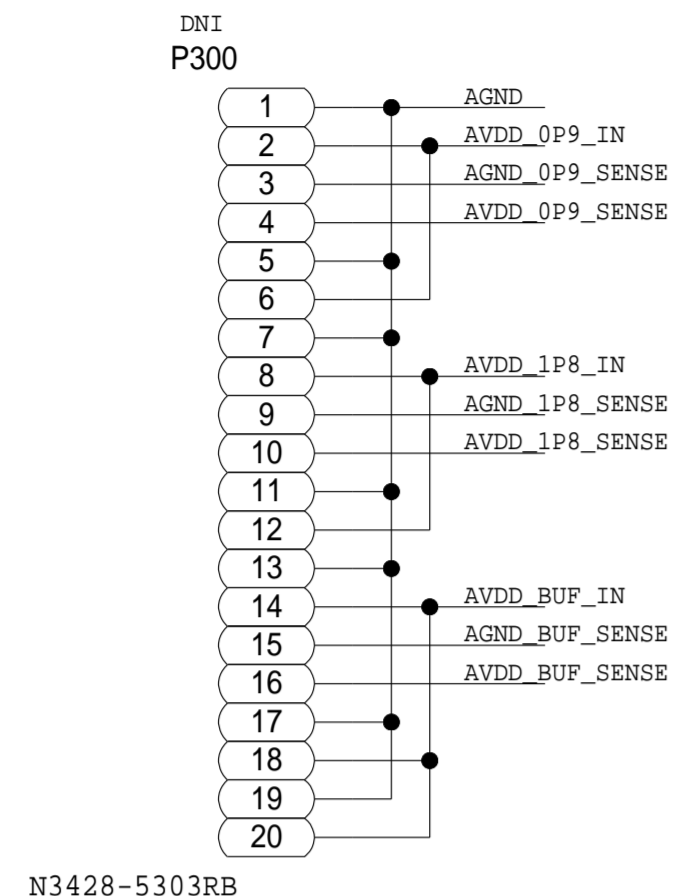
## EEPROM - BOARD ID



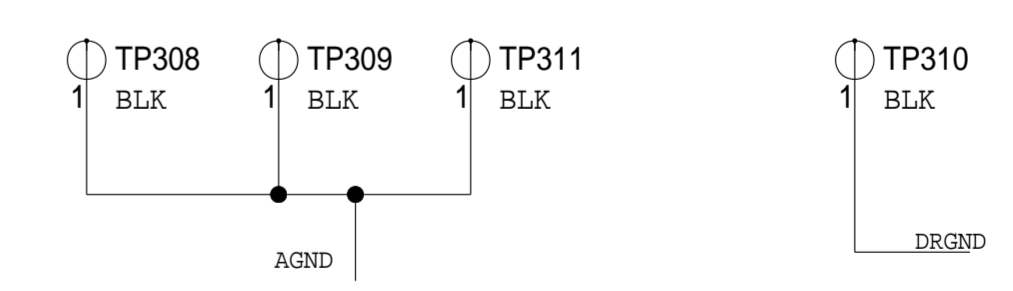
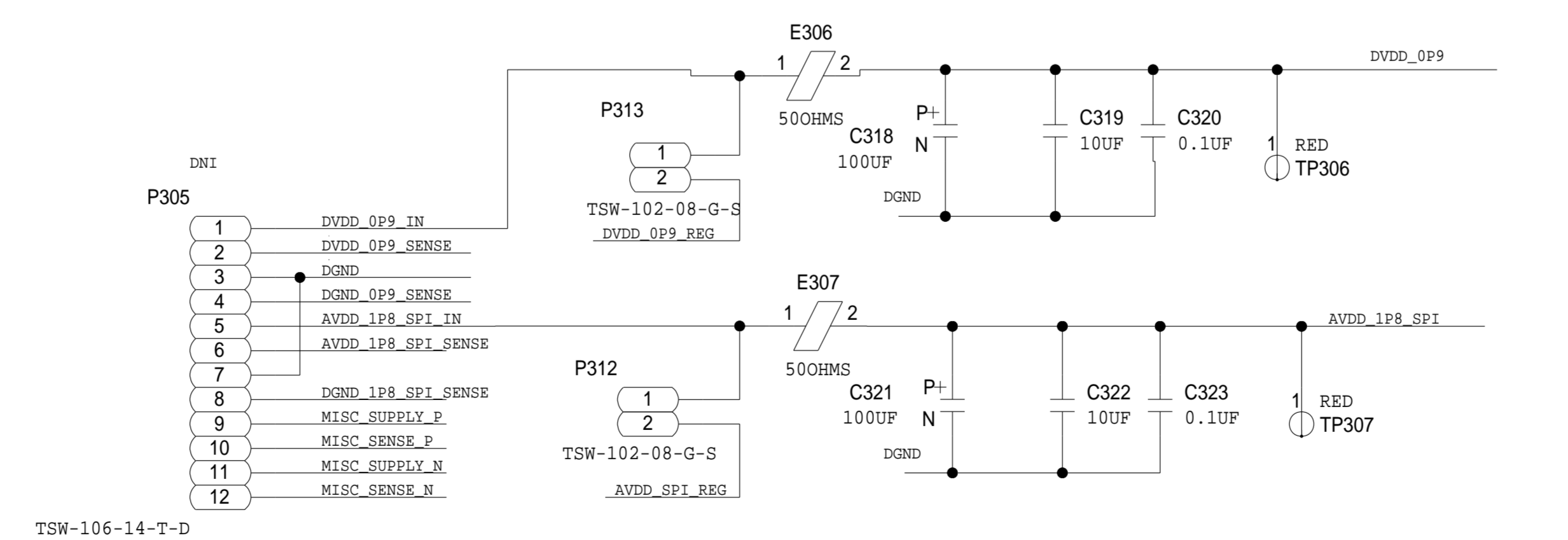
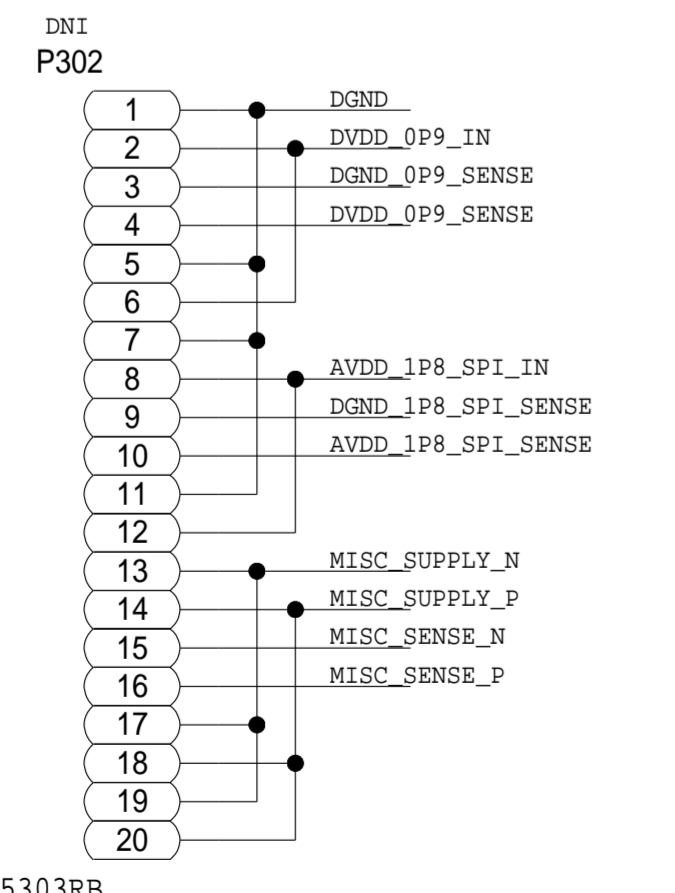
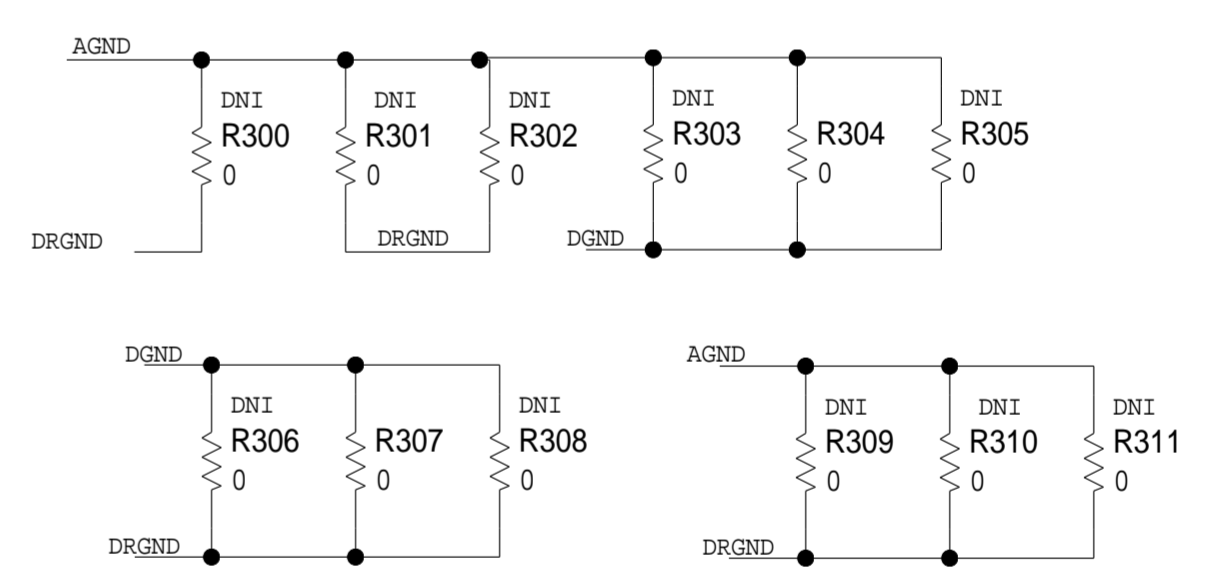
	<b>SCHMATIC</b>		
	CUSTOMER EVALUATION BOARD		
	9694 AD9694		
	DESIGN VIEW -	DRAWING NO. 9694CE01	REV A
PTD ENGINEER J. HARRIS	SIZE D	SCALE NONE	SHEET 2 OF 7

# AD9694 POWER CONNECTIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



LAYOUT: NEED TO ADD TIES TO CONNECT PLANES



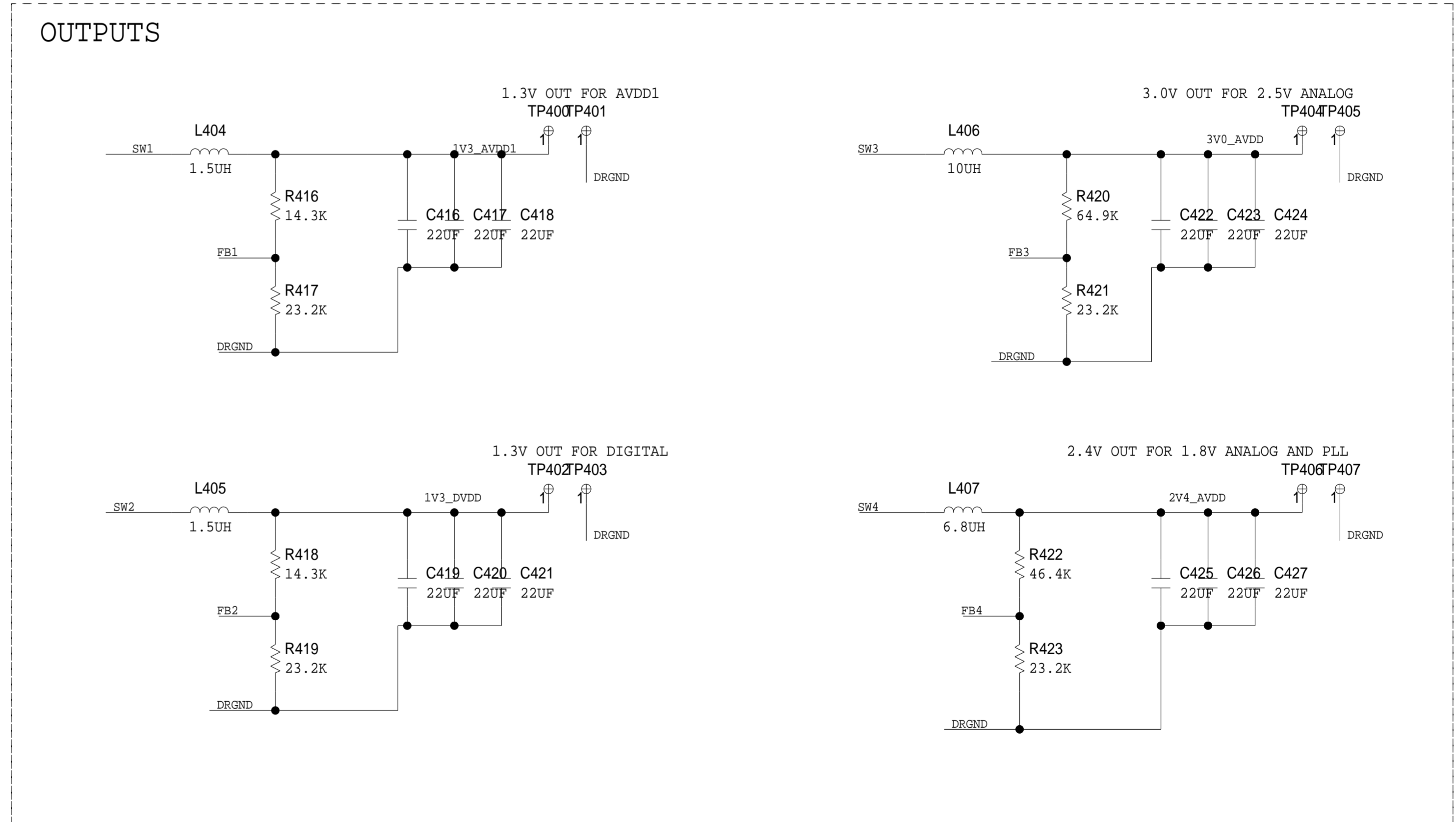
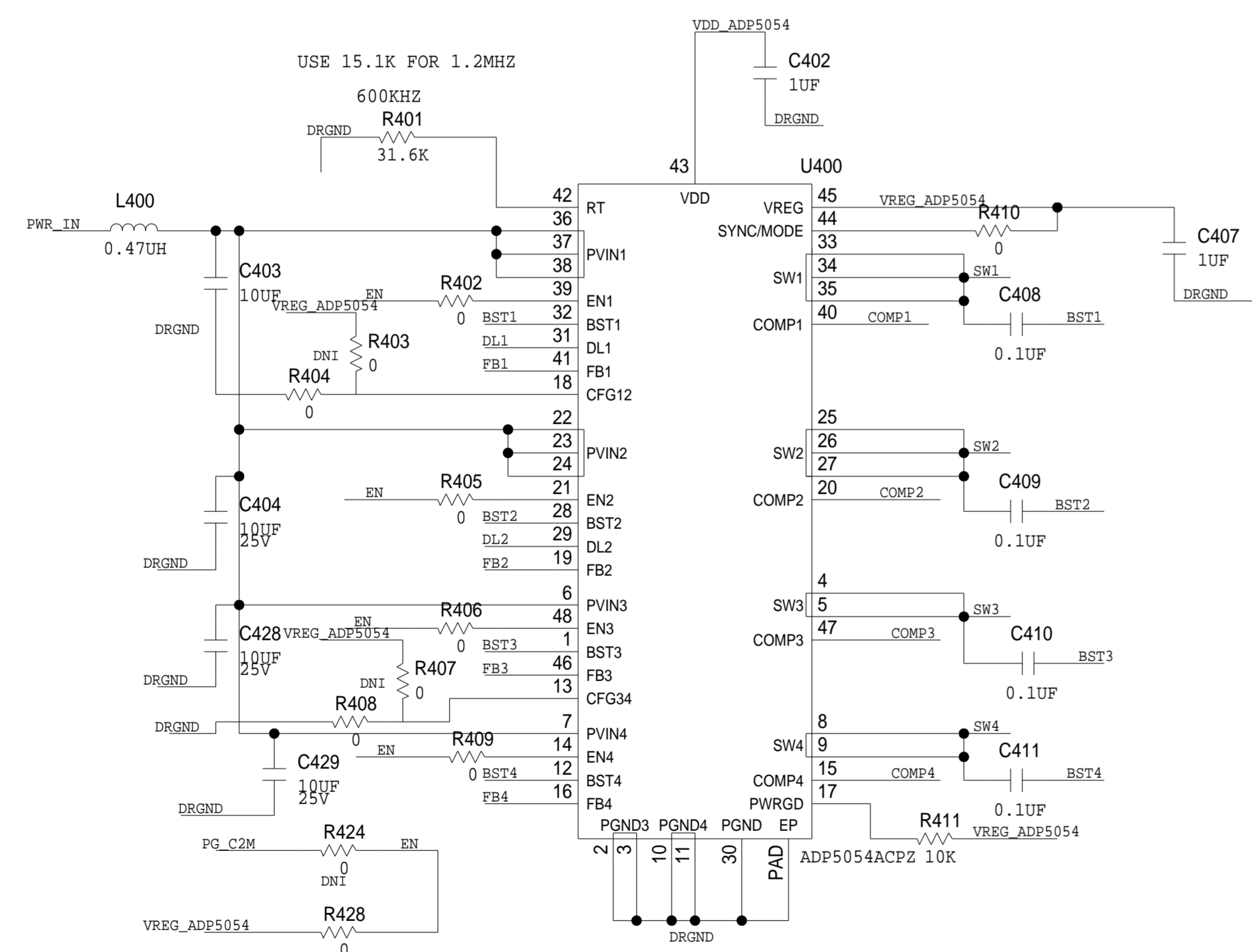
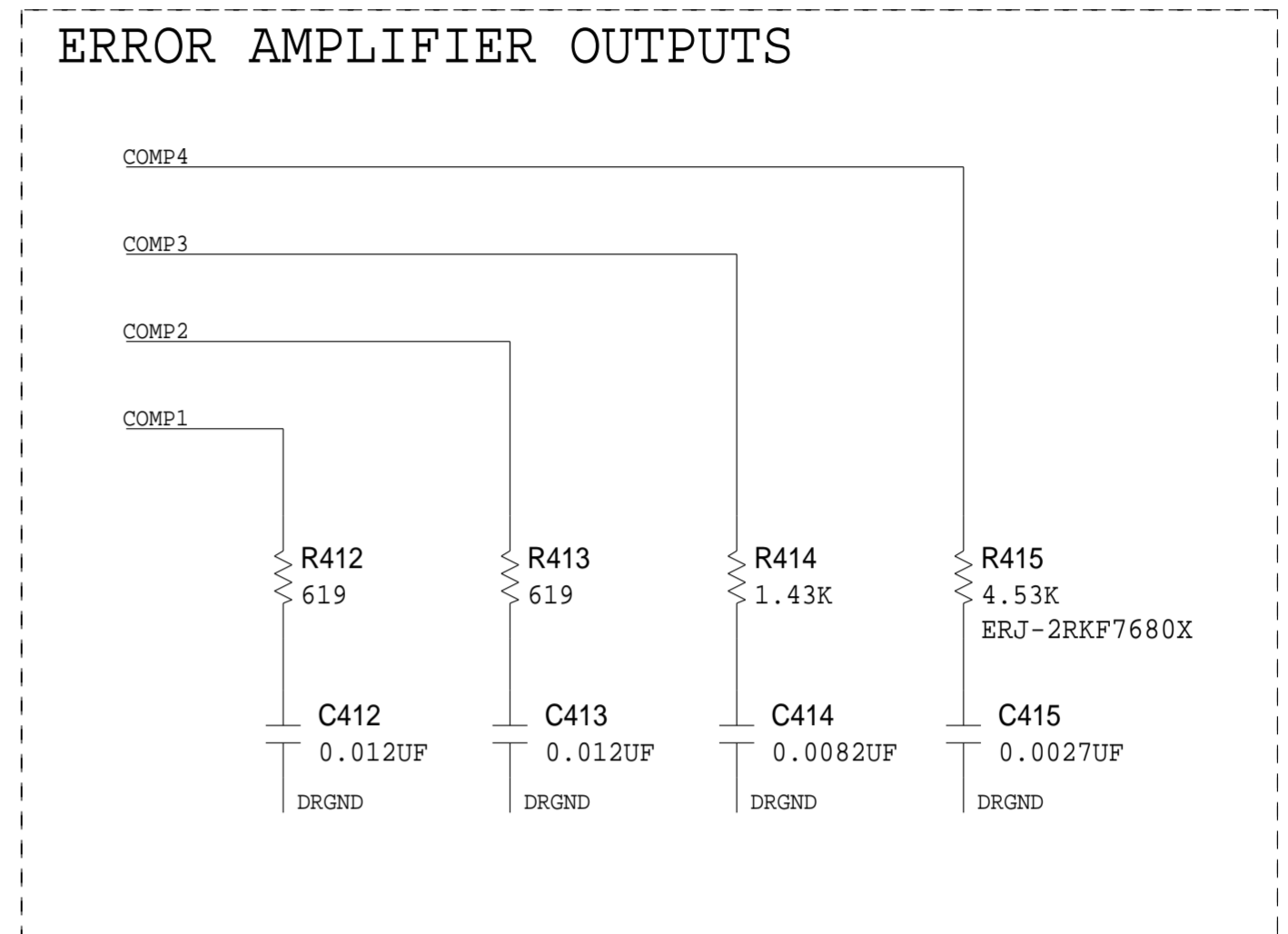
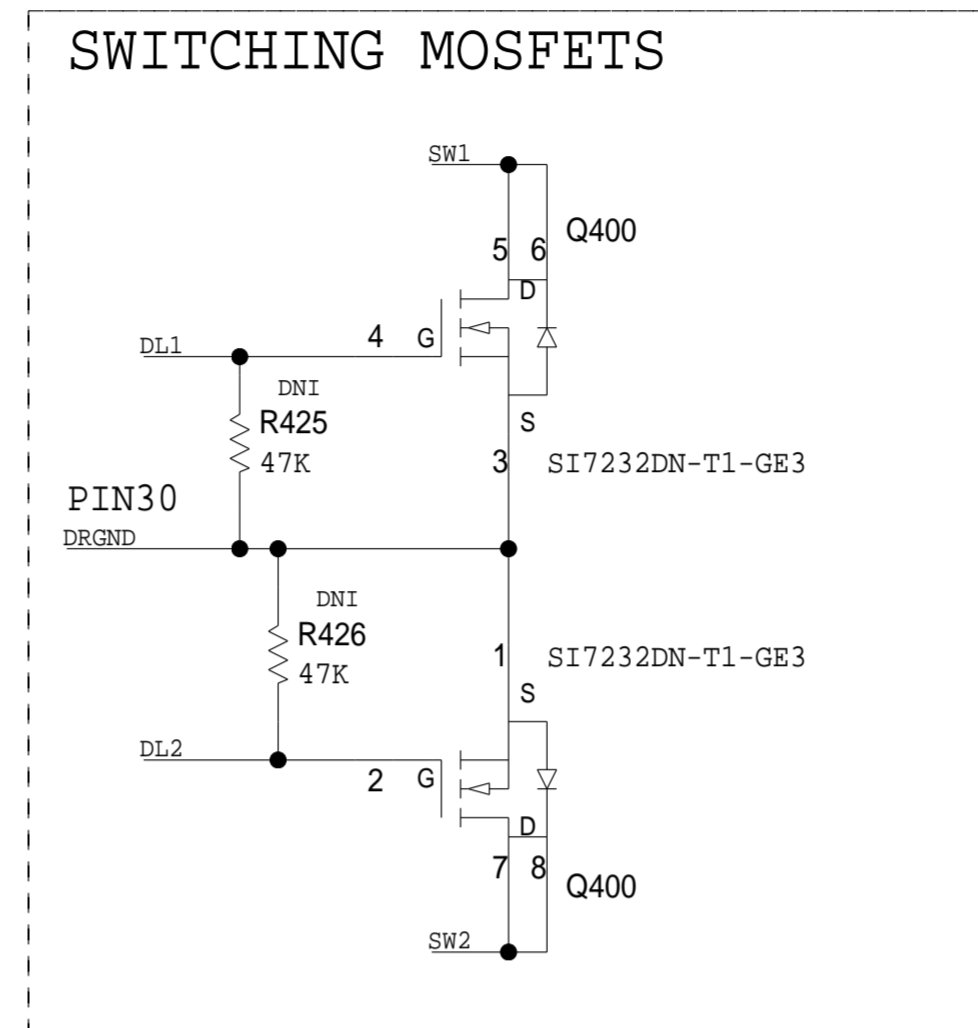
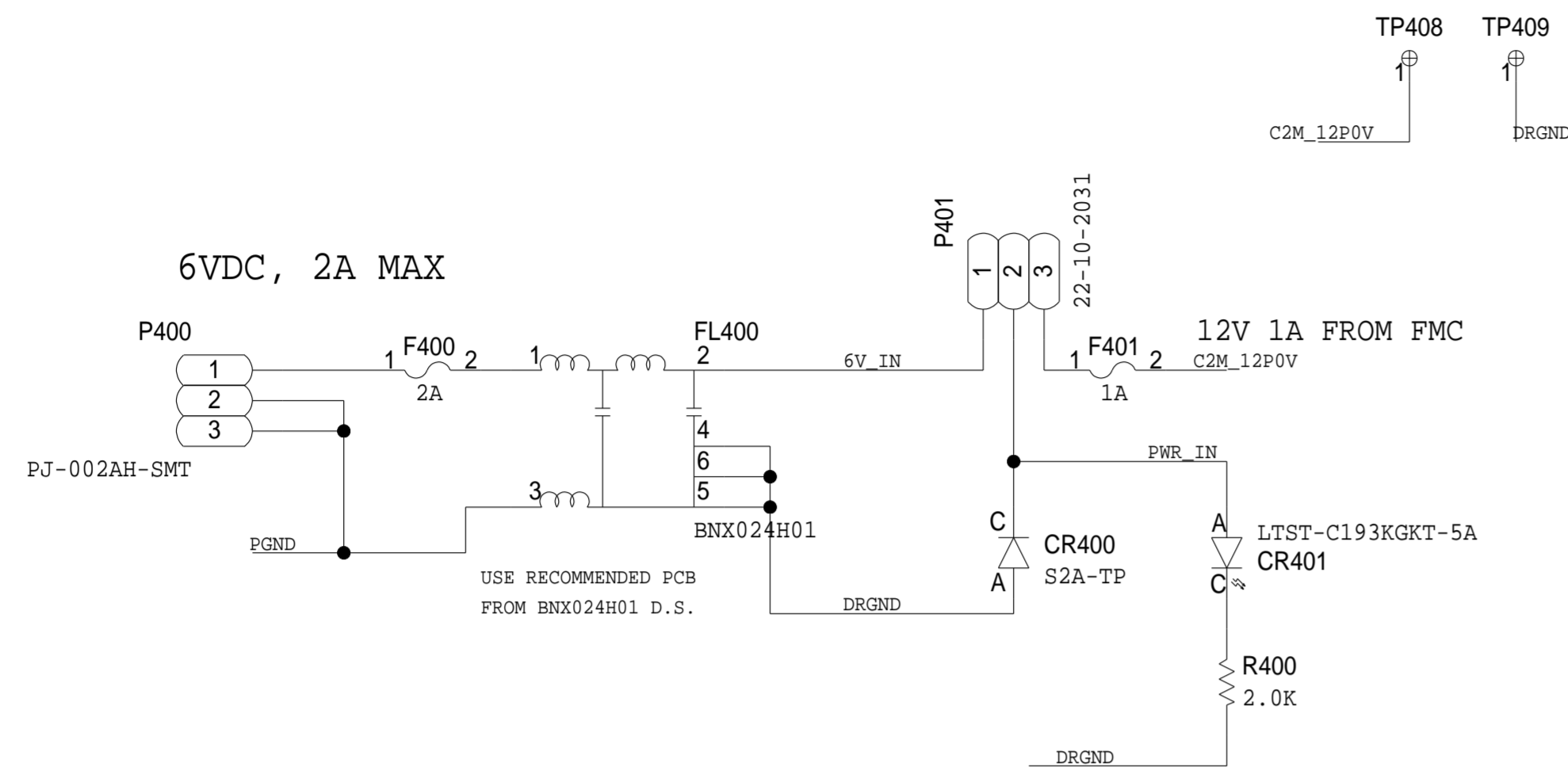
NEW POWER ADAPTER TO SUPPLY

	<b>SCHEMATIC</b>		
	CUSTOMER EVALUATION BOARD 9694 AD9694		
	DESIGN VIEW -	DRAWING NO. 9694CE01	REV A
	PTD ENGINEER J. HARRIS	SIZE D	SCALE NONE
		SHEET 3 OF 7	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

# AD9694 POWER SUPPLY CIRCUITRY

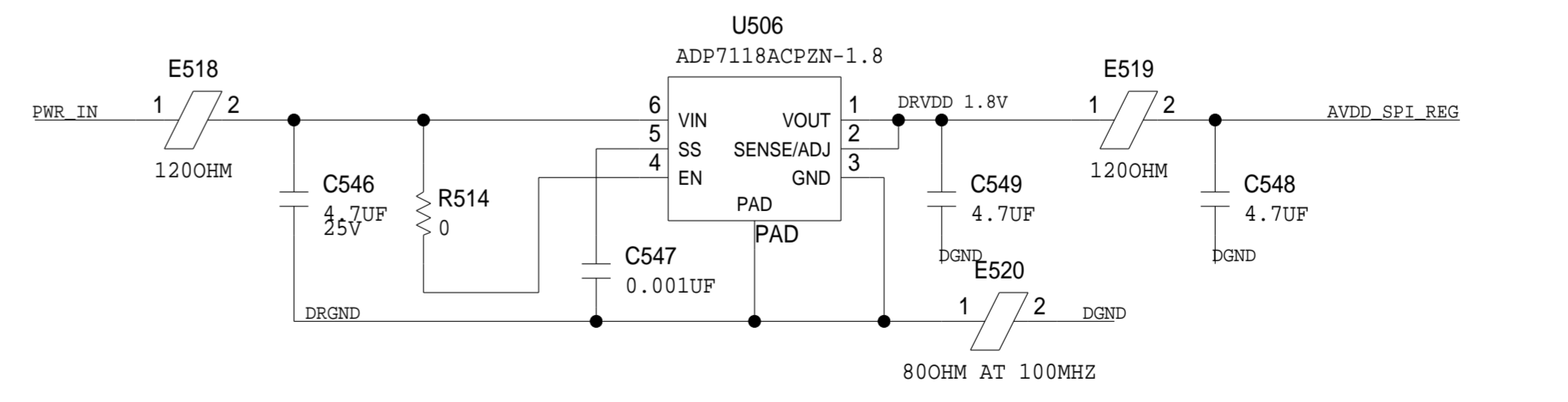
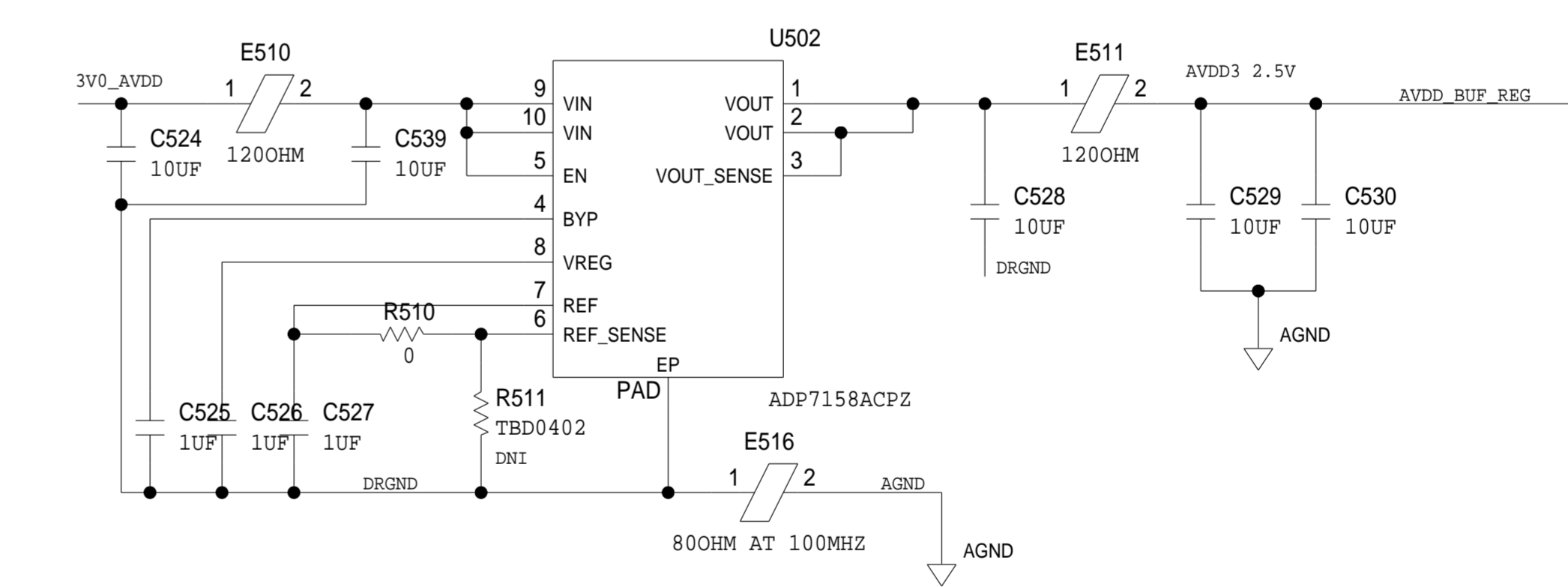
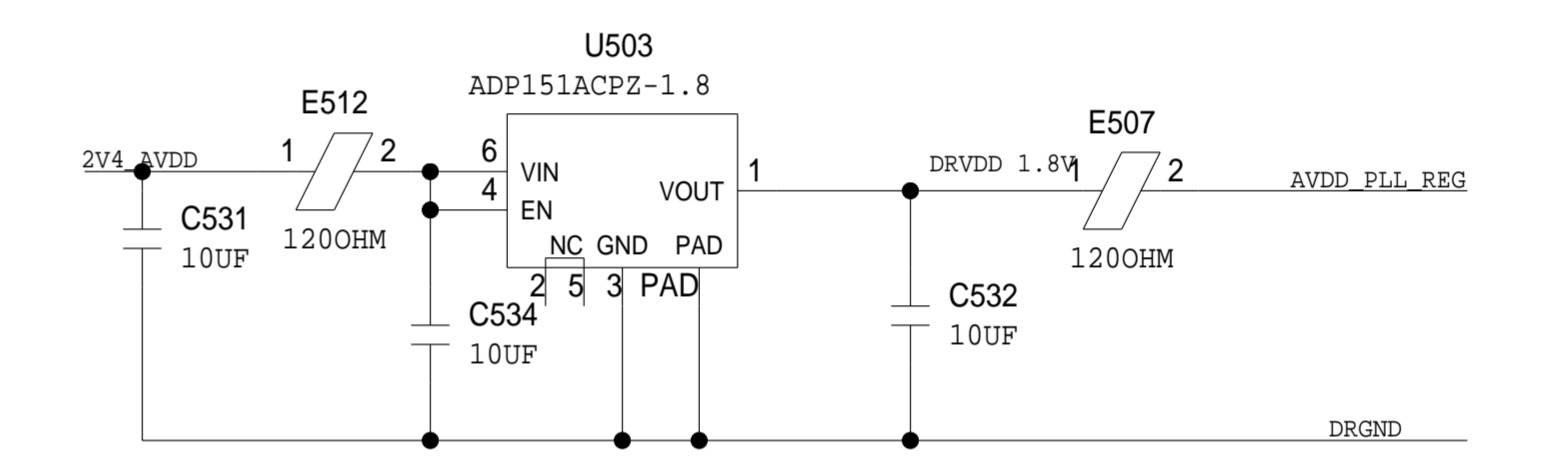
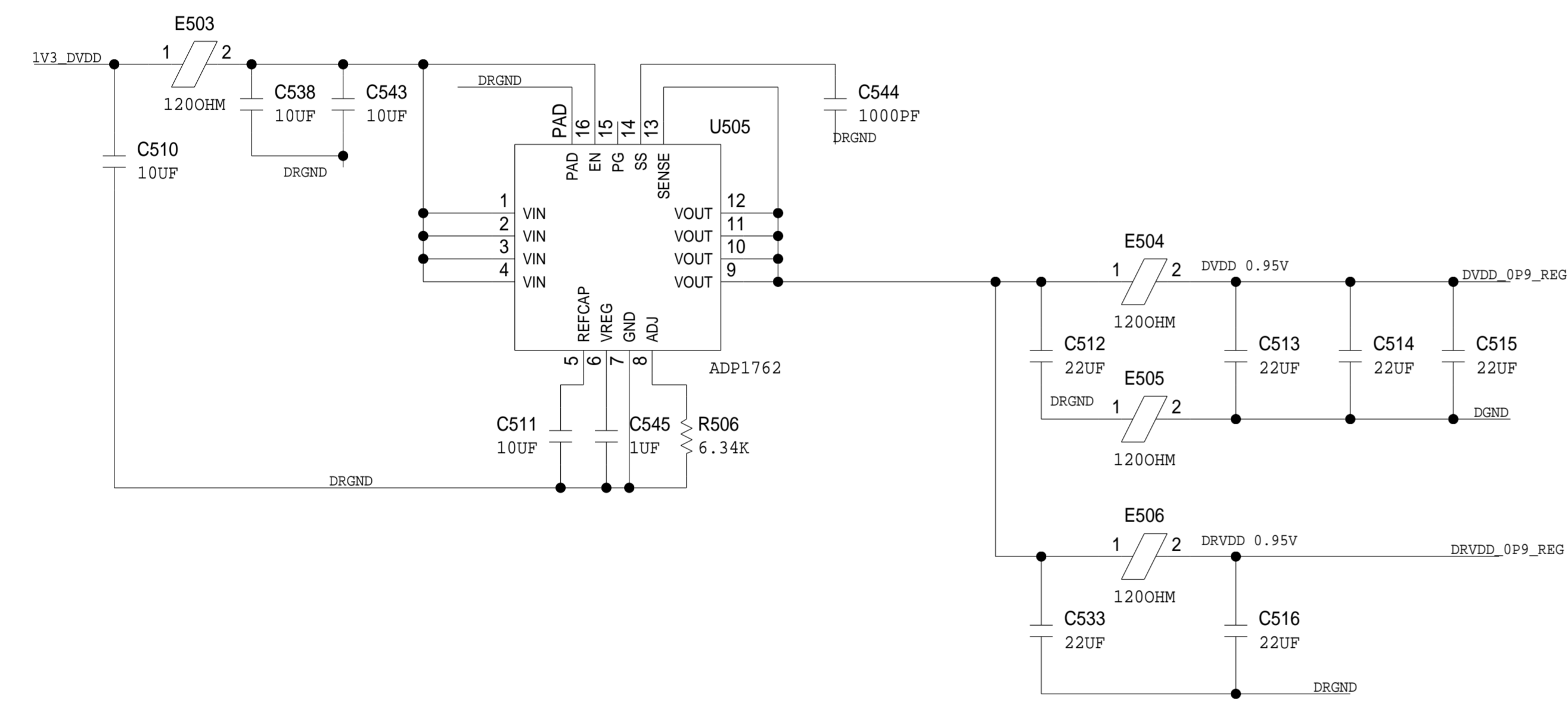
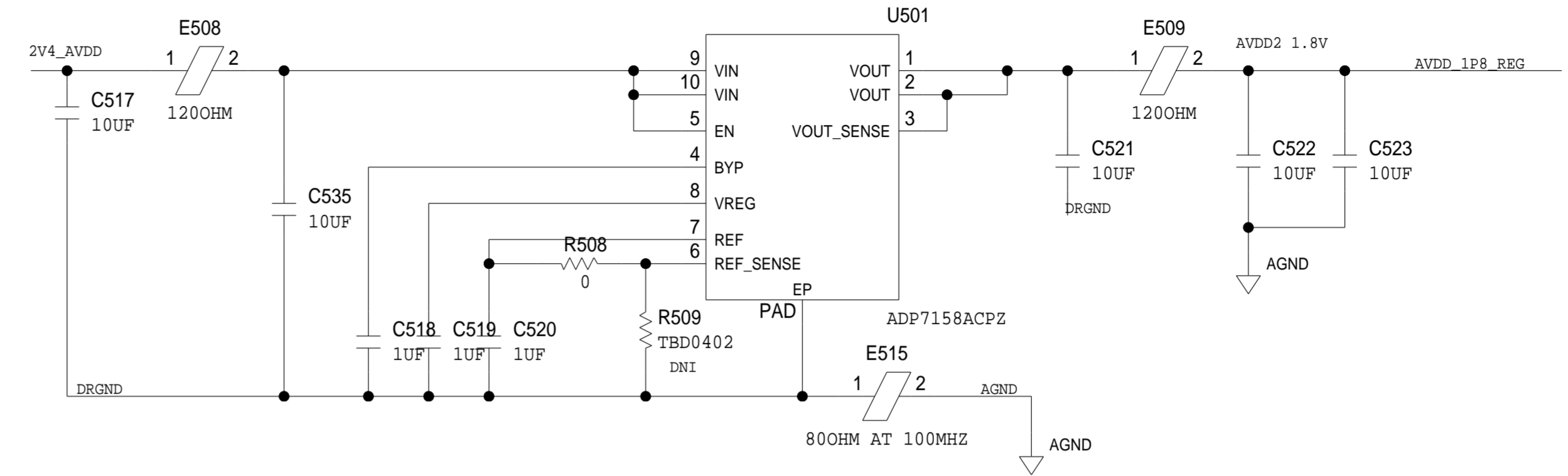
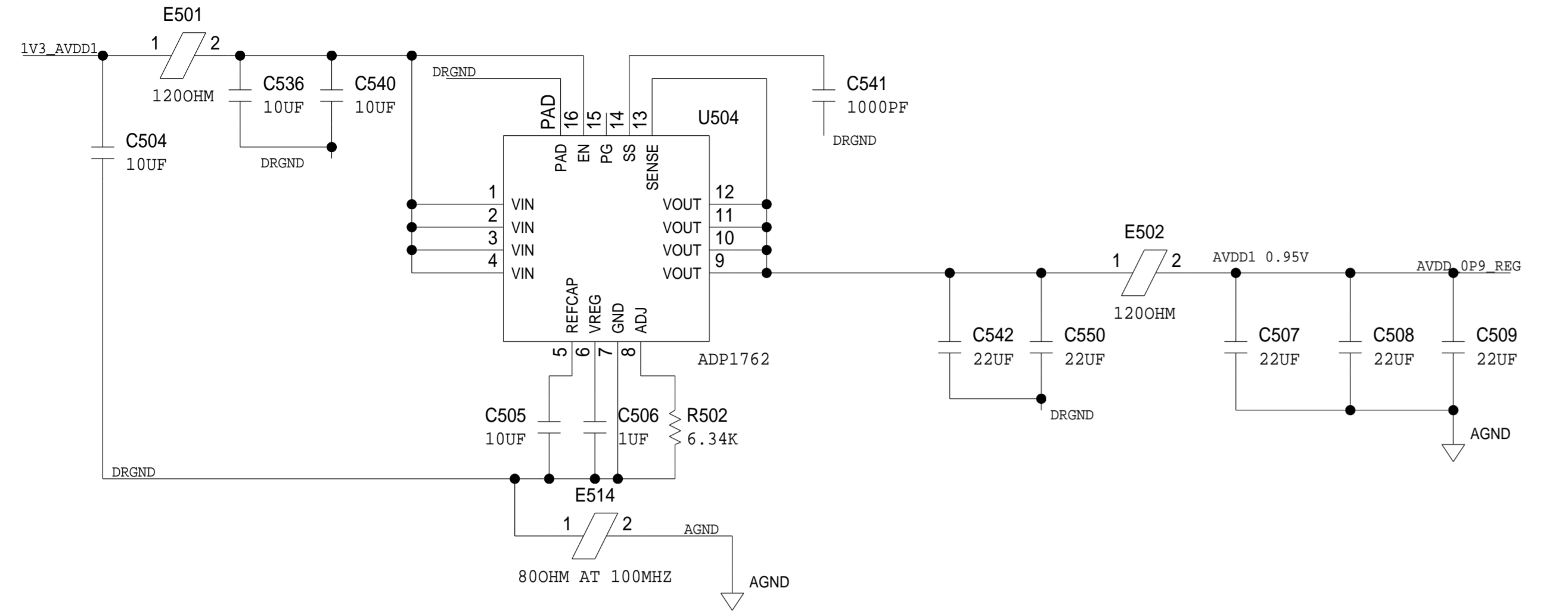
## SUPPLY REGULATORS



	<b>SCHEMATIC</b>		
	CUSTOMER EVALUATION BOARD		
	9694 AD9694		
	DESIGN VIEW	DRAWING NO.	REV
-	9694CE01	A	
PTD ENGINEER	SIZE	SCALE	SHEET 4 OF 7
J. HARRIS	D	NONE	

# AD9694 POWER SUPPLY CIRCUITRY - LDOS

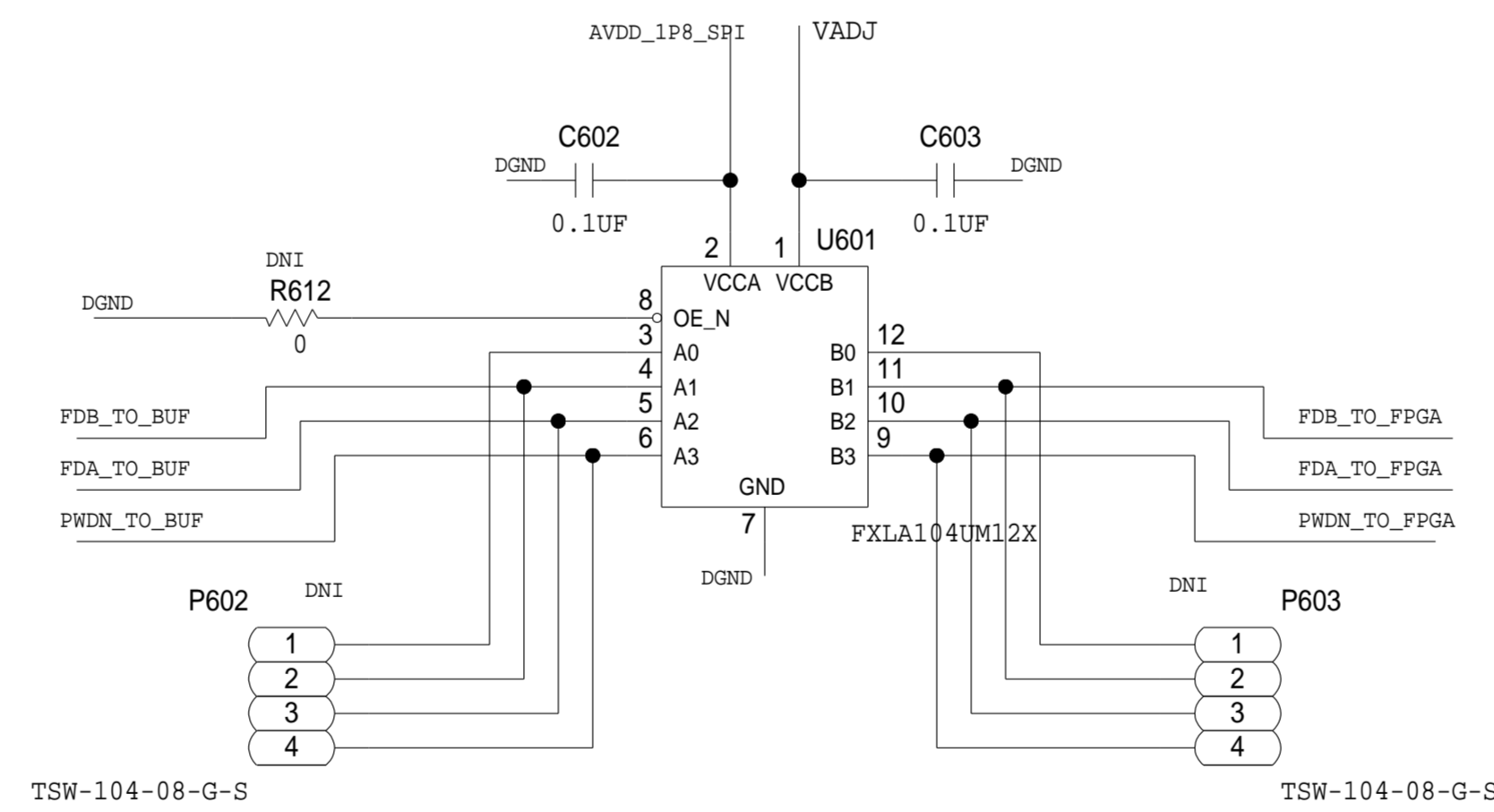
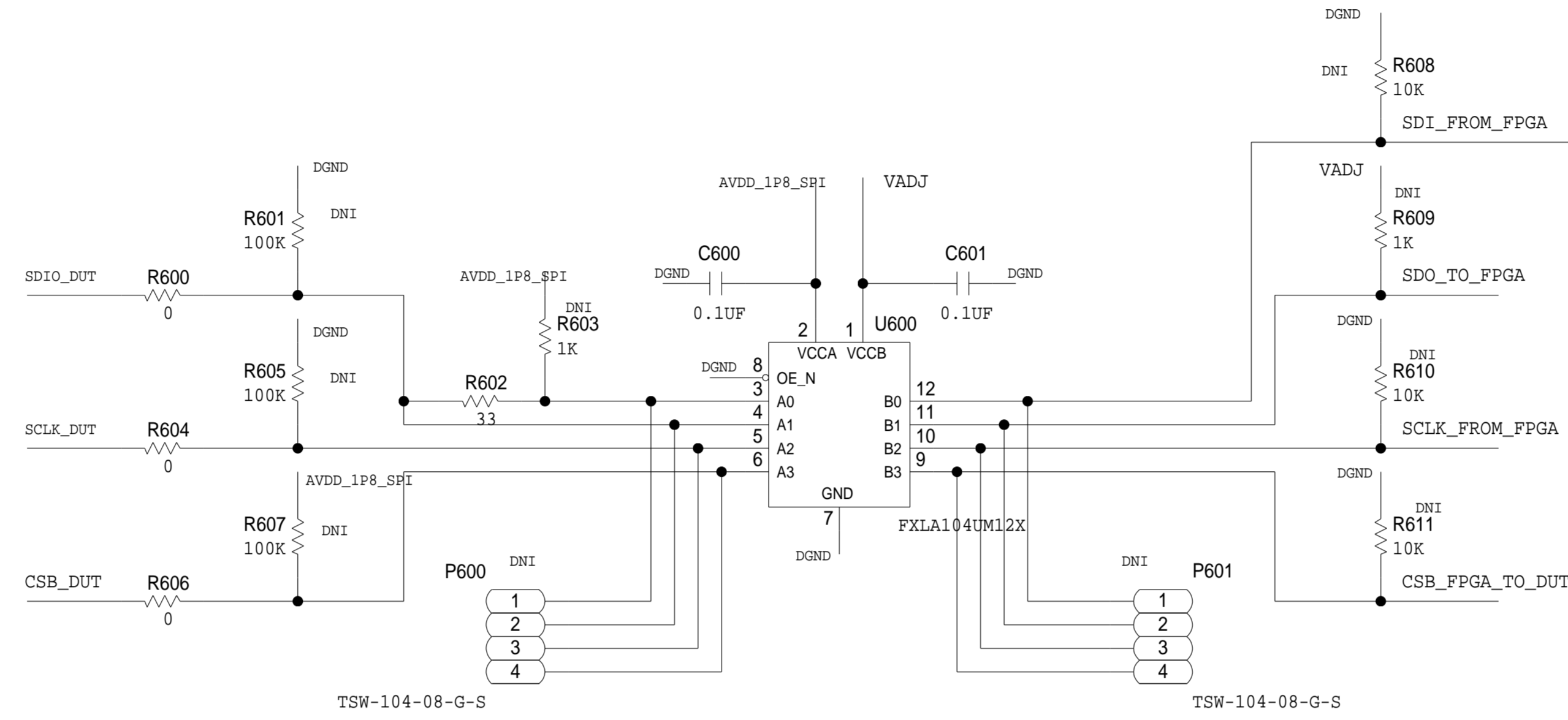
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



	<b>SCHEMATIC</b>		
	CUSTOMER EVALUATION BOARD 9694 AD9694		
	DESIGN VIEW -	DRAWING NO. 9694CE01	REV A
	PTD ENGINEER J. HARRIS	SIZE D	SCALE NONE
		SHEET 5 OF 7	

# AD9694 SPI/BUFFER CIRCUIT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

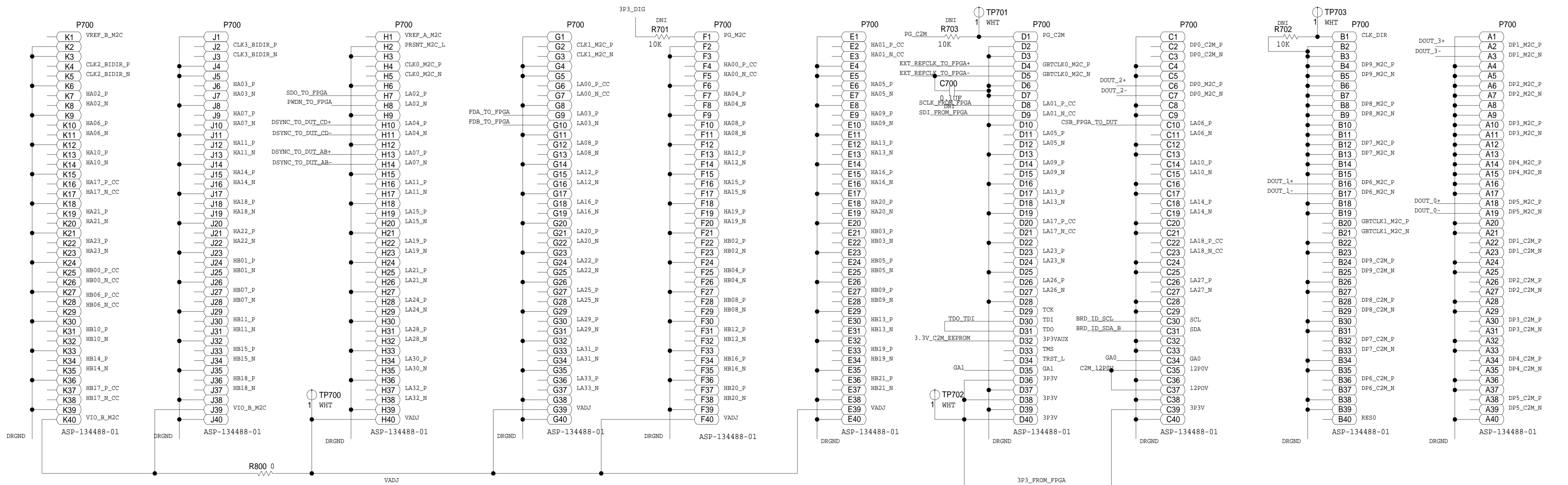
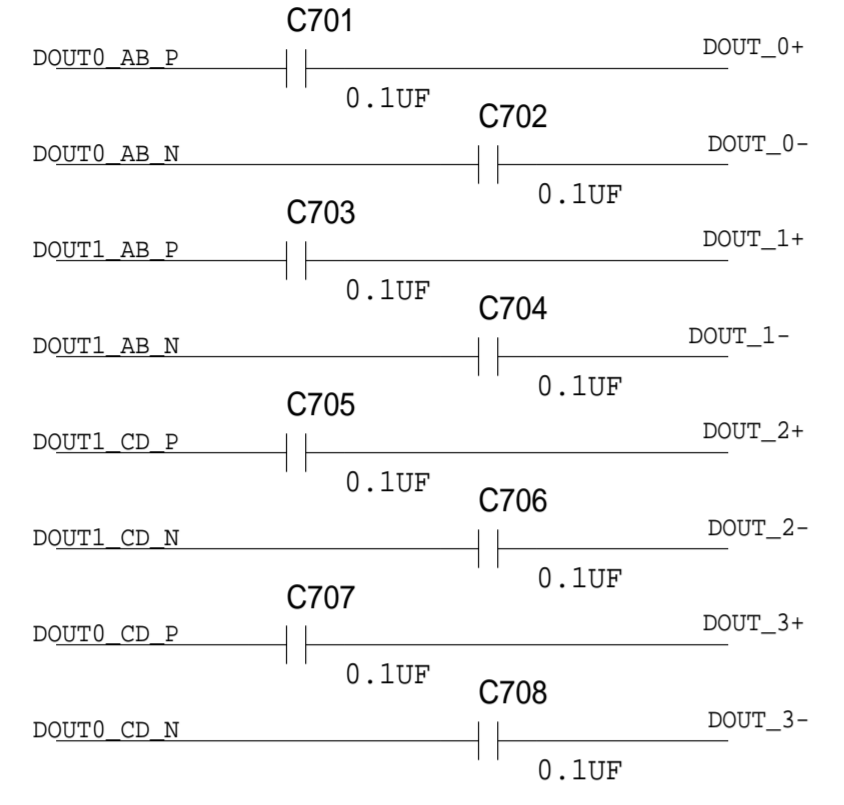


	<b>SCHEMATIC</b>		
	CUSTOMER EVALUATION BOARD		
	9694 AD9694		
	DESIGN VIEW	DRAWING NO.	REV
-	9694CE01	A	
PTD ENGINEER	SIZE	SCALE	SHEET 6 OF 7
J. HARRIS	D	NONE	

# AD9694 ADS7 FMC CONNECTIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

PLACE AS CLOSE TO DUT AS POSSIBLE  
OUTSIDE OF SOCKET



SCHEMATIC			
CUSTOMER EVALUATION BOARD 9694 AD9694			
DESIGN VIEW -	DRAWING NO. 9694CE01	REV A	
PTD ENGINEER J. HARRIS	SIZE D	SCALE NONE	SHEET 7 OF 7

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