RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	03MAR17	R.WILSON
B	REVISED AND REDRAWN	05MAY17	R.WILSON
C	REVISED AND REDRAWN	25MAY17	R.WILSON

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

	DATE
TEMPLATE ENGINEER -	
HARDWARE SERVICES -	
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER -	
TEST PROCESS -	
HARDWARE RELEASE -	
DESIGNER -	
PTD ENGINEER S.GIBBS	13APR17
CHECKER -	

SCHEMATIC

ANALOG DEVICES

HW TYPE : Characterisation
Product(s): AD9213
.
PACKAGE : 192-lead 12X12_MM BGA-family
: Pitch-pitch StyleVendor Style
.
.
.

MASTER PROJECT TEMPLATE: TBD
TESTER TEMPLATE: no_template

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

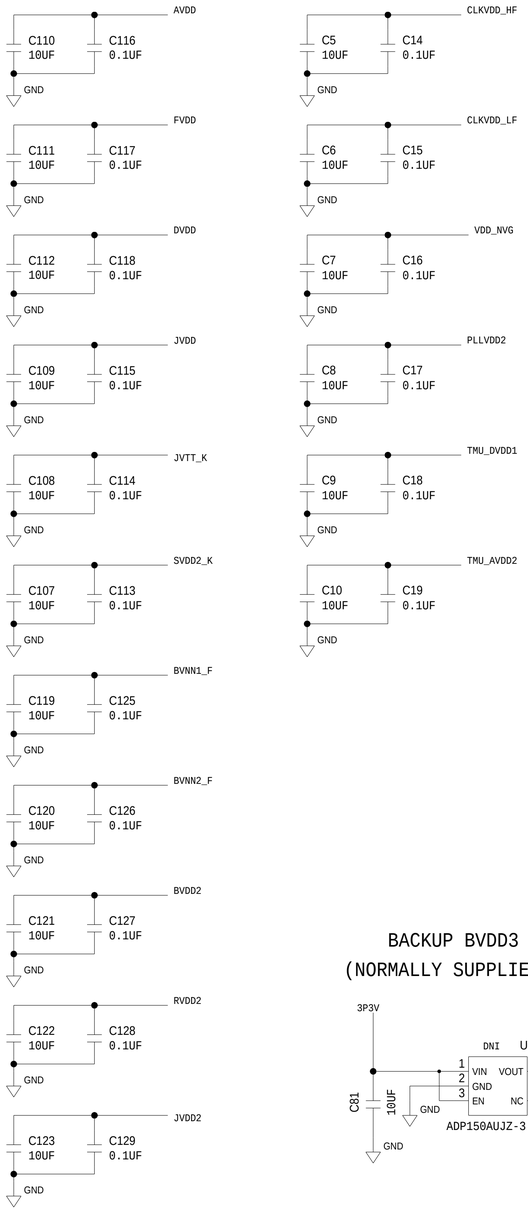
TOLERANCES
DECIMALS: X.XX +-0.010, X.XXX +-0.005
FRACTIONS: +-1/32
ANGLES: +-2

DRAWING NO. 02_044860
REV. C
SIZE D | SCALE 1:1 | CODE ID NO. CodeID | SHEET 1 OF 8

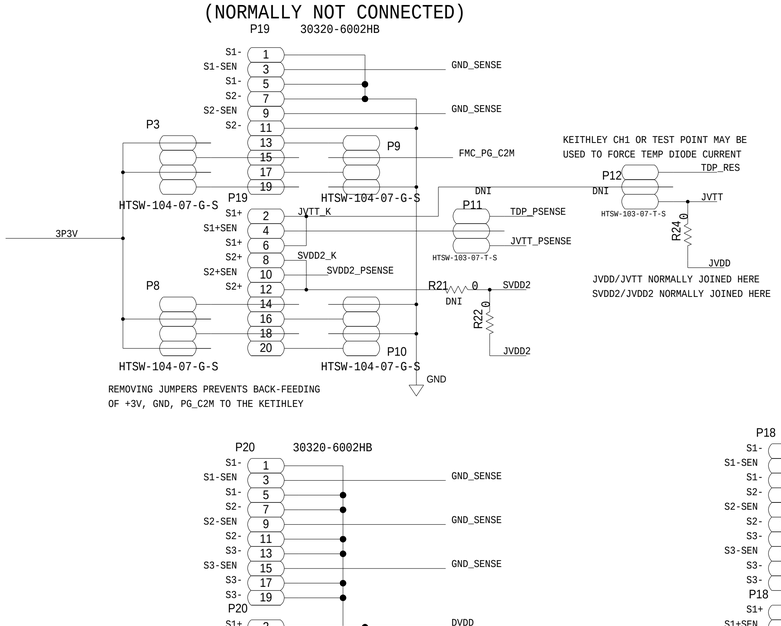
KEITHLEY POWER SUPPLY CONNECTIONS

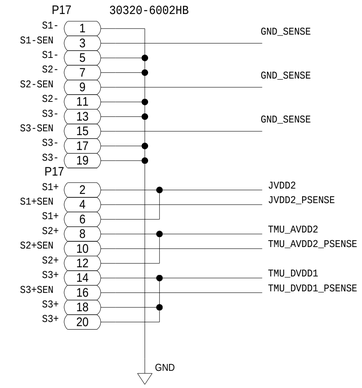
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

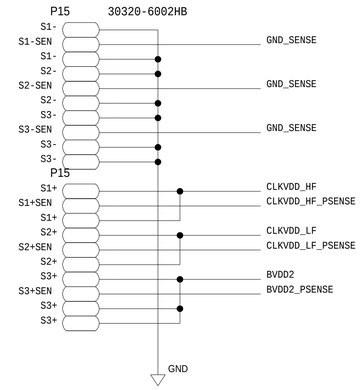
PLACE THESE NEAR THE POWER CONNECTORS

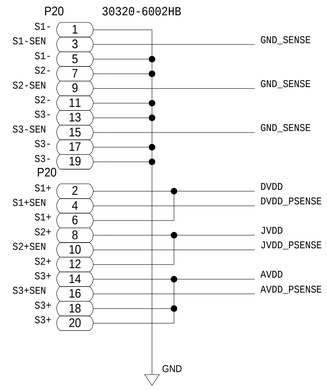


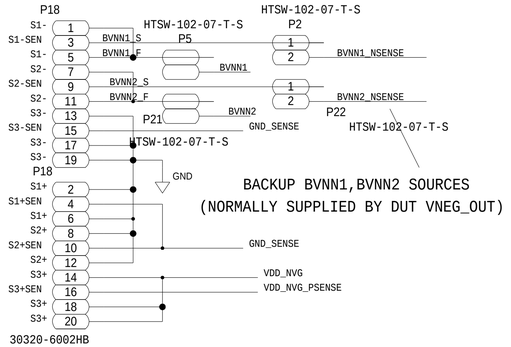
UTILITY CONNECTOR FOR JVTT, SVDD2, TDP/N CONTROL AND POWERING PWR DAUGHTER BD (NORMALLY NOT CONNECTED)



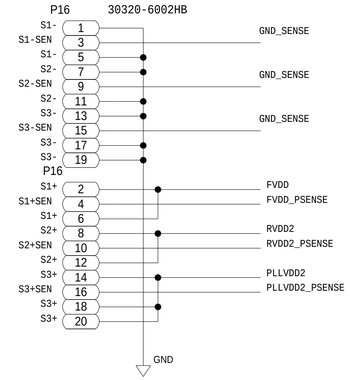




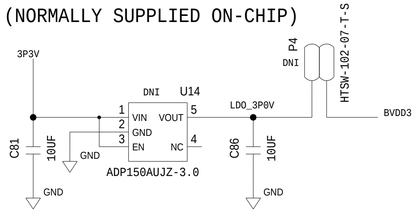




BACKUP BVNN1,BVNN2 SOURCES
(NORMALLY SUPPLIED BY DUT VNEG_OUT)

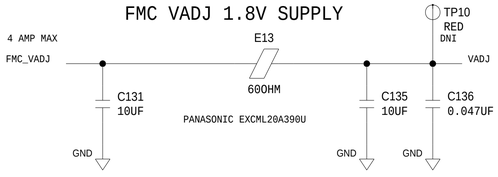


BACKUP BVDD3 SOURCE (NORMALLY SUPPLIED ON-CHIP)

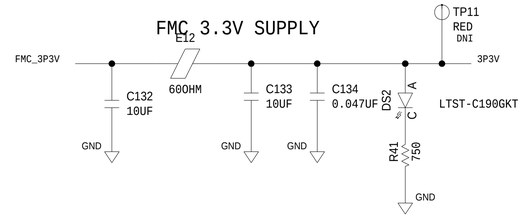


FILTER NETWORKS NEAR FMC CONNECTOR

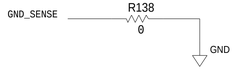
FMC VADJ 1.8V SUPPLY



FMC 3.3V SUPPLY



GND SENSE VIA NEAR OR UNDER DUT



NOTE: KEITHLEY 2230 CHAN 3 IS 5A
BUT CHAN 1 & 2 ARE 1.5A

ANALOG DEVICES

SCHEMATIC

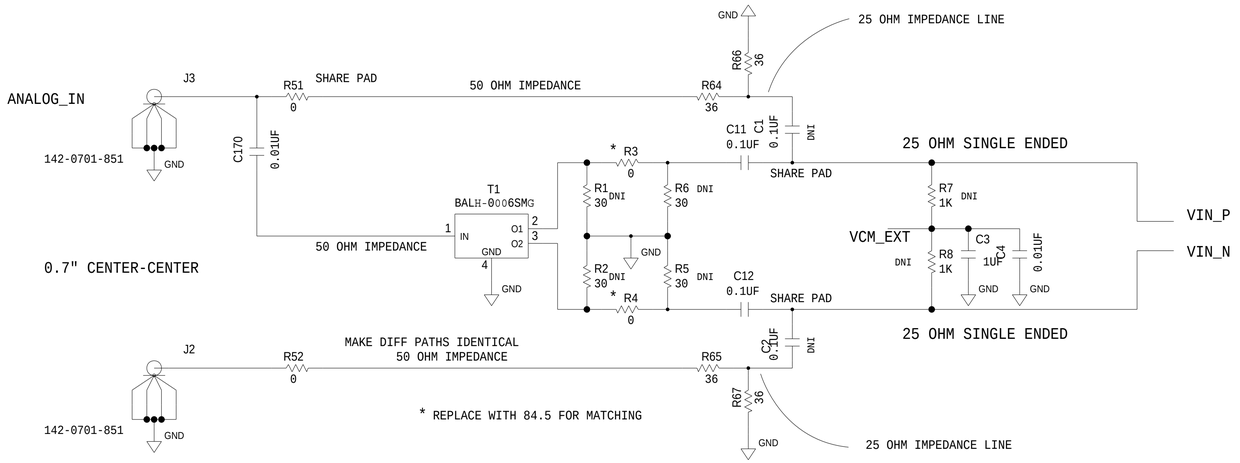
HW TYPE : Characterisation
Product(s): AD9213

DESIGN VIEW: <DESIGN_VIEW>
DRAWING NO.: 02_044860
REV: C
PTD ENGINEER: S.GIBBS
SIZE: D
SCALE: 1:1
SHEET 2 OF 8


COMBINED PHOENIX SOCKET
AND SOLDER-DOWN FOOTPRINT
NEEDS SOLDERMASK UNDER SOCKET
PLACE SENSE LINE VIAS AS
CLOSE TO DUT AS POSSIBLE
SERDOUT 100 OHM DIFF PAIRS
NEAR FMC+ CONNECTOR
CLOSE TO DUT
PLL LOOP FILTER
STACK FOOTPRINTS
PLACE CAP
NEXT TO BALL
AD9213
DUT1
BGA196-0.8-12
J1
142-0701-851
HTSW-102-07-T-S
P6
E1
120OHM AT 100MEGHZ
CLKVDD_LF
CLKVDD_LF_PSENSE
CLKVDD_HF
CLKVDD_HF_PSENSE
BVDD2
BVDD2_PSENSE
RVDD2
RVDD2_PSENSE
JVDD2
JVDD2_PSENSE
SVDD2
SVDD2_PSENSE
BVNN1
BVNN1_NSENSE
BVNN2
BVNN2_NSENSE
PLLVDD2
PLLVDD2_PSENSE
VDD_NVG
VDD_NVG_PSENSE
TMU_AVDD2
TMU_AVDD2_PSENSE
TMU_DVDD1
TMU_DVDD1_PSENSE
AVDD
AVDD_PSENSE
DVDD
DVDD_PSENSE
JVDD
JVDD_PSENSE
JVTT
JVTT_PSENSE
FVDD
FVDD_PSENSE
AVNN1
BVNN1
TP16 RED
TP5 RED
TP6 RED
TP1 RED
TP2 RED
C20 2.2UF
C22 0.033UF
C21 330PF
C23 3000PF
C24 0.01UF DNI
R28 576
C13 0.1UF
R16 0 DNI
R48 100 DNI
R19 15K
R27 0
R58 0
R26 100 DNI
R15 15K
R23 100
R20 0
TRIG_N
TRIG_P
TDP_RES
TDP_PSENSE
SYSREF_P
SYSREF_N
FPGA_SYNCINB_P
FPGA_SYNCINB_N
TMU_AVDD2
GND
SERDOUT_P_0 C138 0.1UF SER_OUT_P_0
SERDOUT_N_0 C139 0.1UF SER_OUT_N_0
SERDOUT_P_1 C77 0.1UF SER_OUT_P_1
SERDOUT_N_1 C78 0.1UF SER_OUT_N_1
SERDOUT_P_2 C79 0.1UF SER_OUT_P_2
SERDOUT_N_2 C80 0.1UF SER_OUT_N_2
SERDOUT_P_3 C82 0.1UF SER_OUT_P_3
SERDOUT_N_3 C83 0.1UF SER_OUT_N_3
SERDOUT_P_4 C84 0.1UF SER_OUT_P_4
SERDOUT_N_4 C85 0.1UF SER_OUT_N_4
SERDOUT_P_5 C87 0.1UF SER_OUT_P_5
SERDOUT_N_5 C88 0.1UF SER_OUT_N_5
SERDOUT_P_6 C89 0.1UF SER_OUT_P_6
SERDOUT_N_6 C90 0.1UF SER_OUT_N_6
SERDOUT_P_7 C91 0.1UF SER_OUT_P_7
SERDOUT_N_7 C92 0.1UF SER_OUT_N_7
SERDOUT_P_8 C93 0.1UF SER_OUT_P_8
SERDOUT_N_8 C94 0.1UF SER_OUT_N_8
SERDOUT_P_9 C95 0.1UF SER_OUT_P_9
SERDOUT_N_9 C96 0.1UF SER_OUT_N_9
SERDOUT_P_10 C97 0.1UF SER_OUT_P_10
SERDOUT_N_10 C98 0.1UF SER_OUT_N_10
SERDOUT_P_11 C99 0.1UF SER_OUT_P_11
SERDOUT_N_11 C100 0.1UF SER_OUT_N_11
SERDOUT_P_12 C101 0.1UF SER_OUT_P_12
SERDOUT_N_12 C102 0.1UF SER_OUT_N_12
SERDOUT_P_13 C103 0.1UF SER_OUT_P_13
SERDOUT_N_13 C104 0.1UF SER_OUT_N_13
SERDOUT_P_14 C105 0.1UF SER_OUT_P_14
SERDOUT_N_14 C106 0.1UF SER_OUT_N_14
SERDOUT_P_15 C124 0.1UF SER_OUT_P_15
SERDOUT_N_15 C130 0.1UF SER_OUT_N_15
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
ANALOG DEVICES
SCHEMATIC
HW TYPE : Characterisation
Product(s): AD9213
DESIGN VIEW
<DESIGN_VIEW>
DRAWING NO.
02_044860
REV
C
PTD ENGINEER
S.GIBBS
SIZE
D
SCALE
1:1
SHEET 3 OF 8

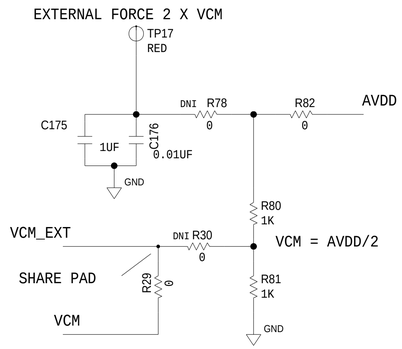
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG INPUT

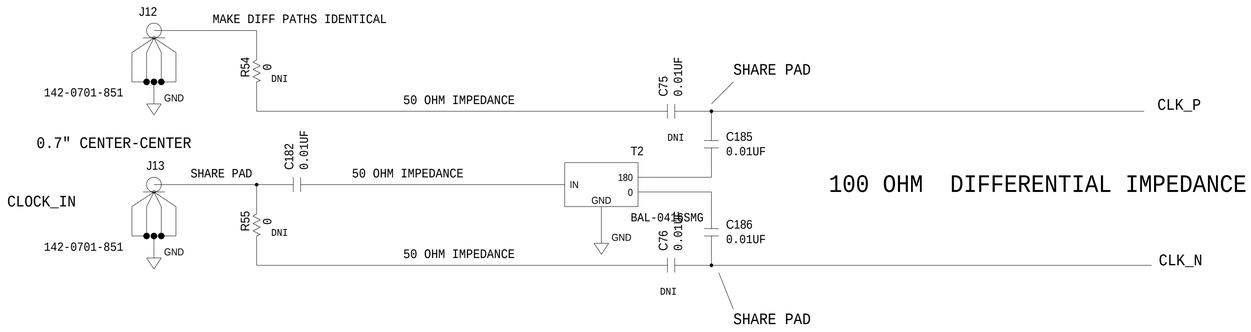


OPTIONAL VCM

SUPPLIED ON-CHIP BY DEFAULT



CLOCK INPUT



EXTERNAL BALUN WILL SUPPORT VERY LOW FREQUENCY CLOCK

ANALOG DEVICES

SCHEMATIC

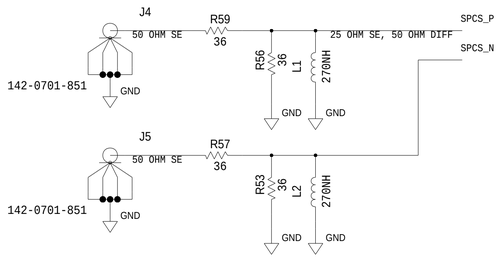
HW TYPE : Characterisation
Product(s): AD9213
.

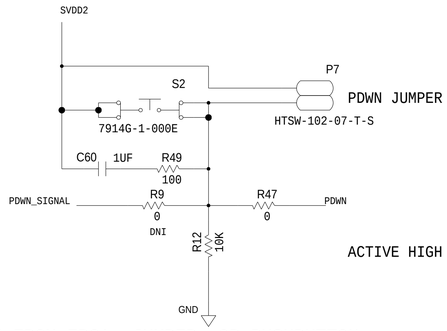
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_044860	C
PTD ENGINEER S.GIBBS	SIZE D / SCALE 1:1	SHEET 4 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

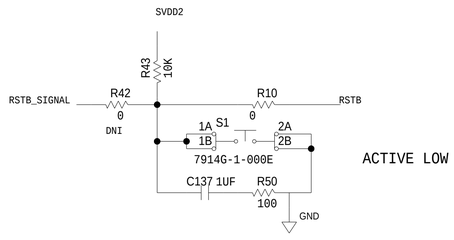
SYSREF,TRIG,SPCS,RSTB,PDWN,TDP/TDN,AGC

FUTURE NON-LINEAR CAL 4GHZ TONE FROM ON-CHIP DAC

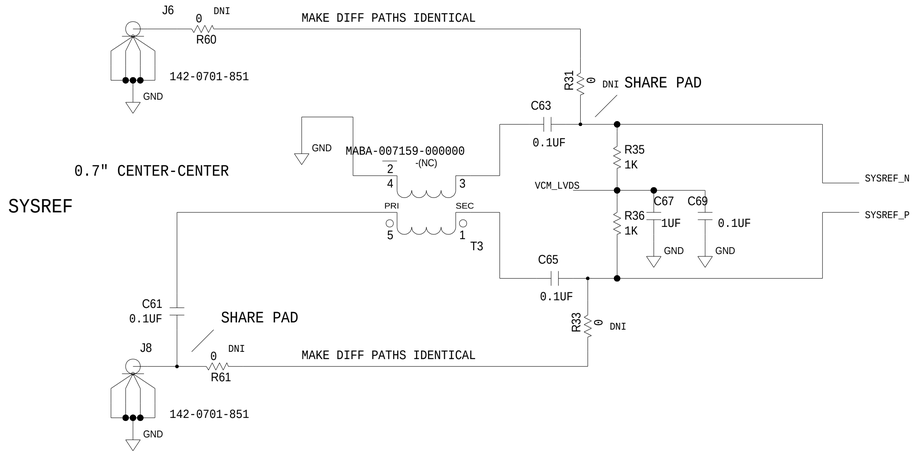




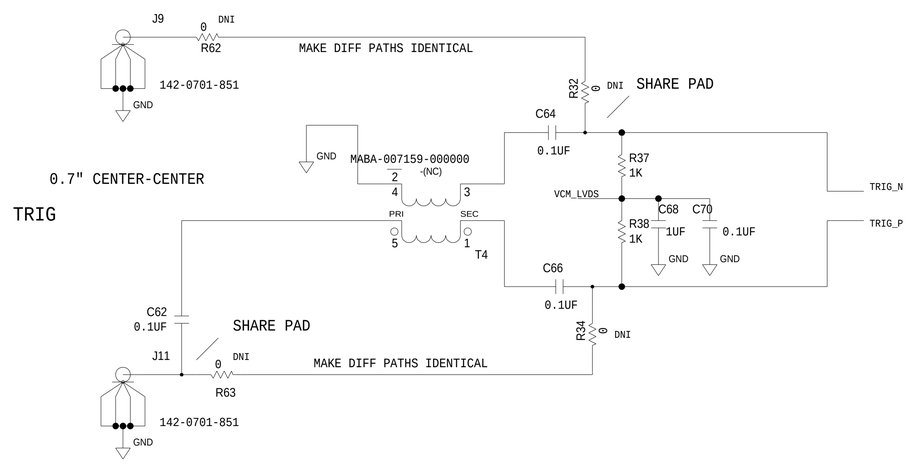
PDWN FROM FPGA, JUMPER, OR PUSHBUTTON



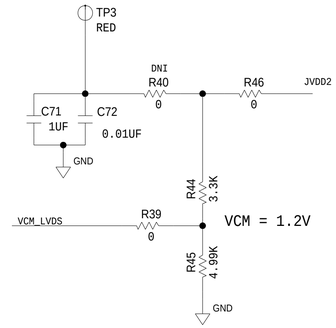
RSTB FROM FPGA OR SVDD2 POWERUP
OR PUSHBUTTON



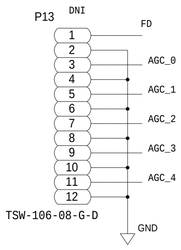
SYSREF,TRIG ARE LVDS AND TERMINATED 100 OHM DIFF ON-CHIP



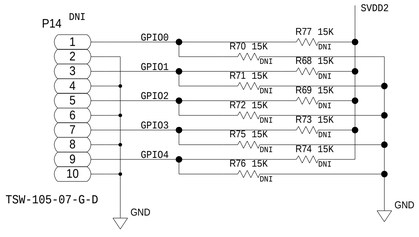
EXTERNAL FORCE 2 X VCM



FUTURE AGC SIGNALS ACCESS HEADER



GPIO HEADER



ANALOG DEVICES

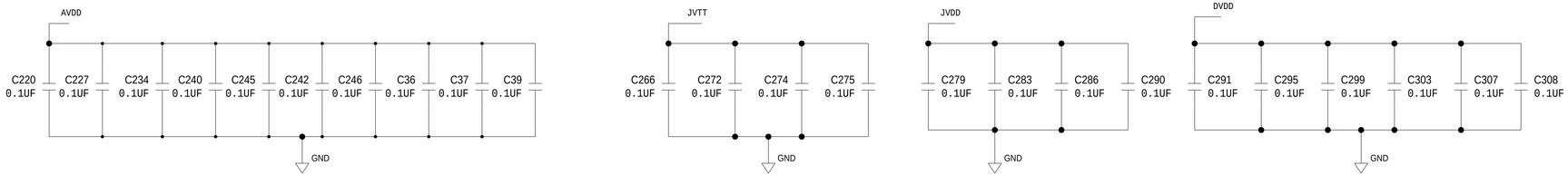
SCHEMATIC

HW TYPE : Characterisation
Product(s): AD9213
.

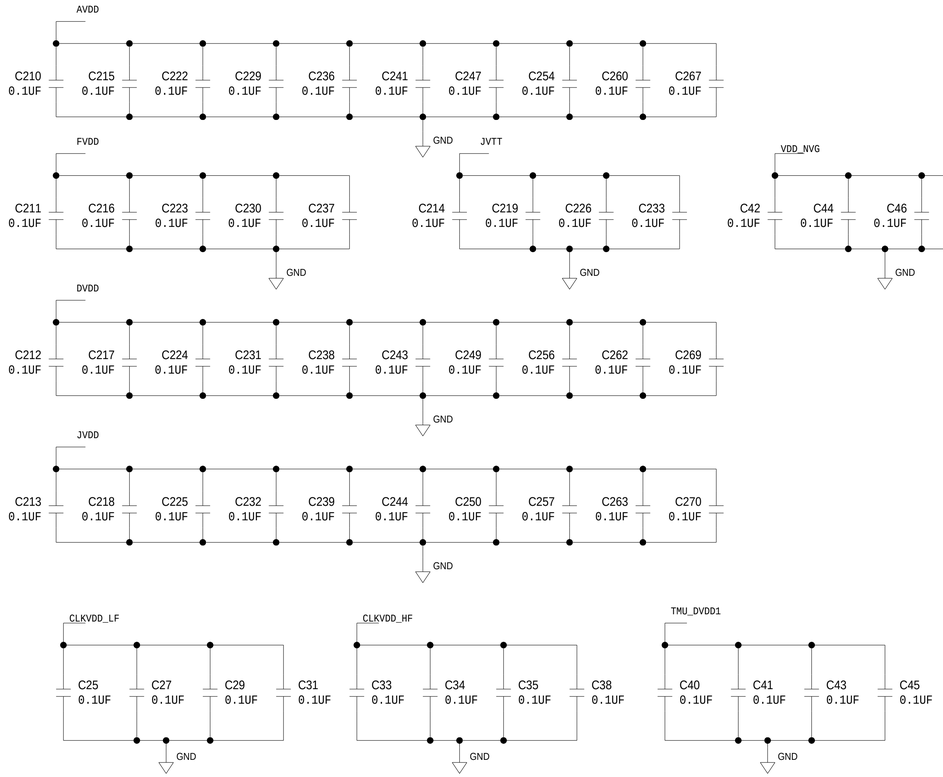
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_044860	C
PTD ENGINEER: S.GIBBS	SIZE: D / SCALE: 1:1	SHEET 5 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

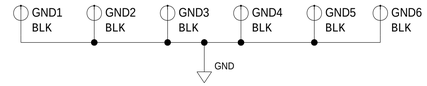
DECOUPLING CAPACITORS DIRECTLY BELOW BGA FOOTPRINT

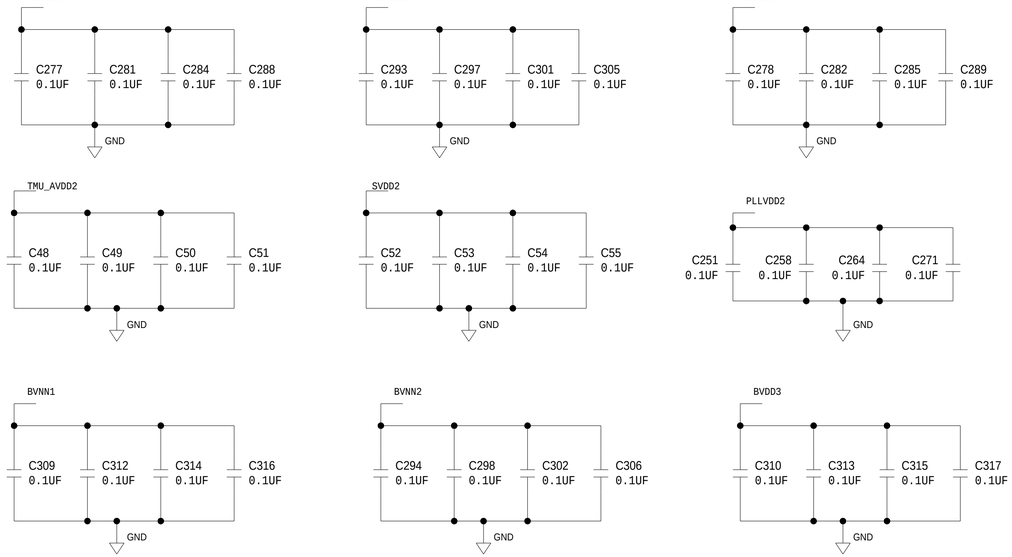


DISTRIBUTED DECOUPLING CAPACITORS



DISTRIBUTED GND TEST PTS





ANALOG DEVICES

SCHEMATIC

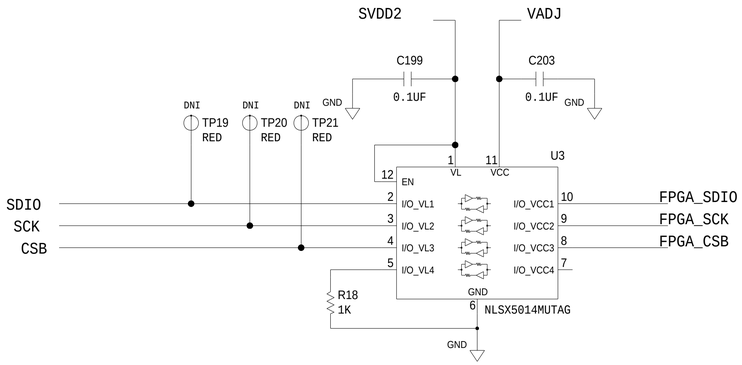
HW TYPE : Characterisation
Product(s): AD9213
.

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_044860	C
PTD ENGINEER	SIZE / SCALE	SHEET 6 OF 8
S.GIBBS	D / 1:1	

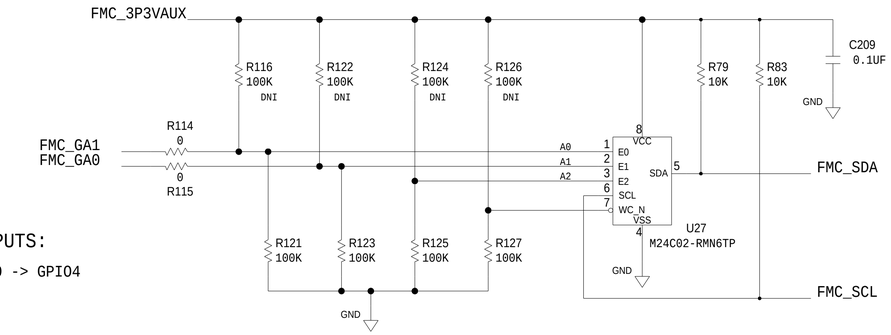
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FMC BUFFERS - SPI,GPIO,RESET,SYNCINB,JTAG,PDWN,EEPROM

3-WIRE SPI



EEPROM



JTAG GPIO MAPPING

INPUTS:

JTDI -> GPIO2

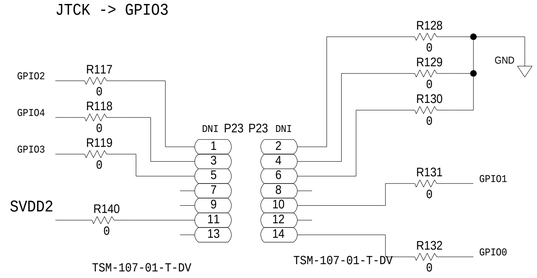
JTMS -> GPIO1

JTRST -> GPIO0

JTCK -> GPIO3

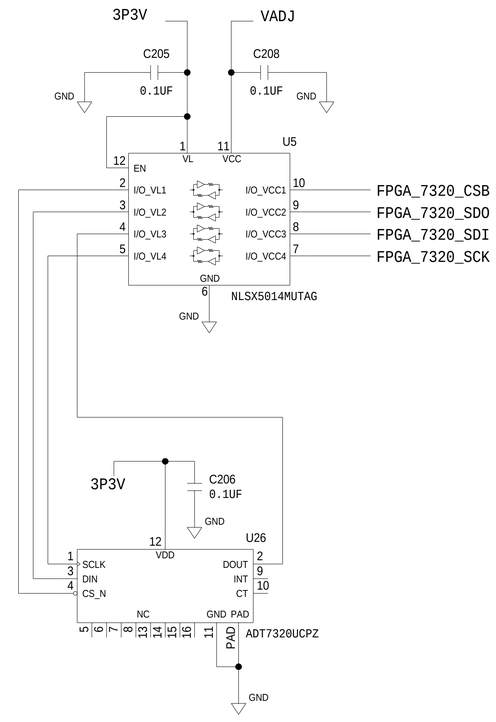
OUTPUTS:

JTDO -> GPIO4

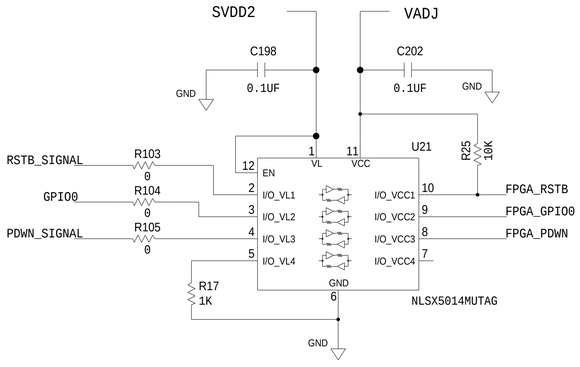


FOR JTAG OPERATION
PIN 8 MUST BE REMOVED AS KEY
PINS 7, 9, 13, 8, 12 ARE NO CONNECT

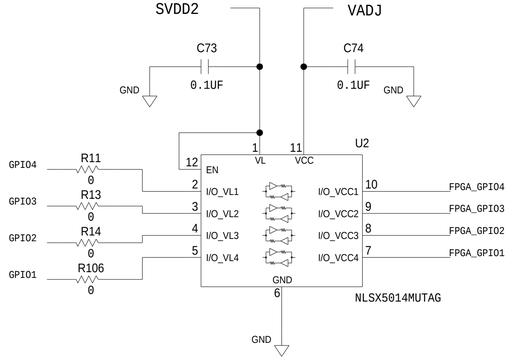
BOARD TEMPERATURE SENSOR



GPIO 0,RSTB,PDWN



GPIO 1-4 INPUTS



ANALOG DEVICES

SCHEMATIC

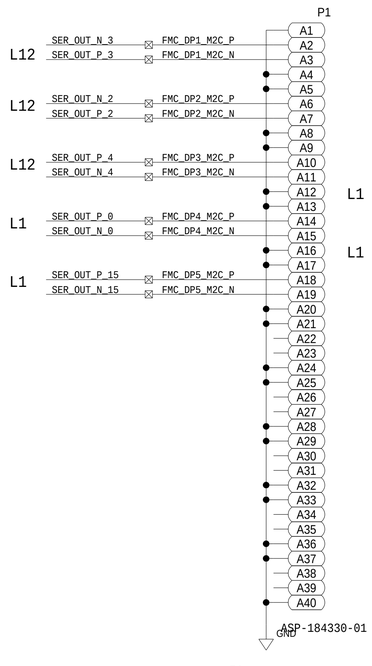
HW TYPE : Characterisation
Product(s): AD9213
.

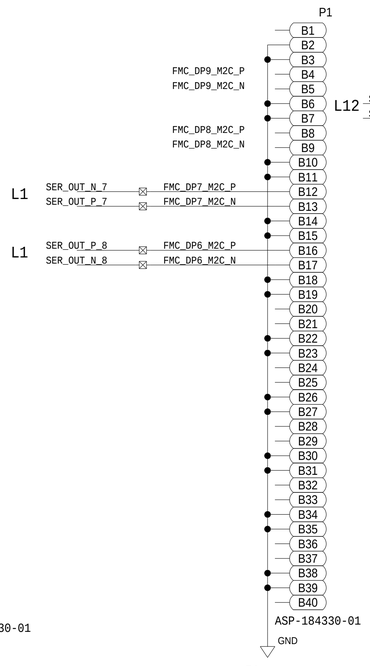
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_044860	REV C
PTD ENGINEER S.GIBBS	SIZE D / SCALE 1:1	SHEET 7 OF 8

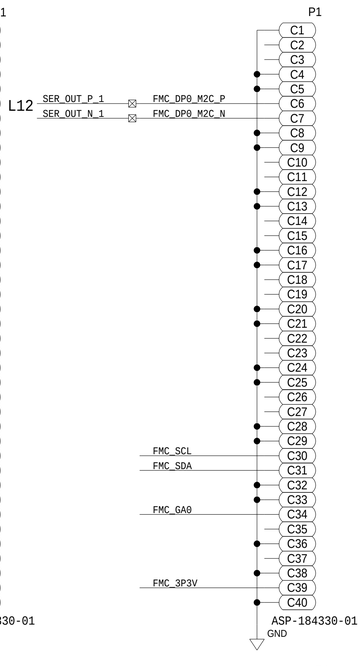
SER_OUT PAIRS ASSIGNED TO TOP (L1) OR BOTTOM (L12)
DPX QUADS ASSIGNED TO DUT QUADS; CHANGES NEED DISCUSSION

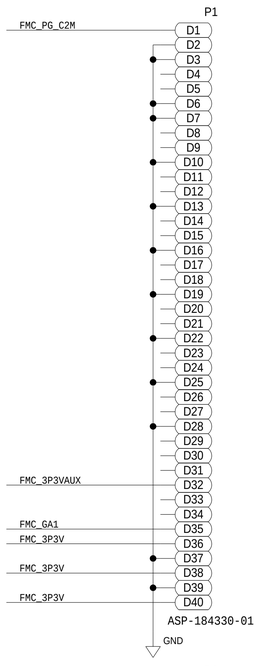
FMC+ HSPC CONNECTOR

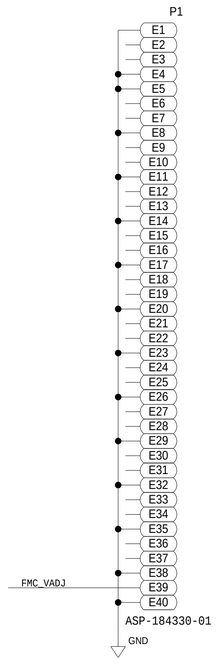
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

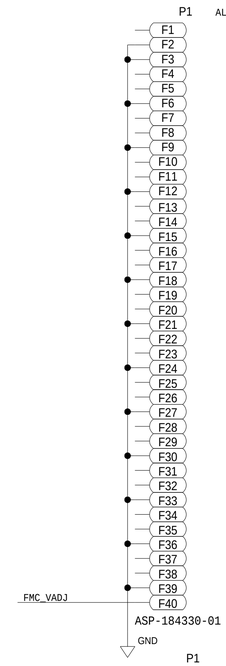


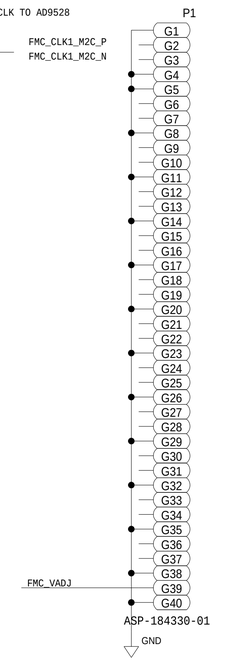


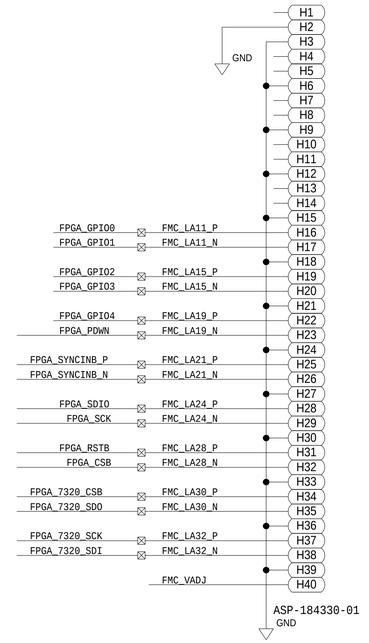


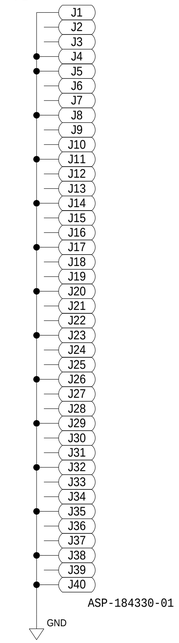


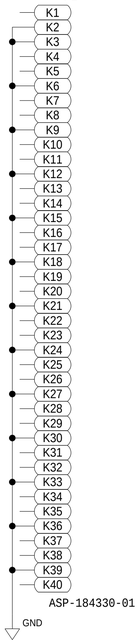


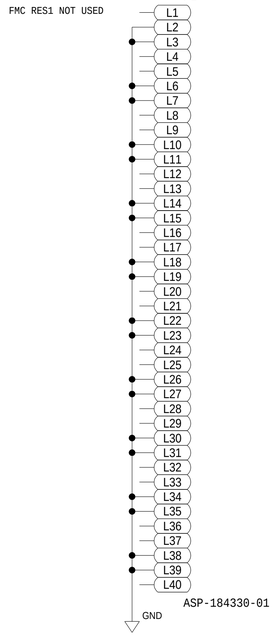


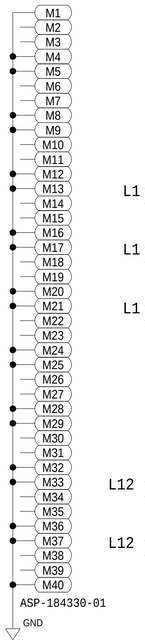


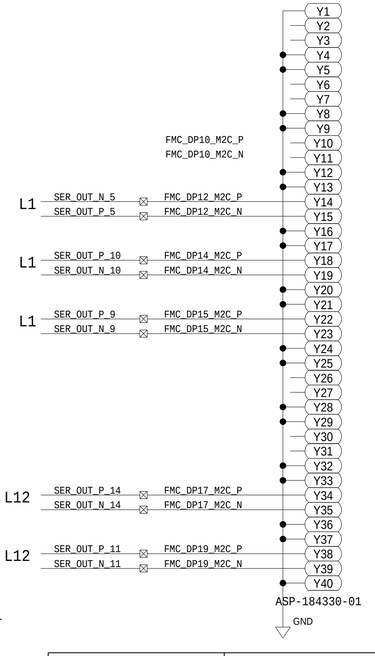


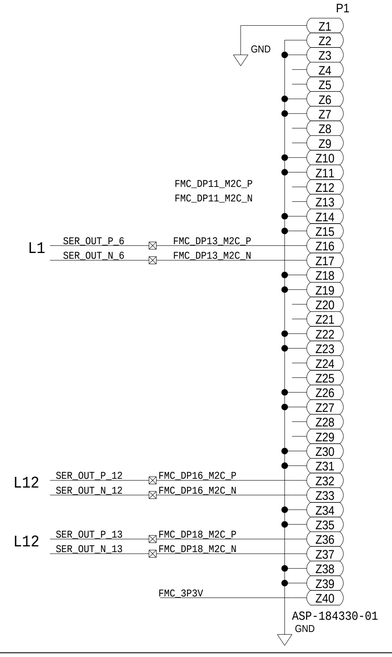












NOTE:SER_OUT PINS SHOULD BE FIT INTO
ADJACENT QUADS 0-3,4-7,8-11,12-15,16-19
FPGA_SYNCINB SHOULD BE DIFF CMOS DRIVE

ANALOG DEVICES

SCHEMATIC

HW TYPE : Characterisation
Product(s): AD9213
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DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_044860	C
PTD ENGINEER: S.GIBBS	SIZE: D / SCALE: 1:1	SHEET 8 OF 8