EVAL-ADAS3022EDZ

Revision history

Date	Rev	Description
2.1.2012	0.1	Document creation
11.07.2017	0.2	Changed clock frequency to 40 MHz

Contents

1. ADAS3022 driver HDL code description
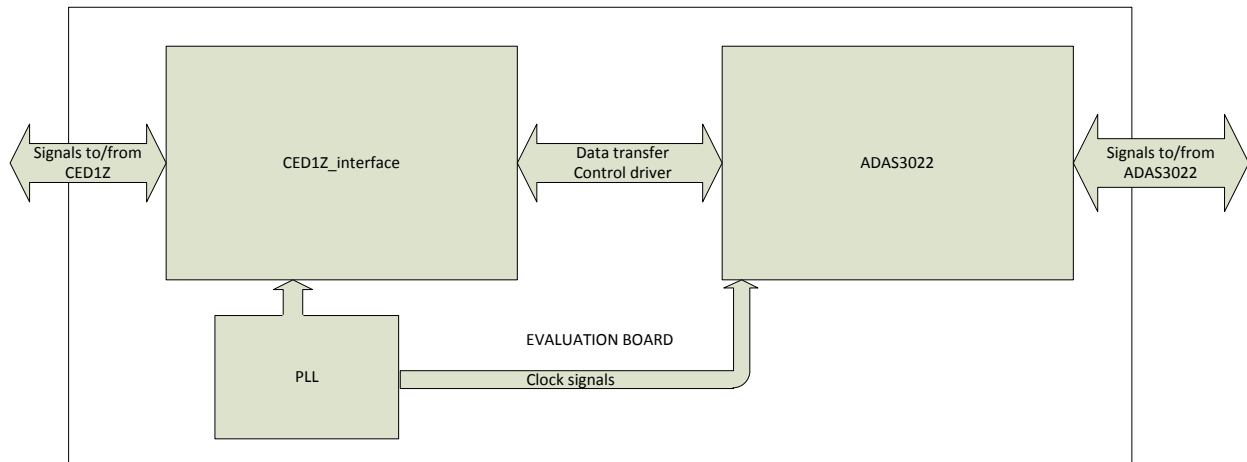
1.1 System overview

Figure 1 System overview

In order to acquire data from the ADAS3022, several modules are implemented on the Evaluation Board FPGA. Below is a short description of these modules.

1.2 ADAS3022

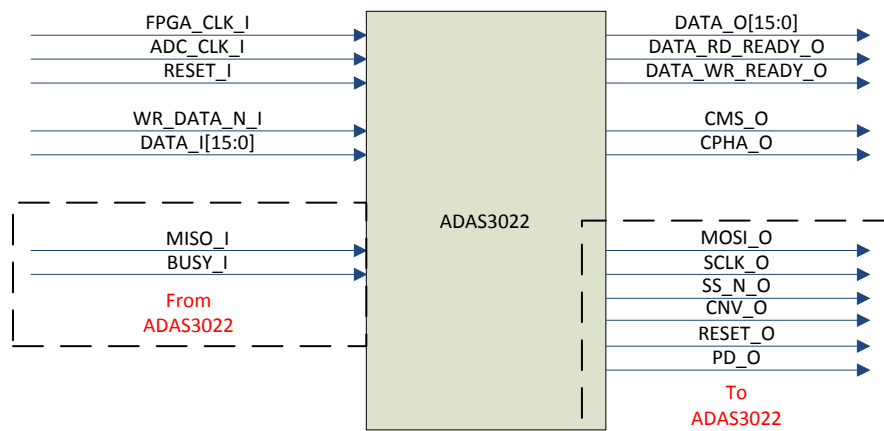This module is the actual driver of the ADAS3022 data acquisition system.

Figure 2 AD7626 module

Port	Direction	Width	Description
General connectors			
FPGA_CLK_I	IN	1	40MHz clock signal
ADC_CLK_I	IN	1	40MHz clock signal
RESET_I	IN	1	Reset
CED1Z_interface connectors			
WR_DATA_N_I	IN	1	Signal used to write data in the driver's internal registers, data which will be sent to the ADAS3022
DATA_I	IN	16	Data bus, used to send new configuration words to the ADAS3022
DATA_O	OUT	16	Parallel port to transfer the data to the CED1Z_interface module.
DATA_RD_READY_O	OUT	1	Signals that at port DATA_O there is new data available
DATA_WR_READY_O	OUT	1	Signals that the write from CED1Z_interface has been successfully performed
CMS_O	OUT	1	The value of the CMS bit in the ADAS configuration register
CPHA_O	OUT	1	The value of the CPHA bit in the ADAS configuration register
ADAS3022 connectors			
MISO_I	IN	1	Signal connected to the SDO pin of the ADAS3022
BUSY_I	IN	1	Signal connected to the BUSY pin of the ADAS3022
MOSI_O	OUT	1	Signal connected to the DIN pin of the ADAS3022
SCLK_O	OUT	1	Signal connected to the SCK pin of the ADAS3022. 40 MHz clock
SS_N_O	OUT	1	Signal connected to the CS_N pin of the ADAS3022
CNV_O	OUT	1	Signal connected to the CNV pin of the ADAS3022
RESET_O	OUT	1	Signal connected to the RESET pin of the ADAS3022
PD_O	OUT	1	Signal connected to the PD pin of the ADAS3022

1.3 CED1Z_inteface

This module is used to communicate with the CED1Z board. It reads the data from the ADAS3022 module and forwards it to the CED1Z board. It also forwards write requests from the CED1Z board to the ADAS3022 module, in order to reconfigure the ADAS3022 data acquisition system.

1.4 PLL

This module is used to generate a 40MHz clock signal from the 100MHz external clock signal that is available on the evaluation board.