ADAS3022

Revision history

Date	Rev	Description
2.01.2012	0.1	Document creation

Contents

1. Introduction

This module is intended to be used with the ADAS3022 PrC 16 Bit, 1 MSPS, 8 Channel Data Acquisition System, together with the Altera Avalon Interface. The module connects the CPU to the IC using a custom SPI Interface, controlling the required signals for starting a conversion or reading data automatically.

2. Architecture

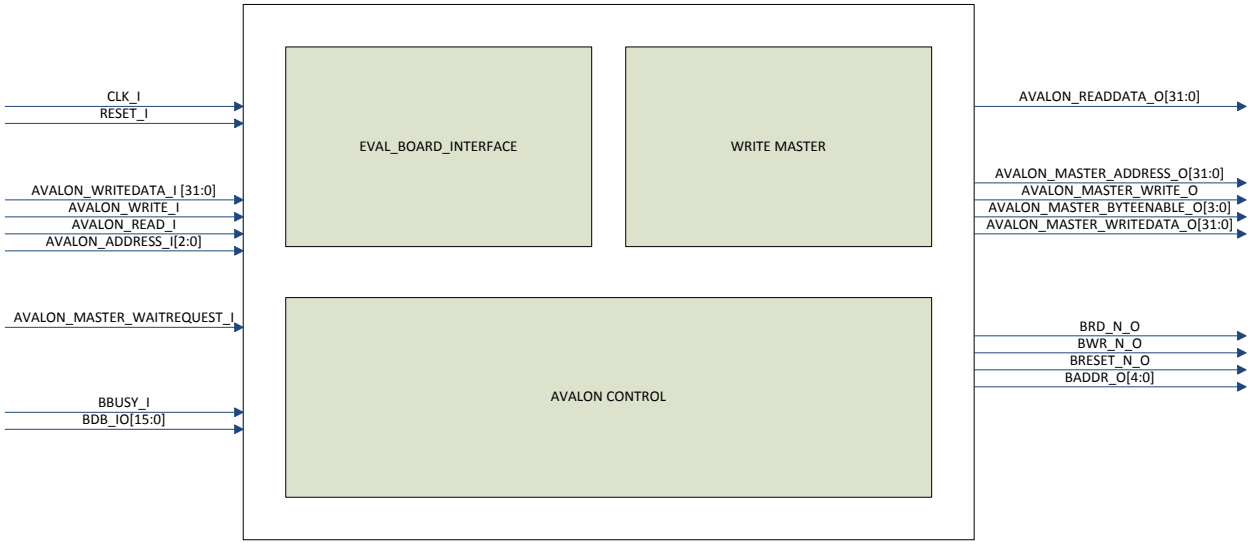

Fig. 1 Avalon core module components

2.1 I/O description

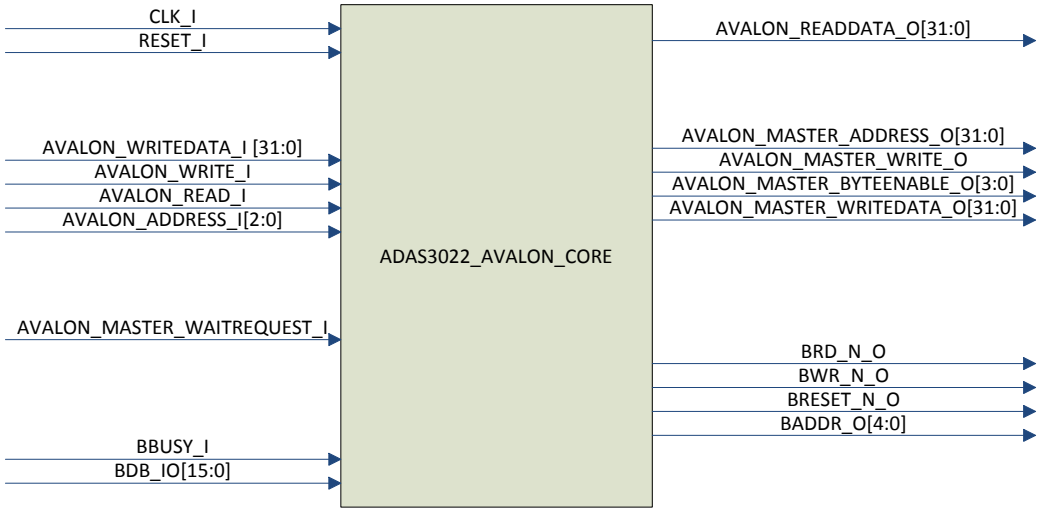

Figure 2 Avalon core pinout

Port	Direction	Width	Description
General connectors			
CLK_I	IN	1	System clock
RESET_I	IN	1	System reset
Avalon Slave Interface			
AVALON_WRITEDATA_I	IN	32	Slave write data bus
AVALON_WRITE_I	IN	1	Slave write data request
AVALON_READ_I	IN	1	Slave read data request
AVALON_ADDRESS_I	IN	2	Slave address bus
AVALON_READDATA_O	OUT	32	Slave read data bus
Avalon Master Interface			
AVALON_MASTER_WAITREQUEST	IN	1	Master wait request signal
AVALON_MASTER_ADDRESS_O	OUT	32	Master address bus
AVALON_MASTER_BYTEENABLE_O	OUT	4	Master byte enable signal
AVALON_MASTER_WRITEDATA_O	OUT	32	Master write data bus
External connectors			
BDB_I	IN	16	Bidirectional data bus used to write/read data to/from the ADAS302xEDZ board
BBUSY_I	IN	1	Logic output that indicates the status of the conversion. Once the conversion is complete and the result is available in the output register, the BUSY output goes high
BRD_N_O	OUT	1	Signal used by the CED1Z board to read data from the ADAS302xEDZ board
BWR_N_O	OUT	1	Signal used by the CED1Z board to write data to the ADAS302xEDZ board
BADDR_O	OUT	3	Used to select the register to be read from the ADAS302xEDZ board
BRESET_N_O	OUT	1	Used to reset the ADAS302xEDZ board

Table 1 IO ports

2.2 Registers description

Name	Offset	Width	Access	Description
CONTROL_REGISTER	0	32	RW	Bit 0 is used to start data acquisition Bit 1 is used to initiate software reset of the core Bit 2 is used to configure the Avalon write master core to write data to the same location Bit 3 is used to write data to the ADAS302xEDZ board
ACQ_COUNT_REGISTER	1	32	RW	Register used to configure the number of samples to be acquired when acquisition is started
BASE_REGISTER	2	32	RW	Register used to configure the base address of the memory location where the acquired data is to be written
STATUS	3	32	R	Bit 0 is used to signal that the acquisition is complete Bit 1 is used to signal that the internal memory buffer has been overflown Bit 2 is used to signal that the user has performed a write to a read only register
DUT_WRITE_REGISTER	4	32	W	Register used to perform writes on the device under test. Bits [15:0] are used for data, and [18:16] are used as address. The rest are discarded
Reserved	5-7	32	-	Reserved

Table 2 Registers

2.3 Modules description

The core can be considered to have several logical modules: Evaluation Board interface communication core, Avalon write master module and general control module.

If bit 0 of the status register is 1, a new acquisition is started. Except for the case in which bit 1 of the status register is overwritten with value 1, the acquisition stops after the number of samples from the ACQ_COUNT_REGISTERS are acquired.

If bit 1 of the status register is 1, the core is reset. All the internal counters are set to 0.

2.3.1 EVAL_BOARD_INTERFACE core

This block controls the signals required for data acquisition from the evaluation board. Data is written in the Avalon master writer module memory.

2.3.2 Avalon write master module

This module is used to store the data acquired from the ADAS3022 in the systems memory. This block is based on the Altera templates: http://www.altera.com/support/examples/nios2/exm-avalon-mm.html

2.3.3 General control module

This block is an Avalon slave module which controls the overall functionality of the part. It allows the user to perform read/write of the registers. It also merges two samples into a 32bit word for faster transfer to the systems memory.