AD7606 HDL Driver

Revision history

Date	Rev	Description
09.21.2012	0.1	Document creation

Contents

1. Introduction

This document describes the HDL driver for the AD7606 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

2. Architecture

Fig. 1 presents the block diagram of the AD7606 IP.

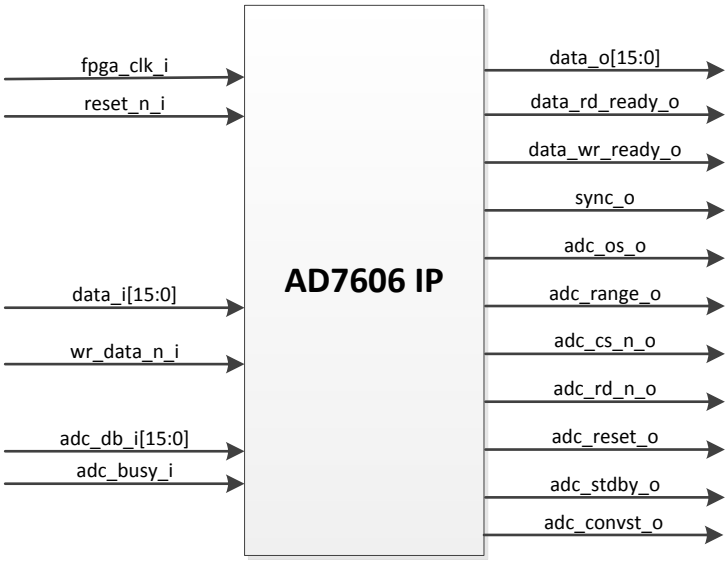

Fig. 1 AD7606 IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input.
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
WR_DATA_N_I	IN	1	Active low signal use to initiate a data write. The data to be written to the driver must be active on the DATA_I bus one clock cycle after this signal is set low and must be kept active until the DATA_WR_READY_O signal returns to high. If the ADC is performing a conversion while the WR_DATA_N_I signal is set low then the DATA_WR_READY_O will transition from high to low only when the conversion is complete.
DATA_I	IN	16	Input bus used to receive the data to configure the operation of AD7606 driver.
DATA_O	OUT	16	Outputs the data read from the ADC.

DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7606. The IP continuously reads the conversion results from the AD7606 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
DATA_WR_READY_O	OUT	1	Active high signal to indicate the status of a write operation to the IP. One clock cycle after the WR_DATA_N_I signal is set low the DATA_WR_READY_O is also set low and returns to high only after the write operation to the AD7606 is complete. During a write operation the data read operations are suspended.
SYNC_O	OUT	1	Signal used to signal that a new conversion has begun, and the next data available will correspond to channel 1.
Ad7606 control and data ports			
ADC_DB_I	IN	16	ADC data bus used to read data from the AD7606.
ADC_BUSY_I	IN	1	ADC Busy Output. Logic output that indicates the status of the conversion. The BUSY output goes high following the falling edge of CONVST and stays high for the duration of the conversion. Once the conversion is complete and the result is available in the output register, the BUSY output goes low. The track-and-hold returns to track mode just prior to the falling edge of BUSY on the 13th rising edge of CLKIN.
ADC_OS_O	OUT	3	These inputs are used to select the oversampling ratio.
ADC_RANGE_O	OUT	1	Analog Input Range Selection. The polarity of this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is +-10V for all channels. If this pin is tied to a logic low, the analog input range is +-5V. A logic change has immediate effect.
ADC_CS_N_O	OUT	1	ADC Chip Select. Active low logic input used in conjunction with RD to read conversion data.
ADC_RD_N_O	OUT	1	ADC Read pin. Active low logic input used in conjunction with CS to access the conversion result. The conversion result is placed on the data bus following the falling edge of RD read while CS is low.
ADC_RESET_O	OUT	1	Reset pin. When set to logic high, the rising edge of RESET resets the AD7606.
ADC_STDBY_O	OUT	1	Standby Mode pin. This pin is used to place the AD7606 into one of the two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin.
ADC_CONVST_N_O	OUT	1	A falling edge on CONVST is used to initiate a conversion. The track-and-hold goes from track mode to hold mode on the falling edge of CONVST and the conversion process is initiated at this point. Following power-down, when operating in auto-shutdown or auto-standby modes, a rising edge on CONVST is used to power up the device.

Table 1 IO ports

Fig. 2 presents the timing diagram for read operations.

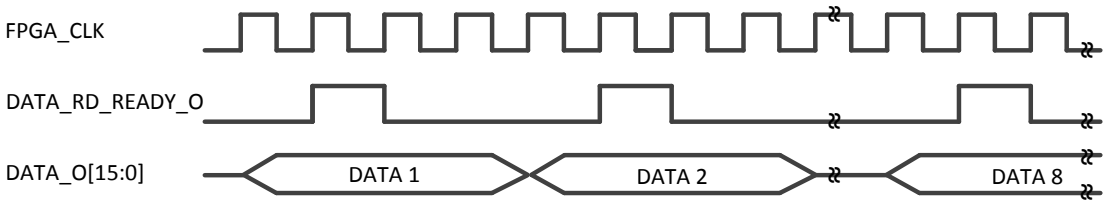

Fig. 2. Read operations timing diagram

Fig. 3 presents the timing diagram for write operations.

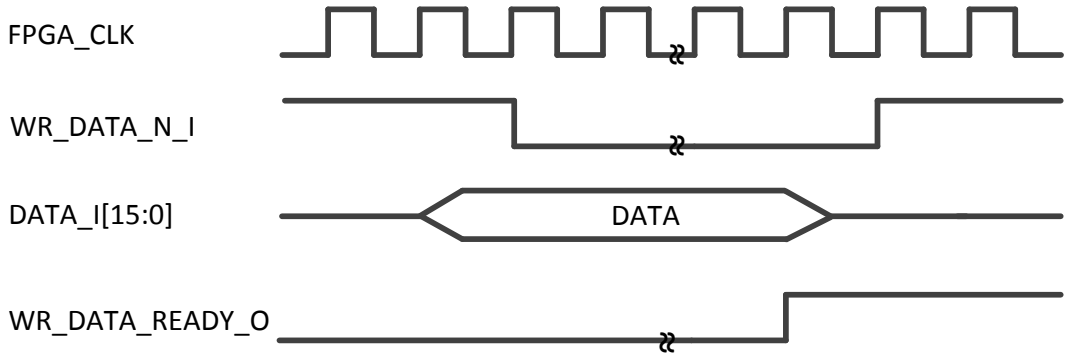

Fig. 3 Write operations timing diagram