

Revision history

Date	Rev	Description
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1. Introduction

This module is intended to be used to communicate with the EVAL-AD7262EDZ evaluation board. The module connects the CPU to the IC using a custom SPI Interface, controlling the required signals for initialize the converter, starting a conversion or reading data automatically.

2. Architecture

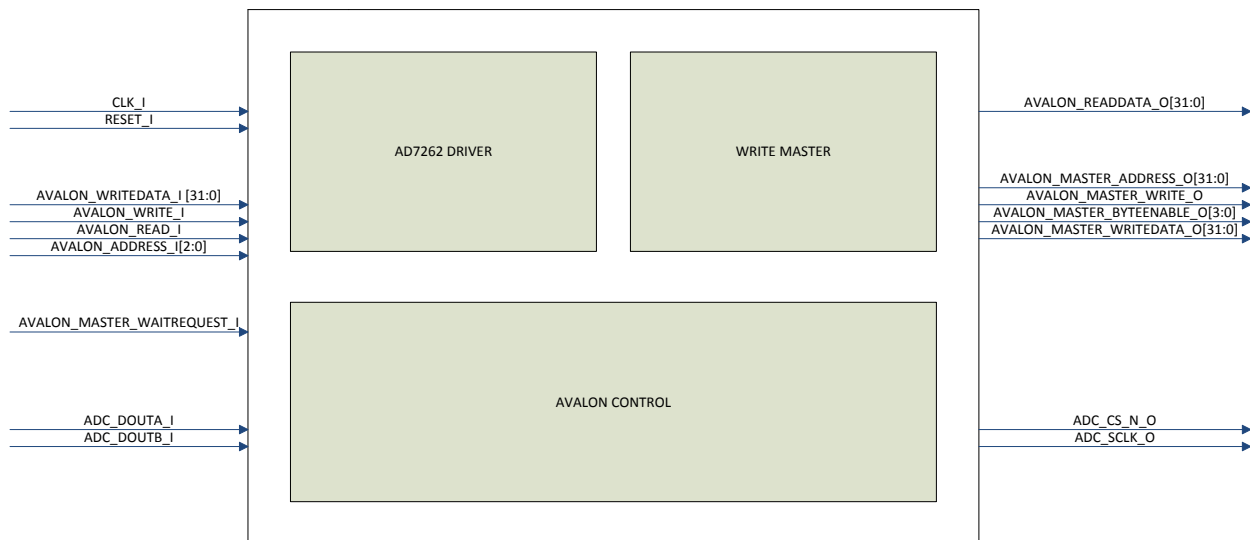


Figure. 1 Avalon core module components

2.1 I/O description

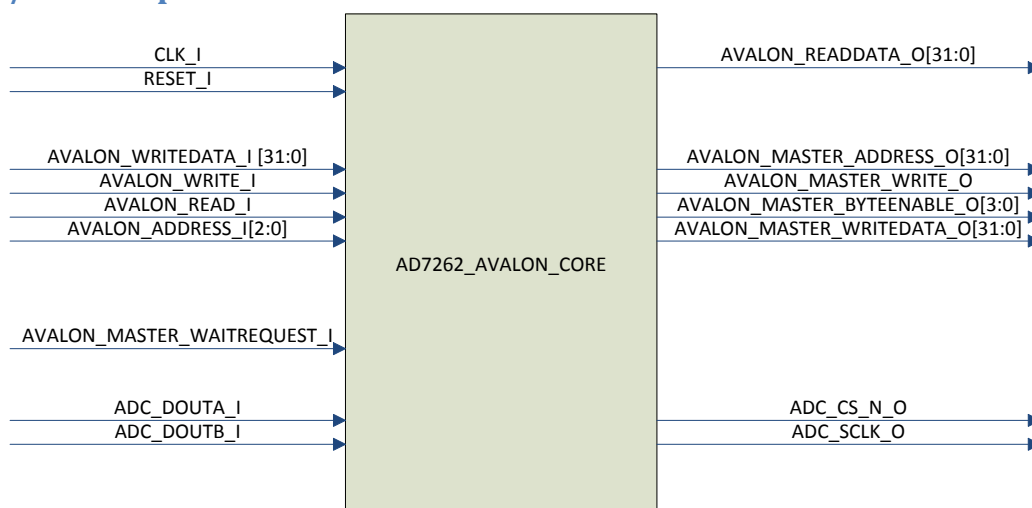


Figure 2 Avalon core pinout

Port	Direction	Width	Description
<i>General connectors</i>			
CLK_I	IN	1	System clock
RESET_I	IN	1	System reset
<i>Avalon Slave Interface</i>			
AVALON_WRITEDATA_I	IN	32	Slave write data bus
AVALON_WRITE_I	IN	1	Slave write data request
AVALON_READ_I	IN	1	Slave read data request
AVALON_ADDRESS_I	IN	2	Slave address bus
AVALON_READDATA_O	OUT	32	Slave read data bus
<i>Avalon Master Interface</i>			
AVALON_MASTER_ADDRESS_O	OUT	32	Master address bus
AVALON_MASTER_WRITE_O	OUT	1	Master write enable signal
AVALON_MASTER_BYTEENABLE_O	OUT	4	Master byte enable signal
AVALON_MASTER_WRITEDATA_O	OUT	32	Master write data bus
AVALON_MASTER_WAITREQUEST_I	IN	1	Master wait request
<i>External connectors</i>			
ADC_SCLK_O	OUT	1	Serial clock for AD7262
ADC_CS_N_O	OUT	1	Chip select, active low logic input.
ADC_DOUTA_I	IN	1	Serial data input from first channel, is supplied to each pin as a serial data stream in twos complement format.
ADC_DOUTB_I	IN	1	Serial data input from second channel, is supplied to each pin as a serial data stream in twos complement format.

Table 1 IO ports

2.2 Registers description

Name	Offset	Width	Access	Description
CONTROL_REGISTER	0	32	RW	Bit 0 is used to start data acquisition Bit 1 is used to initiate software reset of the core Bit 2 is used to configure the Avalon write master core to write data to the same location Bit 3 is used to write data to the AD7682EDZ board Bit 4 is used to enable the Test Mode feature of the driver
ACQ_COUNT_REGISTER	1	32	RW	Register used to configure the number of samples to be acquired when acquisition is started
BASE_REGISTER	2	32	RW	Register used to configure the base address of the memory location where the acquired data is to be written
STATUS	3	32	R	Bit 0 is used to signal that the acquisition is complete Bit 1 is used to signal that the internal memory buffer has been overflown Bit 2 is used to signal that the user has performed a write to a read only register
DUT_WRITE_REGISTER	4	32	W	Register used to perform writes on the device under test. Bits [15:0] are used for data, and [18:16] are used as address. The rest are discarded
DUT_STATE_REGISTER	5	32	R	Bit [3:0] the actual state value of the driver's FSM Bit [15:8] the actual state value of the Avalon Core FSM
Reserved	6-7	32	-	Reserved

Table 2 Registers

2.3 Modules description

The core can be considered to have several logical modules: AD7262 driver core, Avalon write master module and general control module.

If bit 0 of the status register is 1, a new acquisition is started. Except for the case in which bit 1 of the status register is overwritten with value 1, the acquisition stops after the number of samples from the ACQ_COUNT_REGISTERS are acquired.

If bit 1 of the status register is 1, the core is reset. All the internal counters are set to 0 and a hardware reset is initiated by the driver.

2.3.1 AD7262 Driver core

This block controls the signals required for data acquisition from the evaluation board. Data is written in the Avalon master writer module memory.

2.3.2 Avalon write master module

This module is used to store the data acquired from the AD7682 in the systems memory. This block is based on the Altera templates:

<http://www.altera.com/support/examples/nios2/exm-avalon-mm.html>

2.3.3 General control module

This block is an Avalon slave module which controls the overall functionality of the part. It allows the user to perform read/write of the registers.