AD7942 HDL Driver

Revision history

Date	Rev	Description
03.05.2012	0.1	Document creation

Contents

1.

2. Introduction

This document describes the HDL driver for the AD7942 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

3. Architecture

Fig. 1 presents the block diagram of the AD7942 IP.

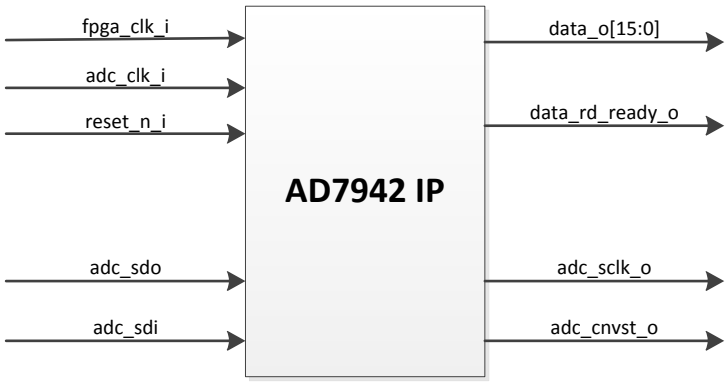

Fig. 1 AD7942 IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input.
ADC_CLK_I	IN	1	Clock to be sent to the ADC during the conversion process.
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
DATA_O	OUT	16	Outputs the data read from the ADC.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7942. The IP continuously reads the conversion results from the AD7942 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
Ad7942 control and data ports			
ADC_SDO	IN	1	ADC Serial Data Output. The conversion result is output on this pin. It is synchronized to SCLK.
ADC_SDI	IN	1	ADC Serial Data Input. This pin is currently not used in the design.

ADC_SCLK_O	OUT	1	ADC Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
ADC_CNVST_O	OUT	1	ADC Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part, chain, or CS mode. In CS mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.

Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

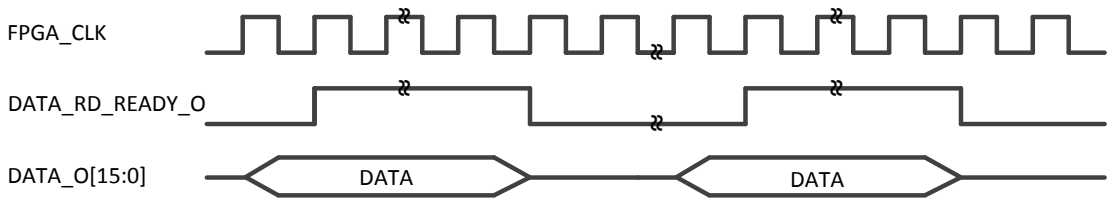

Fig. 2. Read operations timing diagram

Note: The driver is intended to be used for AD7942 ADCs configured in /CS MODE, 3-WIRE, WITHOUT BUSY INDICATOR.