

## **AD7686 HDL Driver**

### **Revision history**

<b>Date</b>	<b>Rev</b>	<b>Description</b>
10.03.2012	0.1	Document creation

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## 1. Introduction

This document describes the HDL driver for the AD7686 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

## 2. Architecture

Fig. 1 presents the block diagram of the AD7686 IP.

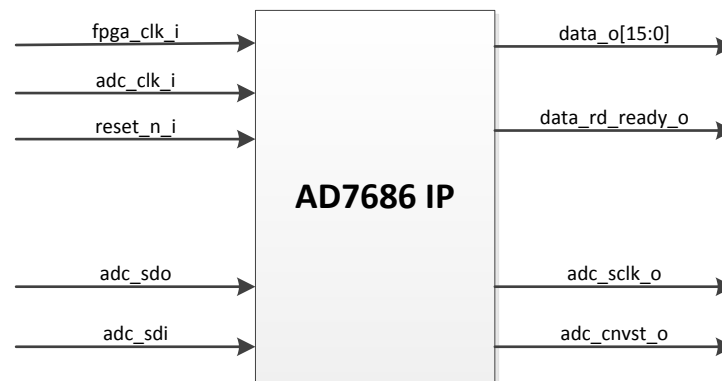


Fig. 1 AD7686 IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
<i>Clock and reset ports</i>			
FPGA_CLK_I	IN	1	Main clock input.
ADC_CLK_I	IN	1	Clock to be sent to the ADC during the conversion process.
RESET_N_I	IN	1	Active low reset signal.
<i>IP control and data ports</i>			
DATA_O	OUT	16	Outputs the data read from the ADC.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7686. The IP continuously reads the conversion results from the AD7686 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
<i>Ad7980 control and data ports</i>			
ADC_SDO	IN	1	ADC Serial Data Output. The conversion result is output on this pin. It is synchronized to SCLK.
ADC_SDI	IN	1	ADC Serial Data Input. This pin is currently not used in the design.
ADC_SCLK_O	OUT	1	ADC Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
ADC_CNVTST_O	OUT	1	ADC Convert Input. This input has multiple functions. On its

			leading edge, it initiates the conversions and selects the interface mode of the part, chain, or CS mode. In CS mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
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Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

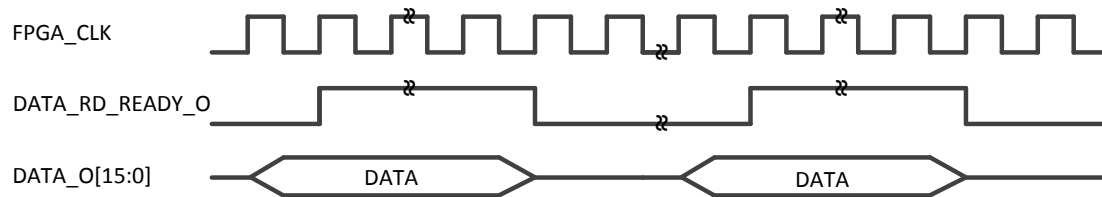


Fig. 2. Read operations timing diagram

**Note:** The driver is intended to be used for AD7686 ADCs configured in /CS MODE, 3-WIRE, WITHOUT BUSY INDICATOR.