AD7450A HDL Driver

Revision history

Date	Rev	Description
11.23.2012	0.1	Document creation
11.27.2012	0.2	Removed pins which are not used by the HDL

Contents

1. Introduction

This document describes the HDL driver for the AD7450A part. The driver is written in Verilog and can be integrated in designs with or without softcores.

2. Architecture

Fig. 1 presents the block diagram of the AD7450A IP.

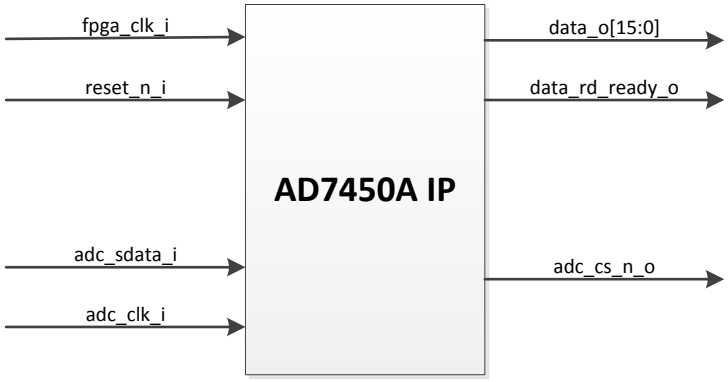

Fig. 1 AD7450A IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input.
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
DATA_O	OUT	16	Outputs the data read from the ADC.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7450A. The IP continuously reads the conversion results from the AD7450A and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
Ad7450A control and data ports			
ADC_SDATA_I	IN	1	The conversion result from the AD7450A is provided on this pin as a serial data stream.
ADC_CLK_I	IN	1	This pin is connected to an external clock, which will drive the data acquisition process from the AD7450A.
ADC_CS_N_O	OUT	1	This pin provides the dual function of initiating a conversion on the AD7450A and framing the serial data transfer.

Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

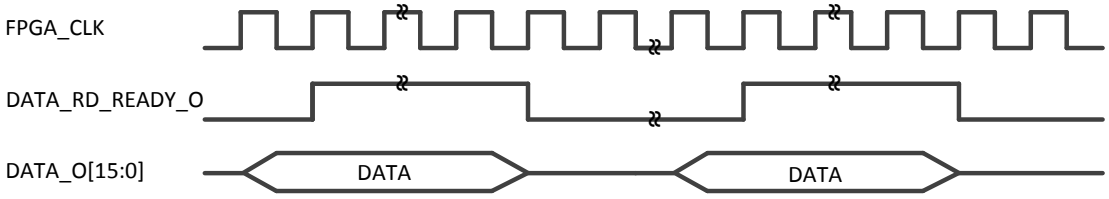

Fig. 2. Read operations timing diagram

Note: The driver is intended to be used with the AD7450ASDZ evaluation board.