AD7328 HDL Driver

Revision history

Date	Rev	Description
04.12.2012	0.1	Document creation

Contents

1. Introduction

This document describes the HDL driver for the AD7328 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

2. Architecture

Fig. 1 presents the block diagram of the AD7328 IP.

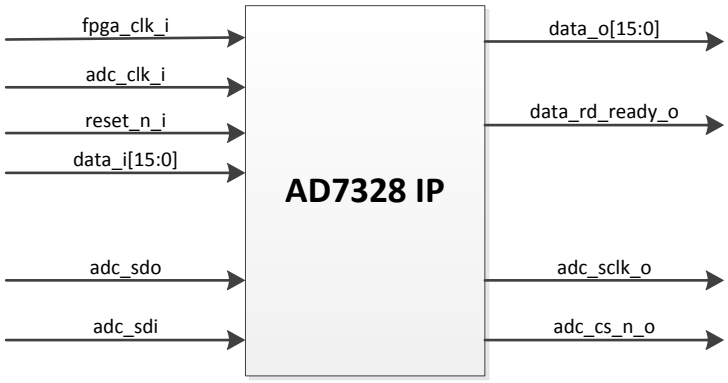

Fig. 1 AD7328 IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input.
ADC_CLK_I	IN	1	Clock to be sent to the ADC during the conversion process.
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
DATA_I	IN	16	Write data to ADC.
DATA_O	OUT	16	Outputs the data read from the ADC.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7328. The IP continuously reads the conversion results from the AD7328 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
Ad7328 control and data ports			
ADC_SDO	IN	1	ADC Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 16 SCLKs are required to access the data. The data stream consists of three channel identification bits, the sign bit and 12 bits of conversion data. The data is provided MSB first.

ADC_SDI	IN	1	ADC Data In. Data to be written to the on-chip registers is provided on this input and is clocked into the register on the falling edge of the SCLK.
ADC_SCLK_O	OUT	1	ADC Serial Data Clock Input. A serial clock input provides the SCLK used for accessing the data from the AD7328. This clock is also used as the clock source for the conversion process.
ADC_CS_N_O	OUT	1	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7328 and frames the serial data transfer.

Table 1. IO ports

Fig. 2 presents the timing diagram for read operations.

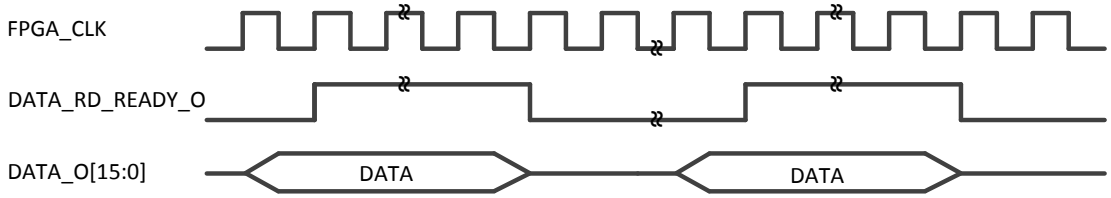

Fig. 2. Read operations timing diagram