AD7327 HDL Driver

Revision history

Date	Rev	Description
11.027.2012	0.1	Document creation

Contents

1. Introduction

This document describes the HDL driver for the AD7327 part. The driver is written in Verilog and can be integrated in designs with or without softcores.

2. Architecture

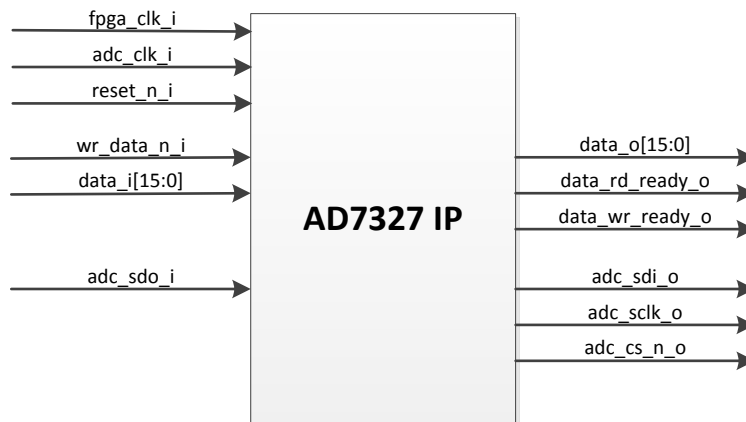Fig. 1 presents the block diagram of the AD7327 IP.

Fig. 1 AD7327 IP

Table 2 presents a description of the IP's IO ports.

Port	Direction	Width	Description
Clock and reset ports			
FPGA_CLK_I	IN	1	Main clock input. 100MHz
ADC_CLK_I	IN	1	Clock to be sent to the ADC during the conversion process. 10MHz
RESET_N_I	IN	1	Active low reset signal.
IP control and data ports			
WR_DATA_N_I	IN	1	Active low signal use to initiate a data write. The data to be written to the driver must be active on the DATA_I bus one clock cycle before this signal is set low and must be kept active until the DATA_WR_READY_O signal returns to high. If the ADC is performing a conversion while the WR_DATA_N_I signal is set low then the DATA_WR_READY_O will transition from high to low only after the conversion is complete.
DATA_I	IN	16	Write data to ADC.
DATA_O	OUT	16	Outputs the data read from the ADC.
DATA_RD_READY_O	OUT	1	Active high signal to indicate the status of a read operation from the AD7327. The IP continuously reads the conversion

			results from the AD7327 and outputs them on the DATA_O bus. When this signal is high data can be read from the DATA_O bus.
DATA_WR_READY_O	OUT	1	Active high signal to indicate the status of a write operation to the IP. One clock cycle after the WR_DATA_N_I signal is set low the DATA_WR_READY_O is also set low and returns to high only after the write operation to the AD7327 is complete. During a write operation the data read operations are suspended.
Ad7327 control and data ports			
ADC_SDO_I	IN	1	The conversion output data is supplied to this pin.
ADC_SDI_O	OUT	1	Data to be written to the ADC is provided to this pin, and is clocked into the AD7327 on the falling edge of SCLK.
ADC_SCLK_O	OUT	1	This pin is used for accessing data from the AD7327. It is also used for the conversion process.
ADC_CS_N_O	OUT	1	This input provides the dual function of initiating conversions on the AD7327 and frames the serial data transfer.

Table 1. IO ports

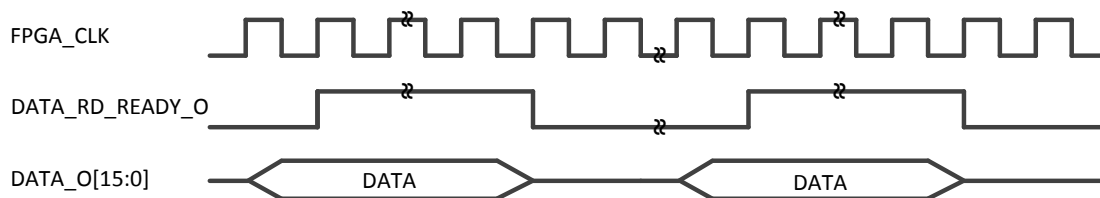Fig. 2 presents the timing diagram for read operations.

Fig. 2. Read operations timing diagram
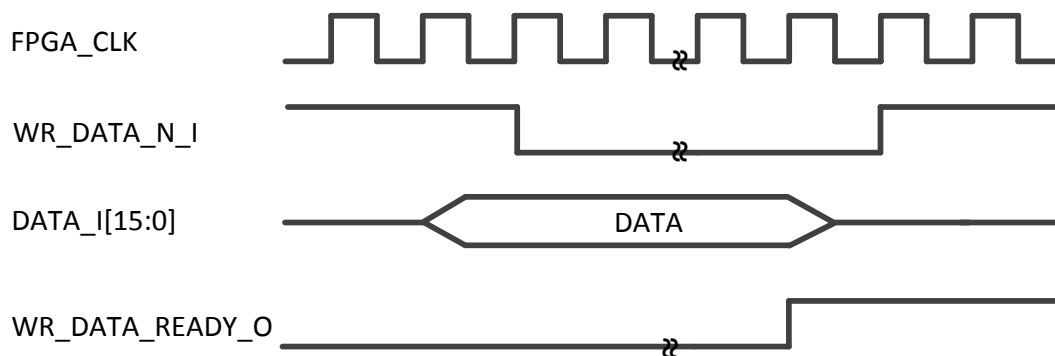
Fig. 3 presents the timing diagram for write operations.

Fig. 3 Write operations timing diagram